EPSONEXCEED YOUR VISION

S1C31D50/51/41 (rev3.00)

32-bit Single Chip Sound Microcontroller

- Arm® 32-but RISC CPUcore Cortex®-M0+
- D50:192K / D51:192K / D41:96K bytes Embedded Flash memory
- D50:8K / D51:10K / D41:8K bytes embedded RAM
- Provide Voice Guidance on a buzzer in addition to a speaker
- "Voice/Audio Play"(2ch mixing play, Voice Speed Conversion w/o CPU resource)
- Voice Pitch Conversion Function(only S1C31D41) New
- ±1%(@Ta=0 to 85°C) 16MHzinternal Oscillator (only S1C31D41) NeW



JEW

DESCRIPTIONS

The S1C31D51/D50/D41 is a 32-bit Arm® Cortex®-M0+ MCU which integrates a specific hardware block called the HW Processor, 2type Embedded Flash size 192K(D50/D51)/96K(D41) bytes is supported. Normally, the buzzer does not provide sufficient voice quality and sound pressure, but our newly developed algorithm allows the buzzer to play the voice, and even devices that could not be equipped with a speaker and voice guidance can generate an error or warning, and can improve usability for the end user.

The HW Processor can perform 2ch Voice/Audio Play, Voice Speed Conversion, and Self Memory Check without using any CPU resource, and the S1C31D51/D50/D41 is suitable for home electronics, white goods, and battery-based products which require voice and audio playback.

In addition, the audio playback format uses a high-compression, high-quality sound algorithm, which makes it possible to install multiple languages.

Furthermore, the EPSON Voice Creation PC tool makes development without studio recording easy

■ FEATURES

FEATURES	64 694 9 56	04.004.0.74	NEV		
Model	S1C31D50	S1C31D51	S1C31D41		
CPU	IA O 22 L'I BYCC CRU	G 1 0 MO			
CPU core	Arm® 32-bit RISC CPU con				
Other	Serial-wire debug ports (SW	-DP) and a micro trace buffer	(MTB) included		
Embedded Flash memory	1				
Capacity(for Program&SoundROM)	_	bytes	96K bytes		
Erase/program count		being programmed by the dec	dicated flash loader		
Other	On-board programming fur				
	Flash programming voltage	can be generated internally.			
Embedded RAMs					
General-purpose RAM	8K bytes	10K bytes	8K bytes		
(under HW Processor is not active)	(+ 14K bytes)	(+ 12K bytes)	(+ 18K bytes)		
Instruction cache		-	512 bytes		
HW Processor	ver1.00	ver2.00	ver3.00		
Sound Play FUNCTION					
Voice/Audio Algorithm	EPSON high quality & High of				
Play channels		for background music + Voice			
Sampling Frequency		ck Ground Music + Voice play)	1		
Bitrate	EOV:16/24	/32/40 kbps	EOV:16/24 kbps		
Multi-SoundROM		supported			
Gapless play		supported			
Volume setting	Support	ed(0db to -63.0db:0.5db step	, silence)		
Repeat time setting	Supported(1time	to 255times, repeat until stop	command receive)		
Voice Speed Conversion	Ver1.00	Ver2	/er2.00		
		75% - 125% (5% step)			
Voice Pitch Conversion		-	75% - 125% (5% step)		
Tone Generation		=	supported		
Electromagnetic/Piezoelectric buzzer Voice/Melody	-	suppo	orted		
Self Memory Check FUNCTION		,			
On Chip RAM Check	W/R Check, MARCH-C				
On Chip Flash check	Checksum, CRC				
External SPI-Flash Check	Checksum, CRC				
Sound DAC	· ·				
Sampling Frequency	15.625kHz				
External Differential Circuit Speaker DAC/Election	romagnetic Buzzer DAC/Pic	ezoelectric buzzer DAC			
Sampling Frequency					
(requires to use 16bit PWM Timer(T16B)1ch)	-	15.62	ZOKITZ		

Model	S1C31D50 S1C31D51	S1C31D41
Serial interfaces	51651050 51651051	51651041
UART (UART3)	3 channels	
OAKI (OAKIS)	Baud-rate generator included, IrDA1.0 supported	
	Open drain output, signal polarity, and baud rate divis	ion ratio are configurable
	Infrared communication carrier modulation output ful	
Synchronous serial interface (SPIA)	3 channels	100.011
-,(,	2 to 16-bit variable data length	
	The 16-bit timer (T16) can be used for the baud-rate	generator in master mode.
Quad synchronous serial interface (QSPI)	1 channel	J
	Supports single, dual, and quad transfer modes.	
	Low CPU overhead memory mapped access mode that	t can directly read data from
	the external flash memory with XIP (eXecute-In-Place) mode.
I ² C (I2C)*1	3 channels	
	Baud-rate generator included	
DMA Controller (DMAC)	T	
Number of channels	4 channels	-
Data transfer path	Memory to memory, memory to peripheral, and perip	heral to memory
Transfer mode	Basic, ping-pong, scatter-gather	
DMA trigger source	UART3, SPIA, QSPI, I2C, T16B, ADC12A, and softwa	re
Clock generator (CLG)	IA (IOCC/OCC1/OCC2/FVOCC)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)	
System clock frequency (operating frequency)	V _{D1} voltage mode = mode0: 16.0MHz (max.)	
IOSC oscillator circuit (boot clock source)	Vbi voltage mode = mode1: 1.8MHz (max.) Vbi voltage mode = mode0: 8/2/1MHz (typ.) software	coloctable
105C oscillator circuit (boot clock source)	V _{D1} voltage mode = mode0: 8/2/1MHz (typ.) software V _{D1} voltage mode = mode1: 1.9/0.9 MHz (typ.) software	
	10 µs (max.) starting time (time from cancelation of S	
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator	SELEF State to vector table
OSCI OSCINATOR CIRCUIT	32kHz (typ.) embedded oscillator	
	Oscillation stop detection circuit included	
OSC3 oscillator circuit	16 MHz (max.) crystal/ceramic oscillator	
	16/8/4MHz(typ) embedded oscillator	16/8/4MHz(typ) embedded
	(-11-)	oscillator(8/4MHz:divie16MHz)
		±1%@Ta=0~85℃
EXOSC clock input	16 MHz (max.) square or sine wave input	
Other	Configurable system clock division ratio	
	Configurable system clock used at wake up from SLEE	
-/- / ()	Operating clock frequency for the CPU and all periphe	ral circuits is selectable.
I/O port (PPORT)		Tayloon is an interest to
Number of general-purpose I/O ports	PKG48pin: 39bit(max.)	PKG32pin: 25bit(max.)
	PKG64pin: 55bit(max.)	PKG48pin: 39bit(max.) PKG64pin: 55bit(max.)
	PKG80pin: 71bit(max.)	rkgo-piii . 55bit(iiiax.)
	PKG100pin: 91bit (max.)	
	Pins are shared with the peripheral I/O.	
Number of input interrupt ports		PKG32pin: 21bit(max.)
	PKG48pin: 33bit(max.)	PKG48pin: 35bit(max.) PKG64pin: 51bit(max.)
	PKG64pin: 49bit(max.) PKG80pin: 65bit(max.)	PKG64pin: 51bit(max.)
	PKG100pin: 85bit (max.)	
Number of ports that support universal port	. , ,	PKG32pin: 9bit(max.)
multiplexer (UPMUX)	PKG48pin: 16bit(max.)	PKG48pin: 20bit(max.)
, ,	PKG64pin: 24bit(max.)	PKG64pin: 32bit(max.)
	PKG80pin: 27bit(max.)	
	PKG100pin: 32bit (max.)	be reciprocal to reciprocat
T1	A peripheral circuit I/O function selected via software	can be assigned to each port.
Timers Watchdog timer (WDT2)	Congratos NMI or watchdog timor roset	
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.	
Watchdog timer (WDT2)	Programmable NMI/reset generation cycle	no week/month/year counters
	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the	
Watchdog timer (WDT2)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of th Theoretical regulation function for 1-second correction	
Watchdog timer (WDT2) Real-time clock (RTCA)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of th Theoretical regulation function for 1-second correction Alarm and stopwatch functions	
Watchdog timer (WDT2) Real-time clock (RTCA)	Programmable NMI/reset generation cycle 128-1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels	1
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of th Theoretical regulation function for 1-second correction Alarm and stopwatch functions	1
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alarm and Stopwatch functions	1
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alachannels 2 channels	1
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alachanels Event counter/capture function	ADC12A operating clock/
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16) 16-bit PWM timer (T16B)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alachanels Event counter/capture function PWM waveform generation function	ADC12A operating clock/
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16) 16-bit PWM timer (T16B)	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alachanels Event counter/capture function PWM waveform generation function	ADC12A operating clock/
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16) 16-bit PWM timer (T16B) 12-bit A/D converter (ADC12A) Conversion method Resolution	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alarm counter/capture function PWM waveform generation function Number of PWM output or capture input ports: 4 por Successive approximation type 12 bits	ADC12A operating clock/
Watchdog timer (WDT2) Real-time clock (RTCA) 16-bit timer (T16) 16-bit PWM timer (T16B) 12-bit A/D converter (ADC12A) Conversion method	Programmable NMI/reset generation cycle 128–1 Hz counter, second/minute/hour/day/day of the Theoretical regulation function for 1-second correction Alarm and stopwatch functions 8 channels Generates the SPIA and QSPI master clocks, and the Alarm counter/capture function PWM waveform generation function Number of PWM output or capture input ports: 4 por Successive approximation type	ADC12A operating clock/

Model	S1C31D50 S1C31D51	S1C31D41
Supply voltage detector (SVD3)	31031030 31031031	31031041
Number of channels	1 channel	
Detection voltage	VDD or an external voltage (2 external detection ports a	re available.)
Detection level	V _{DD} : 28 levels (1.8 to 5.0 V)/external voltage: 32 levels	
Other	Intermittent operation mode	
	Generates an interrupt or reset according to the detect	ion level evaluation.
Temperature sensor/reference voltage gene		
Temperature sensor circuit		Sensor output can be
	-	measured using ADC12A.
Reference voltage generator	-	Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, VDD, and external input.
R/F converter (RFC)		
Conversion method	CR oscillation type 24-bit counters	
Number of conversion channels	1 channel	
Supported sensors	DC bias resistive sensors	
IR remote controller (REMC3)		
Number of transmitter channels	1 channel	
Other	EL lamp drive waveform can be generated (by the hard	lware) for an application ex-
	ample.	
Decet	Output inversion function	
Reset	Descharbe when the week win is set to less	
#RESET pin Power-on reset	Reset when the reset pin is set to low.	
	Reset at power on.	< 1.4F \/ (typ.) is detected)
Brown-out reset	Reset when the power supply voltage drops (when VDD	
Watchdog timer reset Supply voltage detector reset	Reset when the watchdog timer overflows (can be enal	
Interrupt	Reset when the supply voltage detector detects the set	voltage level (can be enabled)
Non-maskable interrupt	Courteres (Doost NIMI HandFoult CVCall DandCV CusTis)	
	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTic)	
Programmable interrupt	External interrupt: 3 systems	
Power supply voltage	Internal interrupt: 27 systems	
VDD operating voltage	1.8 to 5.5 V * If VDD > 3.6 V, the V _{D1} voltage mode i	must be mode0
V _{DD} operating voltage for Flash programming	$2.4 \sim 5.5 \text{ V}$	2.2 ~ 5.5 V
SPI-Flash interface power supply VDDQSPI	3.0 to 3.6V(possible to set main VDD:5v, SPI-Flash pov	
Operating temperature	3.0 to 3.0 (possible to set main VDD.5V, 3F1-1 lash pov	ver supply .5.5v)
Operating temperature range	-40 to 85 °C	
Current consumption (Typ. value)	+0 to 05 C	
current consumption (Typ. value)	IOSC = OFF, OSC1 = OFF, OSC3 = OFF	
	0.46 µA	0.34 μΑ
SLEEP mode *2	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OS	
	0.95 μΑ	0.9 μΑ
HALT mode *3	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OS	
TIALI Mode 5	1.8 µA	1.5 μΑ
	V _{D1} voltage mode = mode0, CPU = OSC3 (16MHz)	
	243 µA/MHz	215 μA/MHz
RUN mode	V _{D1} voltage mode = mode1, CPU = IOSC (2MHz)	
	155 μA/MHz	130 μA/MHz
Shipping form *4	1 200 pry 1 112	200 pry 1 11 12
Cimpping form 4		P-TQFP032-0707-0.80
1	-	(7mm x 7mm, 0.8mm pitch)
	P-TOFP048-0707-0.50	(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
2	(7mm x 7mm, 0.5mm pite	ch)
	P-LOFP064-1010-0.50	GII <i>j</i>
3	(10mm x 10mm, 0.5mm pi	itch)
	P-TOFP080-1212-0.50	icen)
4	(12mm x 12mm, 0.5mm pitch)	-
_	P-LQFP100-1414-0.50	<u> </u>
5	(14mm x 14mm, 0.5mm pitch)	-
[(2 x 2 piccii)	1

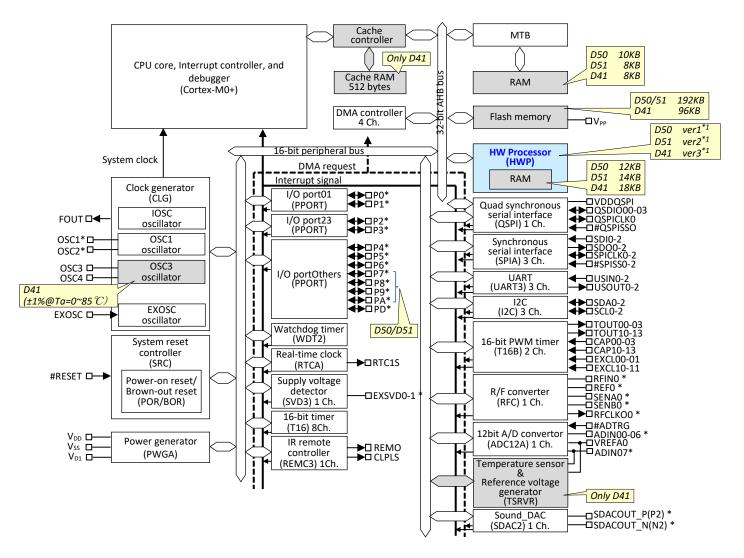
^{*1} The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.

^{*2} SLEEP mode refers to deep sleep mode in the Cortex\$-M0+ processor.

^{*3} HALT mode refers to sleep mode in the Cortex\$-M0+ processor.

^{*4} Shown in parentheses are JEITA package names.

Block Diagram



^{*} The pin configuration depends on the package. For detailed information, refer to Section "Pins."

*1 HW Processor Specification

Sound Play Function

Journa i it	.,									
Model	HWP	2ch	Multi-	Volume	Repeat	Voice Speed	Gapless	Buzzer	Voice Pitch	Tone
Model	version	Sound Play	SoundROM	Setting	Setting	Conversion	Play	Voice/Melody	Conversion	Generation
S1C31D50	1.00					√(ver1.00)	-	-	-	-
S1C31D51	2.00	~	V	~	~	((,,,,,2,00)	,	,	-	-
S1C31D41	3.00					∨(ver2.00)	V	V	V	V

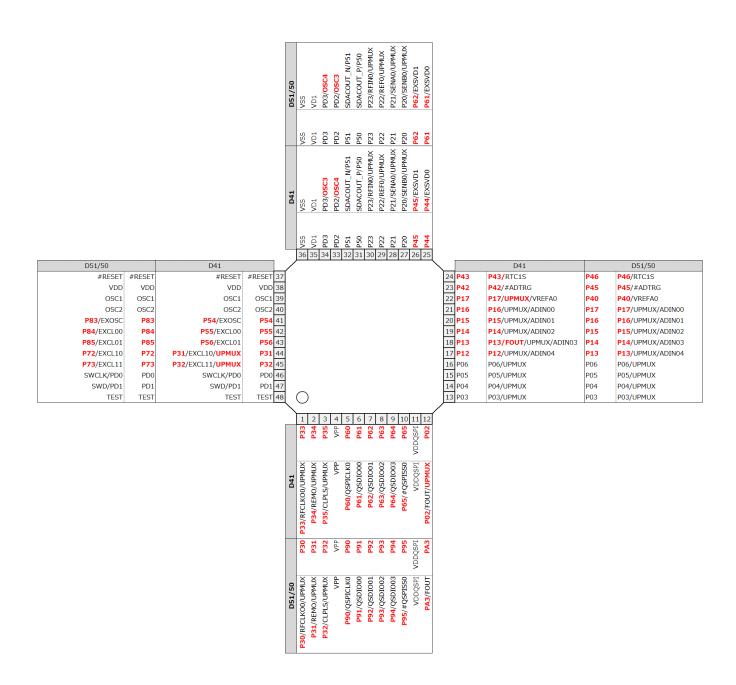
Memory Check Function

, ,								
Madal	HWP	Embedd	ed Flash	External	Embedded RAM			
Model	version	CRC	Checksum	CRC	Checksum	March-C	R/W Check	
S1C31D50	1.00							
S1C31D51	2.00	~	V	V	~	~	V	
S1C31D41	3.00							

■ Pin Configuration Diagram
P-TQFP032-0707-0.80(32pin, 7mm x 7mm, 0.8mm pitch)
✓ S1C31D41

	VSS VSS	VD1 VD1	PD3 PD3/OSC3	PD2 PD2/OSC4	P51 SDACOUT_N/P51	P50 SDACOUT_P/P50	P20 P20/SENBO/UPMUX	P44 P44/EXSVD0				
					20			17				
)-1	20	22	21	20	10	10	11				
#RESET #RESET 25									16	P	43	P43/RTC1S
VDD VDD 26									15	PΖ	42	P42/#ADTRG
P54/EXOSC P54 27									14	P1	17	P17/UPMUX/VREFA
P31/EXCL10/UPMUX P31 28									13	P1	16	P16/UPMUX/ADIN00
P32/EXCL11/UPMUX P32 29									12	P1	15	P15/UPMUX/ADIN01
SWCLK/PD0 PD0 30									11	P1	14	P14/UPMUX/ADIN02
SWD/PD1 PD1 31									10	P1		P13/FOUT/UPMUX/ADIN03
TEST TEST 32	\bigcirc								9	P1	12	P12/UPMUX/ADIN4
	$\widetilde{}$											
	1	2	3	4	5	6	7	8				
	VPP	P60	P61	P62	P63	P64	P65	VDDQSPI				
	VPP	LK0	000	301	302	203	SS 0	SPI				
		P60/QSPICLK0	P61/QSDIO00	P62/QSDI001	P63/QSDI002	P64/QSDIO03	P65/#QSPISS0	VDDQSPI				
		/QS	1/08	2/05	3/09	30/t	/#Q	>				
		P60,	P61	P62	P63	ъ62	965/					
							_					

P-TQFP048-0707-0.50(48pin, 7mm x 7mm, 0.5mm pitch) ✓ S1C31D51/50/41



Note) Basically, Pin Compatible for D50/D51/D41 is achievable, if software deal with Port Pins differential.

Red Pins: differential between D50/D51 and D41.

P-LQFP064-1010-0.50(64pin, 10mm x 10mm, 0.5mm pitch) ✓ S1C31D51/50/41

P51/50	P21 P21/SENA0/UPMUX P20 P20/SENB0/UPMUX	P62 P62/EXSVD1
VSS V01 V01 V01 PD3 PD2 PD2 PS1 PS1 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2		
VSS V01 V01 V01 PD3 PD2 PD2 PS1 PS1 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2 PS2		
×	P21 P20	962
/P51 /P50 /P50		
	MUX	
SC3 SC4 N T D UT P, WUX WHUX WHUX WHUX WHUX FO/UF FO/UF	P21/SENA0/UPMUX P20/SENB0/UPMUX	SVD1
D41 VSS VD1 PD3/OSC3 PD2/OSC4 PD2/OSC4 PD2/OSC4 PD2/UPMUX P25/UPMUX P25/UPMUX P24/UPMUX	P21/SE P20/SE	P45/EXSVD1
VSS VD1 PD3 PD2 P51 P50 P27 P26 P26 P27 P28 P28		P45
48 47 46 45 44 43 42 41 40 39 38 37	36 35	34 3

	D41		l .
#RESET	#RESET	#RESET	49
VDD	VDD	VDD	50
OSC1	OSC1	OSC1	51
OSC2	OSC2	OSC2	52
P81	P52	P52	53
P82	P53	P53	54
P83	P54/EXOSC	P54	55
P84	P55/EXCL00	P55	56
P85	P56/EXCL01	P56	57
P70	P07/UPMUX	P07	58
P71	P30/UPMUX	P30	59
P72	P31/EXCL10/UPMUX	P31	60
P73	P32/EXCL11/UPMUX	P32	61
PD0	SWCLK/PD0	PD0	62
PD1	SWD/PD1	PD1	63
TEST	TEST	TEST	64
	VDD OSC1 OSC2 P81 P82 P83 P84 P85 P70 P71 P72 P73 PD0 PD1	#RESET #RESET VDD VDD OSC1 OSC1 OSC2 OSC2 P81 P52 P82 P53 P83 P54/EXOSC P84 P55/EXCIO1 P70 P07/UPMUX P71 P30/UPMUX P72 P31/EXCI.01/UPMUX P73 P32/EXCI.11/UPMUX PD0 SWCI.K/PD0 PD1 SWD/PD1	#RESET #RESET #RESET VDD VDD VDD OSC1 OSC1 OSC1 OSC2 OSC2 OSC2 P81 P52 P53 P83 P54/EXOSC P54 P84 P55/EXCL00 P55 P85 P56/EXCL01 P56 P70 P07/UPMUX P07 P71 P30/UPMUX P30 P72 P31/EXCL10/UPMUX P31 P73 P32/EXCL11/UPMUX P32 PD0 SWCLK/PD0 PD0 PD1 SWD/PD1 PD1

		D41		F51/50
32	P43	P43/RTC1S	P46	P46/RTC1S
31	P42	P42/#ADTRG	P45	P45/#ADTRG
30	P41	P41	P44	P44
29	P40	P40	P43	P43
28	P17	P17/UPMUX/VREFA	P40	P40/VREFA
27	P16	P16/UPMUX/ADIN00	P17	P17/UPMUX/ADIN00
26	P15	P15/UPMUX/ADIN01	P16	P16/UPMUX/ADIN01
25	P14	P14/UPMUX/ADIN02	P15	P15/UPMUX/ADIN02
24	P13	P13/FOUT/UPMUX/ADIN03	P14	P14/UPMUX/ADIN03
23	P12	P12/UPMUX/ADIN04	P13	P13/UPMUX/ADIN04
22	P11	P11/UPMUX/ADIN05	P12	P12/UPMUX/ADIN05
21	P10	P10/UPMUX/ADIN06	P11	P11/UPMUX/ADIN06
20	P06	P06/SDACOUT_N2/UPMUX	P06	P06/UPMUX
19	P05	P05/SDACOUT_N/UPMUX	P05	P05/UPMUX
18	P04	P04/SDACOUT_P/UPMUX	P04	P04/UPMUX
17	P03	P03/SDACOUT_P2/UPMUX	P03	P03/UPMUX

	1	2	3	4	5	6	7	8	9	10 ლ	11	12	13	14	15	16
	P33	P34	P35	P36	P37	VPP	P60	P61	P62	P63	P64	P65	VDDQSPI	P00	P01	P02
D41	P33/RFCLKO0/UPMUX	P34/REMO/UPMUX	P35/CLPLS/UPMUX	P36/UPMUX	NUMUX P37/UPMUX	ddΛ	P60/QSPICLK0	P61/QSDI000	P62/QSDI001	P63/QSDI002	P64/QSDI003	P65/#QSPISS0	VDDQSPI	POO/UPMUX	PO1/UPMUX	P02/FOUT/UPMUX
	P30	P31	P32	P33	P34	VPP	P90	P91	P92	P93	P94	P95	VDDQSPI	PA1	PA2	PA3
DS1/50	P30/RFCLKO0/UPMUX	P31/REMO/UPMUX	P32/CLPLS/UPMUX	P33/UPMUX	P34/UPMUX	ΛPP	P90/QSPICLK0	P91/QSDI000	P92/QSDI001	P93/QSDI002	P94/QSDI003	P95/#QSPISS0	VDDQSPI	PA1	PA2	PA3/FOUT

Note) Basically, Pin Compatible for D50/D51/D41 is achievable, if software deal with Port Pins differential.

Red Pins: differential between D50/D51 and D41.

P-TQFP080-1212-0.50(80pin, 12mm x 12mm, 0.5mm pitch)

✓ S1C31D51/50

#RESET	#RESET	61
VDD	VDD	62
OSC1	OSC1	63
OSC2	OSC2	64
P80	P80	65
P81	P81	66
P82	P82	67
P83/EXOSC	P83	68
P84/EXCL00	P84	69
P85/EXCL01	P85	70
P86	P86	71
P87	P87	72
P70	P70	73
P71	P71	74
P72/EXCL10	P72	75
P73/EXCL11	P73	76
P74	P74	77
SWCLK/PD0	PD0	78
SWD/PD1	PD1	79
TEST	TEST	80

40	P46	P46/RTC1S
39	P45	P45/#ADTRG
38	P44	P44
37	P43	P43
36	P42	P42
35	P41	P41
34	P40	P40/VREFA
33	P17	P17/UPMUX/ADIN00
32	P16	P16/UPMUX/ADIN01
31	P15	P15/UPMUX/ADIN02
30	P14	P14/UPMUX/ADIN03
29	P13	P13/UPMUX/ADIN04
28	P12	P12/UPMUX/ADIN05
27	P11	P11/UPMUX/ADIN06
26	P10	P10/UPMUX/ADIN07
25	P07	P07/UPMUX
24	P06	P06/UPMUX
23	P05	P05/UPMUX
22	P04	P04/UPMUX
21	P03	P03/UPMUX

1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	PD4	P30	P31	P32	P33	P34	P35	VPP	06d	P91	P92	P93	P94	P95	VDDQSPI	PA0	PA1	PA2	PA3	PA4
	PD4	P30/RFCLKO0/UPMUX	P31/REMO/UPMUX	P32/CLPLS/UPMUX	P33/UPMUX	P34/UPMUX	P35/UPMUX	VPP	P90/QSPICLK0	P91/QSDIO00	P92/QSDI001	P93/QSDIO02	P94/QSDIO03	P95/#QSPISS0	VDDQSPI	PA0	PA1	PA2	PA3/FOUT	PA4

P-LQFP100-1414-0.50(100pin, 14mm x 14mm, 0.5mm pitch) ✓ S1C31D51/50

VSS	VD1	PD3/0SC4	PD2/OSC3	P55	P54	P53	P52	SDACOUT_N/P51	SDACOUT_P/P50	P27/UPMUX	P26/UPMUX	P25/UPMUX	P24/UPMUX	P23/RFIN0/UPMUX	P22/REF0/UPMUX	P21/SENA0/UPMUX	P20/SENB0/UPMUX	P67	P66	P65	P64	P63	P62/EXSVD1	P61/EXSVD0
VSS	VD1	PD3	PD2	P55	P54	P53	P52	P51	P50	P27	P26	P25	P24	P23	P22	P21	P20	J-20	99d	P65	P64	P63	P62	P61
75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51

76	#RESET	#RESET
77	VDD	VDD
78	OSC1	OSC1
79	OSC2	OSC2
80	P56	P56
81	P57	P57
82	P80	P80
83	P81	P81
84	P82	P82
85	P83	P83/EXOSC
86	P84	P84/EXCL00
87	P85	P85/EXCL01
88	P86	P86
89	P87	P87
90	P70	P70
91	P71	P71
92	P72	P72/EXCL10
93	P73	P73/EXCL11
94	P74	P74
95	P75	P75
96	PD0	SWCLK/PD0
97	PD1	SWD/PD1
98	TEST	TEST
99	P76	P76
100	P77	P77

50	P60	P60
49	P47	P47
48	P46	P46/RTC1S
47	P45	P45/#ADTRG
46	P44	P44
45	P43	P43
44	P42	P42
43	P41	P41
42	P40	P40/VREFA
41	P17	P17/UPMUX/ADIN00
40	P16	P16/UPMUX/ADIN01
39	P15	P15/UPMUX/ADIN02
38	P14	P14/UPMUX/ADIN03
37	P13	P13/UPMUX/ADIN04
36	P12	P12/UPMUX/ADIN05
35	P11	P11/UPMUX/ADIN06
34	P10	P10/UPMUX/ADIN07
33	P07	P07/UPMUX
32	P06	P06/UPMUX
31	P05	P05/UPMUX
30	P04	P04/UPMUX
29	P03	P03/UPMUX
28	P02	P02/UPMUX
27	P01	P01/UPMUX
26	P00	P00/UPMUX

_																								
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
PD4	P30	P31	P31	P32	P33	P34	P35	P36	VPP	P37	P90	P91	P92	P93	P94	P95	VDDQSPI	PA0	PA1	PA2	PA3	PA4	PA5	PA6
PD4	P30/RFCLKO0/UPMUX	P31/REMO/UPMUX	P31/REMO/UPMUX	P32/CLPLS/UPMUX	NA3/UPMUX	P34/UPMUX	P35/UPMUX	P36/UPMUX	VPP	NUMU/784	P90/QSPICLK0	P91/QSDI000	P92/QSDI001	P93/QSDI002	P94/QSDIO03	P95/#QSPISS0	VDDQSPI	PA0	PA1	PA2	PA3/FOUT	PA4	PA5	PA6

■ Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

 $I/O: \hspace{1cm} I \hspace{1cm} = Input \\ O \hspace{1cm} = Output$

I/O = Input/Output
P = Power supply
A = Analog signal

Hi-Z = High impedance state

Initial state: I (Pull-up) = Input with pulled up

I (Pull-down) = Input with pulled down
Hi-Z = High impedance state
O (H) = High level output

O (L) = Low level output

Tolerant fail-safe structure:

Over voltage tolerant fail-safe type I/O cell included

Red Pins: differential between D50/D51 and D41.

				_			D41			D51	/50	
Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
VDD	VDD	Р	-	-	Power(+)	<i>∨</i>	V	<i>∨</i>	V	V	V	V
VSS	VSS	Р	-	-	GND	V	V	<i>∨</i>	V	V	V	~
VPP	VPP	Р	-	-	Flash Programing Power	V	V	<i>∨</i>	V	V	V	~
VD1	VD1	Α	-	-	VD1 Regulator output	V	V	~	>	V	>	V
VDDQSPI	VDDQSPI	Р	-	-	QSPI Interface/ P9 Port group power Supply(D50/51)/ P6 Port group power Supply (D41)	V	V	<i>\</i>	<i>></i>	<i>\</i>	<i>></i>	>
OSC1	OSC1	Α	-	-	OSC1 oscillator input	-	V	<i>∨</i>	V	V	V	<i>∨</i>
OSC2	OSC2	Α	-	-	OSC1 oscillator output	-	V	<i>∨</i>	V	V	V	V
TEST	TEST	I	I(Pull-down)	-	Test mode enable	V	V	V	V	V	V	V
#RESET	#RESET	I	I(Pull-up)	-	Reset input	V	V	<i>∨</i>	V	V	V	<i>∨</i>
P00	P00	I/O		,	I/O port			,				,
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	-	-	~
P01	P01	I/O		,	I/O port			,				,
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	-	-	~
P02	P02	I/O		,	I/O port							,
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	~	~	-	-	-	~
P03	P03	I/O			I/O port				V	V	V	V
	SDACOUT_P2 <u>D41</u>	0	Hi-Z	~	Buzzer sound DAC positive output 2	-	V	V	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				V	V	V	~
P04	P04	I/O			I/O port				V	V	V	<i>∨</i>
	SDACOUT_P <u>D41</u>	0	Hi-Z	V	Buzzer sound DAC positive output 1	-	V	~	1	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				V	~	V	~
P05	P05	I/O			I/O port				V	V	V	<i>∨</i>
	SDACOUT_N <u>D41</u>	0	Hi-Z	V	Buzzer sound DAC nagetive output 1	-	V	~	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				V	V	V	V
P06	P06	I/O			I/O port				V	V	V	V
	SDACOUT_N2 <u>D41</u>	0	Hi-Z	~	Buzzer sound DAC nagetive output 2	-	V	V	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				~	V	V	V
P07	P07	I/O	11: 7		I/O port			.,			.,	.,
	UPMUX	I/O	Hi-Z	~	User-selected I/O(universal port multiplexer)	-	-	~	-	-	/ V V V V V V V V V V V V V V V V V V V	~

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					Tolerant			D41			D51	/50	
Pin name	Pin func	tion	I/O	Initial	fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
P10	P10		I/O			I/O port		_	V			V	<i>V</i>
	UPMUX		I/O	Hi-Z		User-selected I/O(universal port multiplexer)	1	-	V			>	V
	ADIN06	<u>D41</u>	Α	HI-Z	-	12-bit A/D converter Ch.0 analog signal input6	1	-	V	ı	1	-	-
	ADIN07	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input7	-	-	1	-		V	V
P11	P11		I/O			I/O port		-	~		~	~	V
	UPMUX		I/O	Hi-Z		User-selected I/O(universal port multiplexer)		_	V		V	V	V
	ADIN05	D41	Α	пі-∠	-	12-bit A/D converter Ch.0 analog signal input5	ı	-	V	1	-	1	-
	ADIN06	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input6	-	-	-	-	V	V	V
P12	P12		I/O			I/O port	>	~	<	ı	>	>	V
	UPMUX		I/O	Hi-Z		User-selected I/O(universal port multiplexer)	>	V	V	ı	>	>	V
	ADIN04	D41	Α	пі-∠	-	12-bit A/D converter Ch.0 analog signal input4	>	V	V	ı	1	ı	-
	ADIN05	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input5	ı	-	1	ı	>	>	V
P13	P13		I/O			I/O port				V	V	V	V
	FOUT	<u>D41</u>	0			Clock external output	V	V	~	-	1	-	-
	UPMUX		I/O	Hi-Z	-	User-selected I/O(universal port multiplexer)				V	V	V	V
	ADIN03	D41	Α			12-bit A/D converter Ch.0 analog signal input3	V	V	V	-	-	-	-
	ADIN04	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input4	-	-	-	V	V	V	V
P14	P14		I/O			I/O port	V	~	_	~	<i>\</i>	V	V
	UPMUX		I/O	7		User-selected I/O(universal port multiplexer)	V	\ \	V	V	V	V	V
	ADIN02	D41	Α	Hi-Z	-	12-bit A/D converter Ch.0 analog signal input2	V	V	~	-	1	-	-
	ADIN03	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input3	-	-	1	V	V	V	V
P15	P15		I/O			I/O port	V	~	~	~	~	V	~
	UPMUX		I/O	Hi-Z		User-selected I/O(universal port multiplexer)	V	\ \	V	V	V	V	V
	ADIN01	D41	Α	пі-∠	-	12-bit A/D converter Ch.0 analog signal input1	V	~	<	-	1	-	-
	ADIN02	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input2	-	-	1	>	V	V	V
P16	P16		I/O			I/O port	~	~	~	~	~	V	V
	UPMUX		I/O	Hi-Z		User-selected I/O(universal port multiplexer)	>	V	V	>	V	V	V
	ADIN00	D41	Α	пі-∠	-	12-bit A/D converter Ch.0 analog signal input0	>	V	V	ı	1	ı	-
	ADIN01	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input1	-	-	1	>	<	V	V
P17	P17		I/O			I/O port	<i>V</i>	~	V	V	V	V	V
	UPMUX		I/O			User-selected I/O(universal port multiplexer)					V		
	VREFA0	D41	Α	Hi-Z	-	12-bit A/D converter Ch.0 reference voltage input	V	V	~	-	-	-	-
	ADIN00	D50/D51	Α			12-bit A/D converter Ch.0 analog signal input0	-	-	-	>	V	>	V

				Tolerant			D41			D51	/50	
Pin name	Pin function	I/O	Initial	fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
P20	P20	I/O			I/O port							
	SENB0	Α	Hi-Z	V	R/F converter Ch.0 sensor B oscillator pin	V	V	V	V	V	V	V
	UPMUX	I/O			User-selected I/O(universal port multiplexer)							
P21	P21	I/O			I/O port							
	SENA0	Α	Hi-Z	~	R/F converter Ch.0 sensor A oscillator pin	-	V	V	V	V	V	~
	UPMUX	I/O			User-selected I/O(universal port multiplexer)							
P22	P22	I/O			I/O port							
	REF0	Α	Hi-Z	~	R/F converter Ch.0 reference oscillator pin	-	V	V	V	~	V	V
	UPMUX	I/O			User-selected I/O(universal port multiplexer)							
P23	P23	I/O			I/O port							
	RFIN0	Α	Hi-Z	V	R/F converter Ch.0 oscillation input	-	V	V	V	~	V	~
	UPMUX	I/O			User-selected I/O(universal port multiplexer)							
P24	P24	I/O			I/O port							
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	~	V	~
P25	P25	I/O			I/O port							
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	~	V	~
P26	P26	I/O			I/O port							
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	V	-	~	V	~
P27	P27	I/O			I/O port							
	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	~	V	~
P30	P30	I/O			I/O port	-	-	V				
	RFCLKO0 D50/D51	0	Hi-Z	V	R/F converter Ch.0 clock monitor output	-	-	1	V	V	V	V
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	-	-	V				
P31	P31	I/O			I/O port	V	V	V	V	V	V	~
	EXCL10 D41	I			16-bit PWM timer Ch.1 event counter input 0	V	V	V	-	-	-	-
	REMO <u>D50/D51</u>	0	Hi-Z	V	IR remote controller transmit data output	-	-	-	V	V	V	~
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	~	V	V	V	V	V	V
P32	P32	I/O			I/O port	V	V	V	V	V	V	V
	EXCL11 D41	I			16-bit PWM timer Ch.1 event counter input 1	V	V	V	-	-	-	-
	CLPLS D50/D51	0	Hi-Z	V	IR remote controller clear pulse output	-	-	-	V	V	V	~
	UPMUX	I/O			User-selected I/O(universal port multiplexer)	V	V	V	V	V	V	V
P33	P33	I/O			I/O port				-	V	V	V
	RFCLKO0 <u>D41</u>		Hi-Z	V	R/F converter Ch.0 clock monitor output	-	V	V	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				-	V	V	V
P34	P34	I/O			I/O port				-	V	V	V
	REMO D41	0	Hi-Z	V	IR remote controller transmit data output	_	V	V	-	-	-	-
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				-	V	V	V
P35	P35	I/O			I/O port				-	-	V	V
1 -	CLPLS D41	0	Hi-Z	~	IR remote controller clear pulse output	_	~	~		-	-	_
	UPMUX	I/O			User-selected I/O(universal port multiplexer)				-	-	V	V
P36	P36	I/O			I/O port							\vdash
. 50	UPMUX	I/O	Hi-Z	V	User-selected I/O(universal port multiplexer)	-	-	~	-	-	-	~
P37	P37	I/O	Hi-Z	V	I/O port							
	UPMUX	I/O	111.4	<u> </u>	User-selected I/O(universal port multiplexer)	-	-	V	-	-	-	V

					Tolerant			D41			D51	/50	
Pin name	Pin fur	nction	I/O	Initial	fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
P40	P40		I/O			I/O port	-	-	V				
	VREFA	D50/D51	А	Hi-Z	-	12-bit A/D converter Ch.0 reference voltage input	-	-	-	V	V	V	~
P41	P41		I/O	Hi-Z	V	I/O port	-	-	V	ı	-	<i>∨</i>	~
P42	P42		I/O	Hi-Z	✓*1	I/O port	>	~	~	1	1	<	V
	#ADTRG0	D41	I	1111 2	, 1	12-bit A/D converter Ch.0 trigger input	Ů	Ľ	Ť	-	-	-	-
P43	P43		I/O	Hi-Z	✓*1	I/O port	~	\ \	_	-	<i>∨</i>	V	~
	RTC1S	D41	0		-	Real-time clock 1-second cycle pulse output		Ь		-	-	-	-
P44	P44		I/O	Hi-Z	V	I/O port	V	~	~	-	V	V	~
	EXSVD0	D41	Α	пі-2		Supply voltage detector external voltage detection input 0	V	ľ	_	-	-	-	-
P45	P45	·	I/O			I/O port							
	EXSVD1	D41	Α	Hi-Z	V	Supply voltage detector external voltage detection input 1	-	~	~	V	~	~	~
	#ADTRG0	D50/D51	I			12-bit A/D converter Ch.0 trigger input	_	-	_				
P46	P46		I/O			I/O port							
	RTC1S	D50/D51	0	Hi-Z	V	Real-time clock 1-second cycle pulse output	-	-	-	V	V	V	~
P47	P47	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	~
P50	SDACOUT_P		0			Sound DAC positive output							
	P50		I/O	O(L)	V	I/O port	~	~	~	~	<i>∨</i>	~	~
P51	SDACOUT_N		0			Sound DAC negative output							
	P51		I/O	O(L)	V	I/O port	~	~	~	~	V	~	~
P52	P52		I/O	Hi-Z	V	I/O port	-	-	V	-	-	V	V
P53	P53		I/O	Hi-Z	V	I/O port	-	-	V	-	-	V	V
P54	P54		I/O			I/O port				-	-	-	V
	EXOSC	D41	I	Hi-Z	V	Clock generator external clock input	V	~	~	-	-	-	-
P55	P55	•	I/O	7	,	I/O port		,	,	-	-	-	~
	EXCL00	D41	I	Hi-Z	V	16-bit PWM timer Ch.0 event counter input 0	-	~	~	-	-	-	-
P56	P56		I/O	11: 7	V	I/O port		_	V	-	-	-	V
	EXCL01	D41	I	Hi-Z	V	16-bit PWM timer Ch.0 event counter input 1	•	V	V	-	-	-	-
P57	P57	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	~
P60	P60		I/O			I/O port				-	-	-	~
	QSPICLK0	D41	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 clock input/output	~	~	~	-	-	-	-
P61	P61	•	I/O			I/O port				~	V	V	~
	QSDIO00	D41	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data	~	V	V	-	1	-	-
	EXSVD0	D50/D51	Α	пі-2	V	input/output Supply voltage detector external voltage	-	-	-	<i>V</i>	V	<i>V</i>	V
262		200,201	7.10			detection input 0							
P62	P62		I/O			I/O port Quad synchronous serial interface Ch.0 data	~	V	V	V	V	V	V
	QSDIO01	D41	I/O	Hi-Z	~	input/output				-	-	-	_
	EXSVD1	D50/D51	Α			Supply voltage detector external voltage detection input 1	-	-	-	~	V	~	V
P63	P63	1	I/O			I/O port				-	-	~	<i>∨</i>
	QSDIO02	D41	I/O	Hi-Z	~	Quad synchronous serial interface Ch.0 data input/output	V	~	V	-	-	-	-
P64	P64		I/O			I/O port		\vdash		-	-	V	V
		D41	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data	V	V	V	_	_	_	_
	QSDIO03	D41	,			input/output		<u> </u>					
P65	P65		I/O	Hi-Z	V	I/O port	V	~	V		-	-	~
	#QSDISS0	D41	I/O	ı⊐ ! -∠		Quad synchronous serial interface Ch.0 slave- select input/output	ľ	ľ	ľ	-	-	-	3
P66	P66	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	V
P67	P67	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	V

^{* 1 :} D41 unsupported

					Tolerant			D41			D51	/50	
Pin name	Pin func	tion	I/O	Initial	fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
P70	P70	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	V	V	V
P71	P71	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	V	V	V
P72	P72	D50/D51	I/O	11: 7	,	I/O port	-	-	-	,	,	,	
	EXCL10	D50/D51	I	Hi-Z	V	16-bit PWM timer Ch.1 event counter input 0	-	-	1	V	V	V	~
P73	P73	252/254	I/O	11: 7	,	I/O port	-	-	-	<i>V</i>	,	V	~
	EXCL11	D50/D51	I	Hi-Z	V	16-bit PWM timer Ch.1 event counter input 1	1	-	1	V	<i>∨</i>	V	V
P74	P74	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	V	V
P75	P75	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	V
P76	P76	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	V
P77	P77	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-		-	-	V
P80	P80	D50/D51	I/O	Hi-Z	V	I/O port	1	-	-	-	-	V	V
P81	P81	D50/D51	I/O	Hi-Z	~	I/O port	-	-	1		V	V	V
P82	P82	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	V	V	V
P83	P83	D50/D51	I/O	11: 7	V	I/O port	-	-	-	ζ	V	V	~
	EXOSC	<u>D50/D51</u>	I	Hi-Z		Clock generator external clock input	-	-	-	V	V	V	V
P84	P84	252/254	I/O	11: 7	V	I/O port	-	-	-	V	,	V	V
	EXCL00	D50/D51	I	Hi-Z		16-bit PWM timer Ch.0 event counter input 0	-	-	-	V	V	V	V
P85	P85	252/254	I/O	11: 7	V	I/O port	-	-	-	,	<i>V</i>	V	
	EXCL01	D50/D51	I	Hi-Z		16-bit PWM timer Ch.0 event counter input 1	-	-	-	V	V	V	~
P86	P86	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	V	V
P87	P87	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	V	V
P90	P90		I/O			I/O port	-	-	-				
	QSPICLK0	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 clock input/output	-	-	-	~	>	>	V
P91	P91		I/O			I/O port	-	-	1				
	QSDIO00	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data input/output	-	-	-	~	~	~	V
P92	P92		I/O			I/O port	-	-	-				
	QSDIO01	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data input/output	-	-	-	<i>\</i>	>	>	<i>∨</i>
P93	P93		I/O			I/O port	1	-	1				
	QSDIO02	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data input/output	-	-	-	V	<i>∨</i>	<i>V</i>	V
P94	P94		I/O			I/O port	-	-	-				
	QSDIO03	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 data input/output	-	-	-	~	~	<i>\</i>	V
P95	P95		I/O			I/O port	-	-	-				
	#QSPISS0	D50/D51	I/O	Hi-Z	V	Quad synchronous serial interface Ch.0 slave- select input/output	-	-	-	V	~	<i>V</i>	V

					Tolerant			D41			D51	/50	
Pin name	Pin function	n	I/O	Initial	fail-safe structure	Description	32pin	48pin	64pin	48pin	64pin	80pin	100pin
PA0	PA0	D50/D51	I/O	Hi-Z	V	I/O port	-	-	1	ī	-	V	V
PA1	PA1	D50/D51	I/O	Hi-Z	V	I/O port	1	1	1	1	V	V	V
PA2	PA2	D50/D51	I/O	Hi-Z	V	I/O port	1	1	1	-	V	V	V
PA3	PA3	D50/D51	I/O	Hi-Z	~	I/O port		-	-	<	~	ζ	_
	FOUT	<u>D30/D31</u>	0	HI-Z	V	Clock external output	,	1	1	V	V	V	V
PA4	PA4	D50/D51	I/O	Hi-Z	V	I/O port	1	1	1	1		V	V
PA5	PA5	D50/D51	I/O	Hi-Z	V	I/O port	-	1	-	1		1	V
PA6	PA6	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	-	V
PD0	SWCLK		I	T (Dull up)	V	Serial-wire debugger clock input	~	<i>V</i>	~	~	~	~	_
	PD0		I/O	I (Pull-up)		I/O port	V	V	V	V	V	V	V
PD1	SWD		I/O	I (Pull-up)	V	Serial-wire debugger data input/output	~	<	<	<	\ \	<	V
	PD1		I/O	I (Pull-up)	V	I/O port	V	V	V	V	V	V	Ľ
PD2	PD2		I/O			I/O port	V	V	V	>	V	V	~
	OSC4	D41	Α	Hi-Z	-	OSC3 oscillator circuit output	>	V	>	-	-	-	-
	OSC3	D50/D51	Α			OSC3 oscillator circuit input	-	-	-	V	V	V	V
PD3	PD3		I/O			I/O port	>	V	V	V	V	V	V
	OSC3	D41	Α	Hi-Z	-	OSC3 oscillator circuit input	V	V	V	-	-	-	-
	OSC4	D50/D51	Α			OSC3 oscillator circuit output	-	-	-	V	V	V	V
PD4	PD4	D50/D51	I/O	Hi-Z	V	I/O port	-	-	-	-	-	V	V
PD5	PD5	D50/D51	I/O	Hi-Z	V	I/O port	-	1	1	-	-	-	~

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

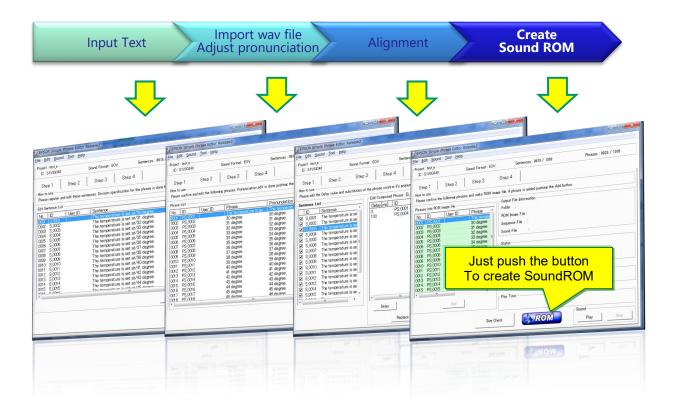
Peripheral circuit	Signal to be assigned	I/O	Channel number n	Function
I ² C	SCLn	I/O	n=0~2	I2C Ch.n clock input/output
(I2C)	SDAn	I/O	11=0/~2	I2C Ch.n data input/output
UART	USINn	I	- 0 3	UART3 Ch.n data input
(UART3)	USOUTn	0	n=0~2	UART3 Ch.n data output
Synchronous serial interface (SPIA)	SDIn	I	n=0~2	SPIA Ch.n data input
	SDOn	0		SPIA Ch.n data output
	SPICLKn	I/O		SPIA Ch.n clock input/output
	#SPISSn	I		SPIA Ch.n slave-select input
16-bit PWM timer (T16B)	TOUTn0/CAPn0	I/O	n=0,1	T16B Ch.n PWM output/capture input 0
	TOUTn1/CAPn1	I/O		T16B Ch.n PWM output/capture input 1
	TOUTn2/CAPn2	I/O		T16B Ch.n PWM output/capture input 2
	TOUTn3/CAPn3	I/O		T16B Ch.n PWM output/capture input 3

Note) Do not assign a function to two or more pins simultaneously.

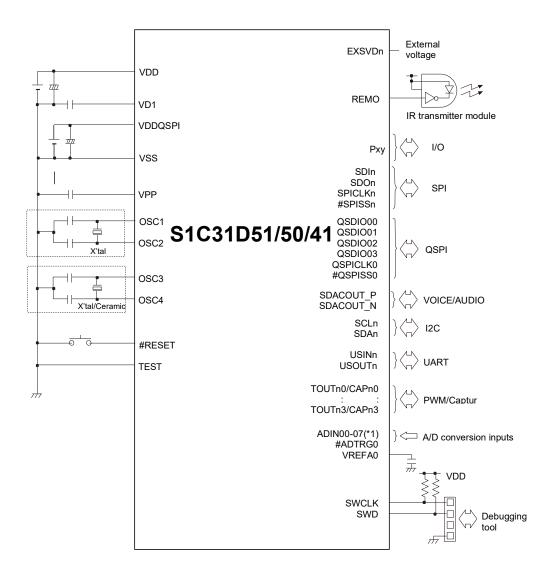
■ EPSON Voice Creation PC Tool

EPSON Voice creation PC tool makes voice related development easy because of no-studio recording, no narrator arrangement. This tool supports languages in the table below (all female voice), and easily creation, modification can be done, by "wav file" import function, existing wav file can be used.

Asia	America	Europe
Chinese	American English	British English
Korean	American Spanish	German
Japanese	Canadian French	French
_	_	Spanish
_	_	Italian
_	_	Russian



■ Basic External Connection Diagram

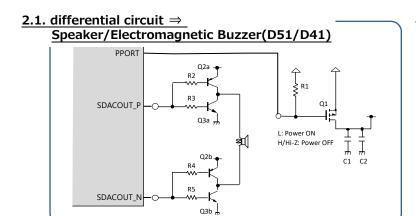


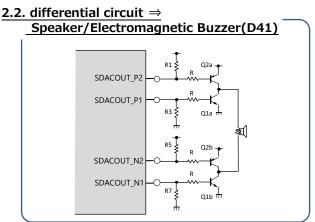
^{*1)} S1C31D41 ADIN07 is connected internal TSRVR signal.

■ Basic Speaker/Buzzer External Connection Diagram

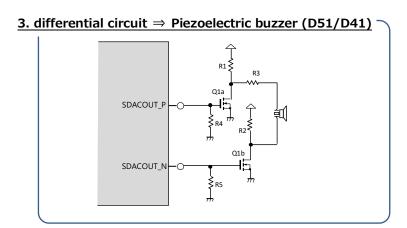
Please see the circuit in D50/D51/D41 Evaluation Board manual to the details.

1. AMP \Rightarrow Speaker(D50/D51/D41) | PPORT | Enable Control | SDACOUT_N | SDACOUT_N | SDACOUT_P | SDACO





note) Resistance value depends on the power supply for the buzzer, please check each evaluation manual.



note) Resistance value depends on the power supply for the buzzer, please check each evaluation manual.

■ Revision History

Contents						
Date	Rev.	Page	Туре	Details		
2018/7/30	1.00	All	New	New release		
2020/6/30	2.00	All	Changed	Added S1C31D51		
2020/12/15	2.01	All	Changed	Deleted "FEAUTURES" – Embedded RAMS – Instruction cache Modified "Basic External Connection Diagram"		
2021/2/15	2.02	p.13	Changed	Corrected "Basic External Connection Diagram"		
2022/6/2	3.00	All	Changed	Added S1C31D41		

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