S1C31D50 (rev1.0)

EPSON
EXCEED YOUR VISION

32-bit Single Chip Microcontroller

- ARM® 32-bit RISC CPUcore Cortex®-M0+
- Embedded 192K bytes Flash memory(Program & Sound ROM), 8K bytes RAM
- "Voice/Audio Play"(2ch mixing play, Voice Speed Conversion w/o CPU resource)
- "Self Memory Check" w/o CPU resource

ARM®

■ DESCRIPTIONS

The S1C31D50 is a 32-bit ARM® Cortex®-M0+ MCU which integrates a specific hardware block called the HW Processor. The HW Processor can perform 2ch Voice/Audio Play, Voice Speed Conversion, and Self Memory Check without using any CPU resource. The S1C31D50 is suitable for home electronics, white goods, and battery-based products which require voice and audio playback.

With the HW Processor, low memory footprint and multi-language support are achievable because of its integrated high-compression algorithm for voice and audio.

Furthermore, the EPSON Voice Creation PC tool makes development without studio recording easy. (EPSON Voice Creation PC tool supports English, Chinese, Japanese, and Korean female voices.)

■ FEATURES

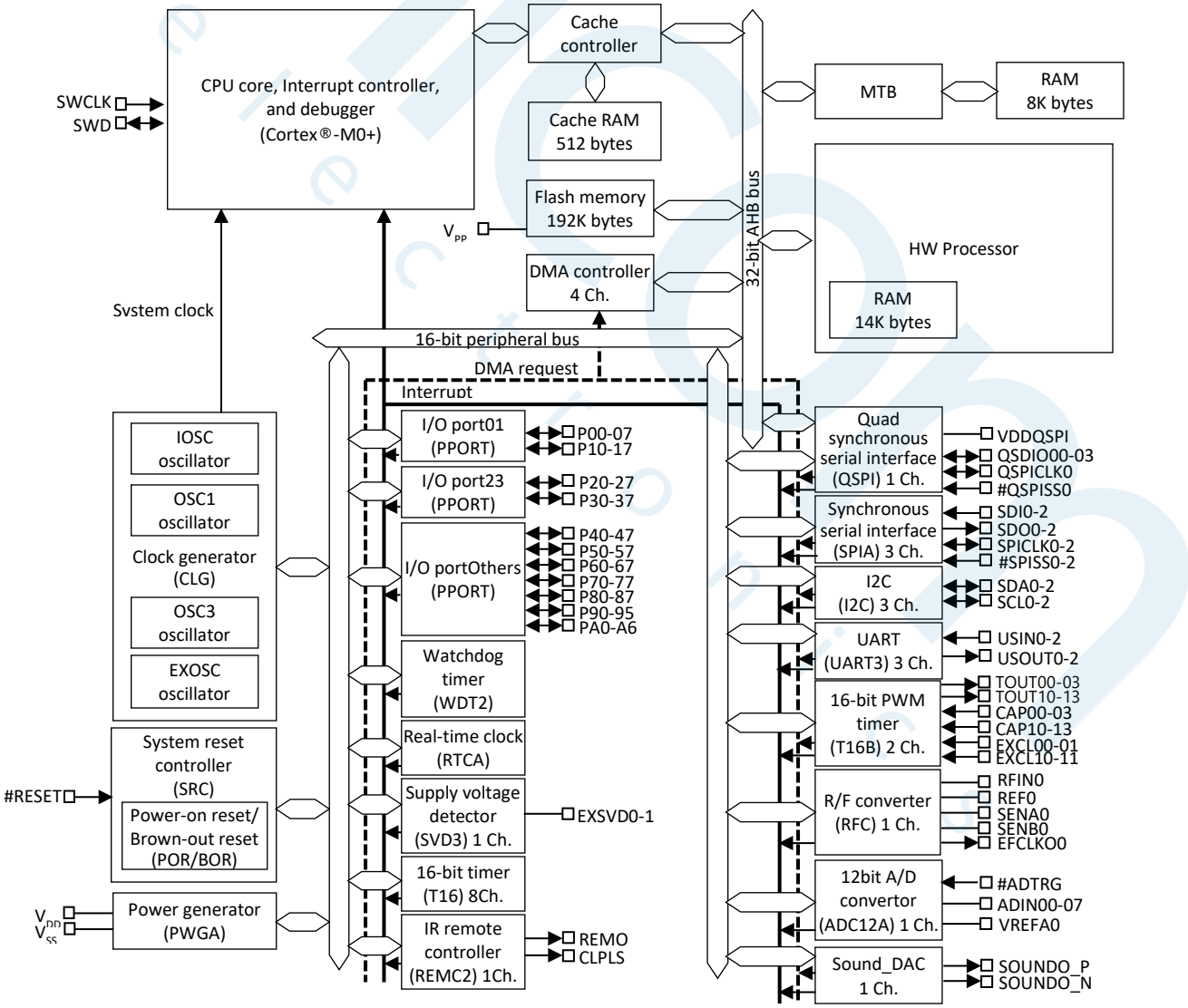
Model	S1C31D50
CPU	
CPU core	ARM® 32-bit RISC CPU core Cortex®-M0+
Other	Serial-wire debug ports (SW-DP) and a micro trace buffer (MTB) included
Embedded Flash memory	
Capacity	192K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * When being programmed by the dedicated flash loader
Other	On-board programming function
	Flash programming voltage can be generated internally.
Embedded RAMs	
General-purpose RAM	8K bytes + 14K bytes (when HW Processor is not active)
Instruction cache	512 bytes
HW Processor	
Voice Audio Play FUNCTION	
Voice/Audio Algorithm	EPSON high quality & High compress algorithm
Play channels	2ch mixing support(suitable for background music + Voice play
Sampling Frequency	15.625kHz, (suitable for background music + Voice play)
Bitrate	16/24/32/40 kbps
Voice Speed Conversion	75% - 125% (5% step)
Self Memory Check FUNCTION	
On Chip RAM Check	W/R Check, MARCH-C
On Chip Flash check	Checksum, CRC
External SPI-Flash Check	Checksum, CRC
Sound DAC	
Sampling Frequency	15.625kHz
Serial interfaces	
UART (UART3)	3 channels
	Baud-rate generator included, IrDA1.0 supported
	Open drain output, signal polarity, and baud rate division ratio are configurable.
	Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)	3 channels
	2 to 16-bit variable data length
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
Quad synchronous serial interface (QSPI)	1 channel
	Supports single, dual, and quad transfer modes.
	Low CPU overhead memory mapped access mode that can directly read data from the external flash memory with XIP (eXecute-In-Place) mode.
I^2C (I2C)	3 channels
	Baud-rate generator included
DMA Controller (DMAC)	
Number of channels	4 channels
Data transfer path	Memory to memory, memory to peripheral, and peripheral to memory
Transfer mode	Basic, ping-pong, scatter-gather
DMA trigger source	UART3, SPIA, QSPI, I2C, T16B, ADC12A, and software

Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	V_{D1} voltage mode = mode0: 16 MHz (max.) V_{D1} voltage mode = mode1: 2 MHz (max.)
IOSC oscillator circuit (boot clock source)	V_{D1} voltage mode = mode0: 8/2/1 MHz (typ.) software selectable V_{D1} voltage mode = mode1: 2/1 MHz (typ.) software selectable
	10 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	32kHz (typ.) embedded oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	16 MHz (max.) crystal/ceramic oscillator
	16/8/4MHz(typ) embedded oscillator
EXOSC clock input	16 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	PKG48pin : 39bit(max.) PKG64pin : 55bit(max.) PKG80pin : 71bit(max.) PKG100pin : 91bit (max.)
	Pins are shared with the peripheral I/O.
Number of input interrupt ports	PKG48pin : 33bit(max.) PKG64pin : 49bit(max.) PKG80pin : 65bit(max.) PKG100pin : 85bit (max.)
Number of ports that support universal port multiplexer(UPMUX)	PKG48pin : 16bit(max.) PKG64pin : 24bit(max.) PKG80pin : 27bit(max.) PKG100pin : 32bit (max.)
	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.
	Programmable NMI/reset generation cycle
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	8 channels
	Generates the SPIA and QSPI master clocks, and the ADC12A operating clock/ trigger signal.
16-bit PWM timer (T16B)	2 channels
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 4 ports/channel
Supply voltage detector (SVD3)	
Number of channels	1 channel
Detection voltage	V_{DD} or an external voltage (2 external detection ports are available.)
Detection level	V_{DD}: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
12-bit A/D converter (ADC12A)	
Conversion method	Successive approximation type
Resolution	12 bits
Number of conversion channels	1 channel
Number of analog signal inputs	8 ports/channel (max)
R/F converter（RFC）	
Conversion method	CR oscillation type 24-bit counters
Number of conversion channels	1 channel
Supported sensors	DC bias resistive sensors
IR remote controller (REMC3)	
Number of transmitter channels	1 channel
Other	EL lamp drive waveform can be generated (by the hardware) for an application ex- ample.
	Output inversion function
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Brown-out reset	Reset when the power supply voltage drops (when $V_{DD} \leq 1.45$ V (typ.) is detected).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/ disabled using a register).
Interrupt	
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTic)
Programmable interrupt	External interrupt: 3 systems
	Internal interrupt: 27 systems

Power supply voltage	
V_{DD} operating voltage	1.8 to 5.5 V　* If V_{DD} > 3.6 V, the V_{D1} voltage mode must be mode0.
V_{DD} operating voltage for Flash programming	2.4 to 5.5 V (when V_{PP} is supplied externally) 2.7 to 5.5 V (when V_{PP} is generated internally)
SPI-Flash interface power supply VDDQSPI	3.0 to 3.6V（possible to set main V_{DD}:5v, SPI-Flash power supply :3.3v）
Operating temperature	
Operating temperature range	-40 to 85 °C
Current consumption (Typ. value)	
SLEEP mode *1	0.46 µA (TBD) IOSC = OFF, OSC1 = OFF, OSC3 = OFF
	0.95 µA (TBD) IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF, RTCA = ON
HALT mode *2	1.7 µA (TBD) IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF
RUN mode	250 µA/MHz (TBD) V_{D1} voltage mode = mode0, CPU = IOSC
	155 µA/MHz (TBD) V_{D1} voltage mode = mode1, CPU = IOSC
Shipping form	
1	TQFP12-48 (　7mm x　7mm, 0.5mm pitch)
2	QFP13-64　(10mm x 10mm, 0.5mm pitch)
3	TQFP14-80 (12mm x 12mm, 0.5mm pitch)
4	QFP15-100 (14mm x 14mm, 0.5mm pitch)

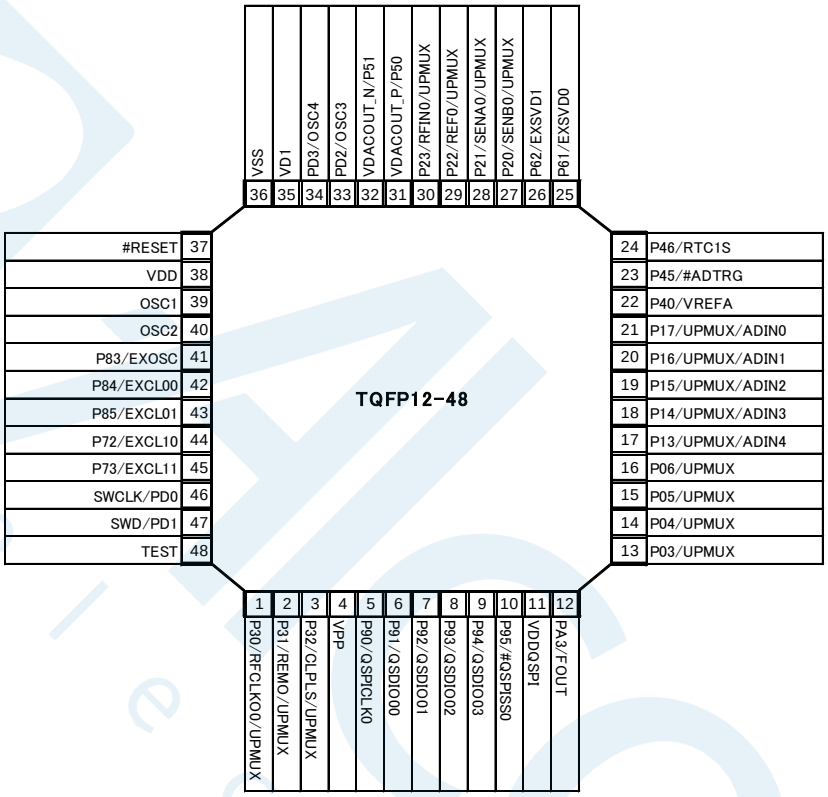
*1 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor.
*2 HALT mode refers to sleep mode in the Cortex®-M0+ processor.

■ Block Diagram

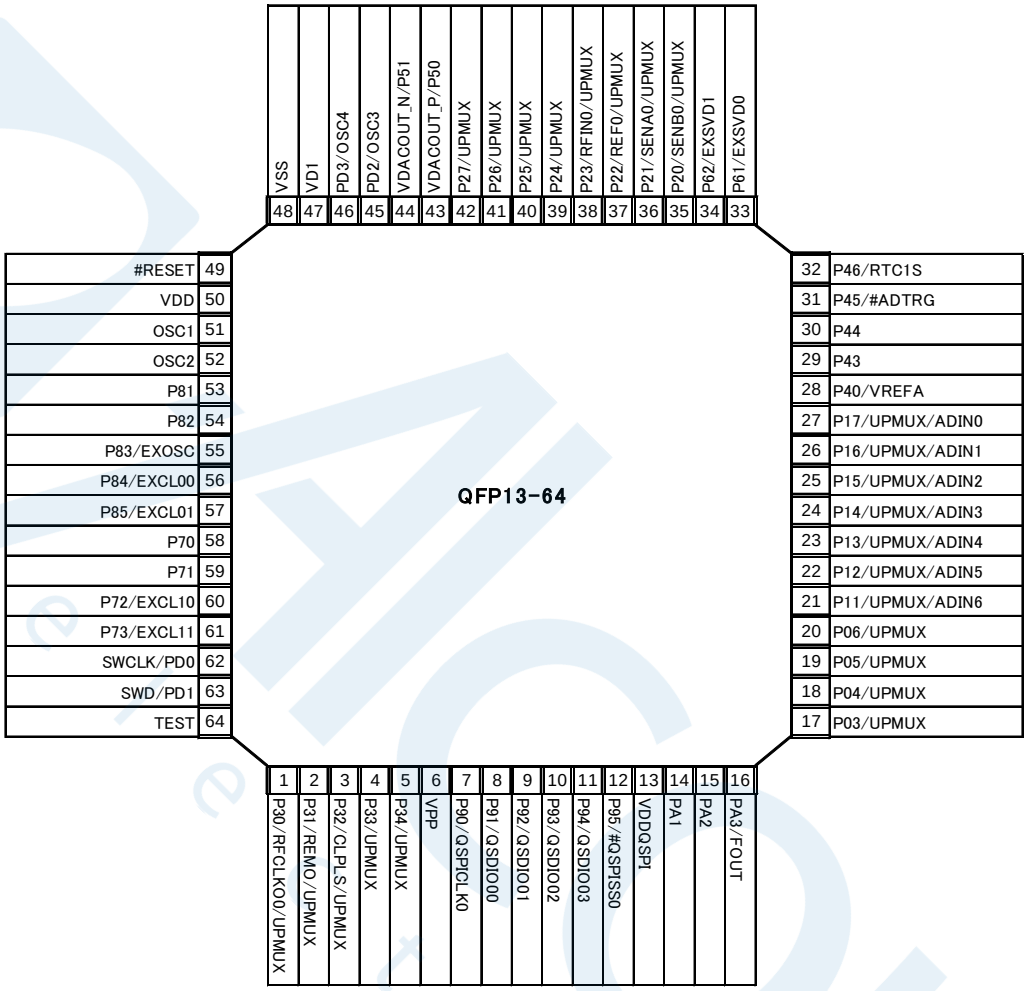


■ Pin Configuration Diagram

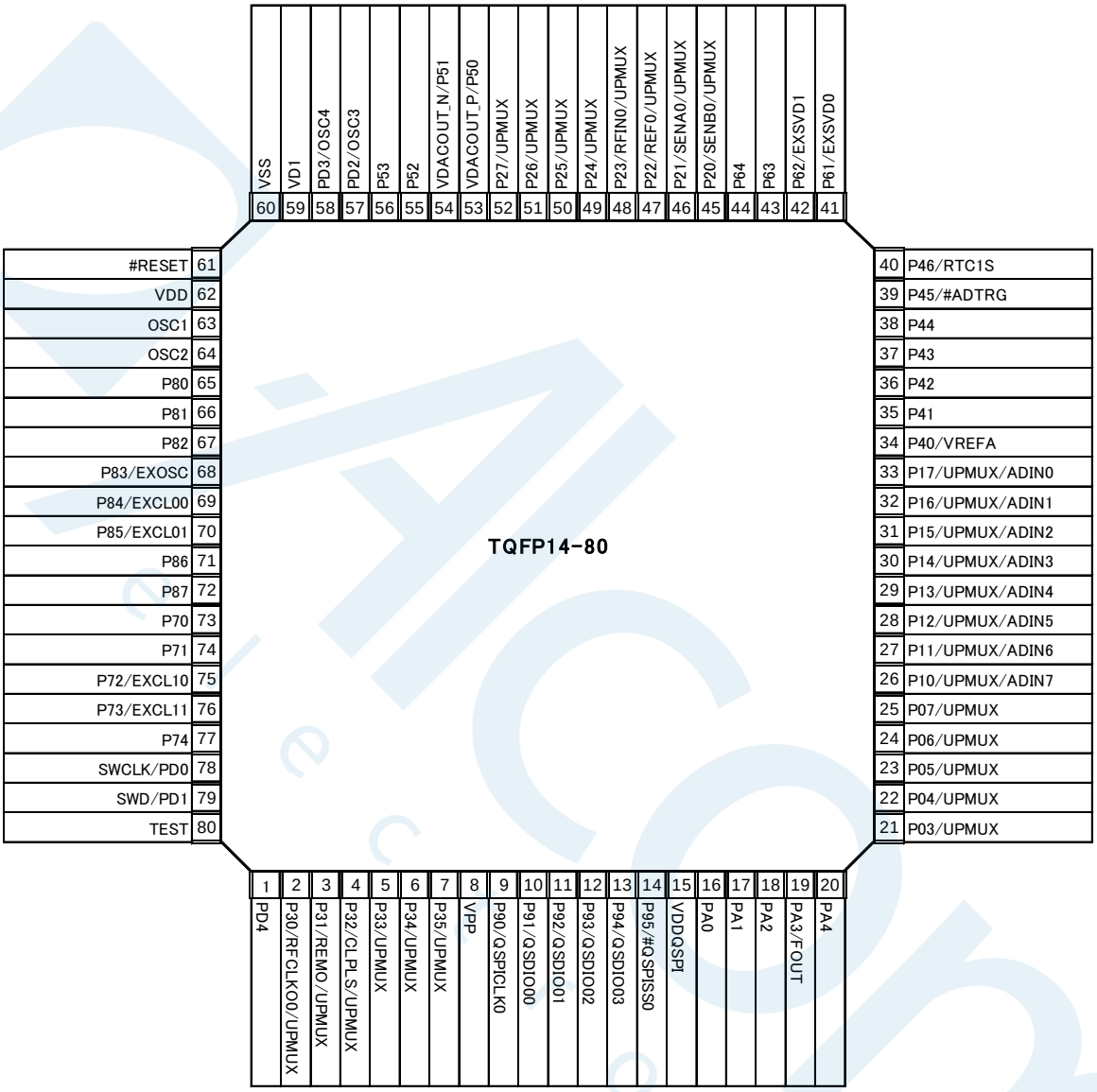
TQFP12-48



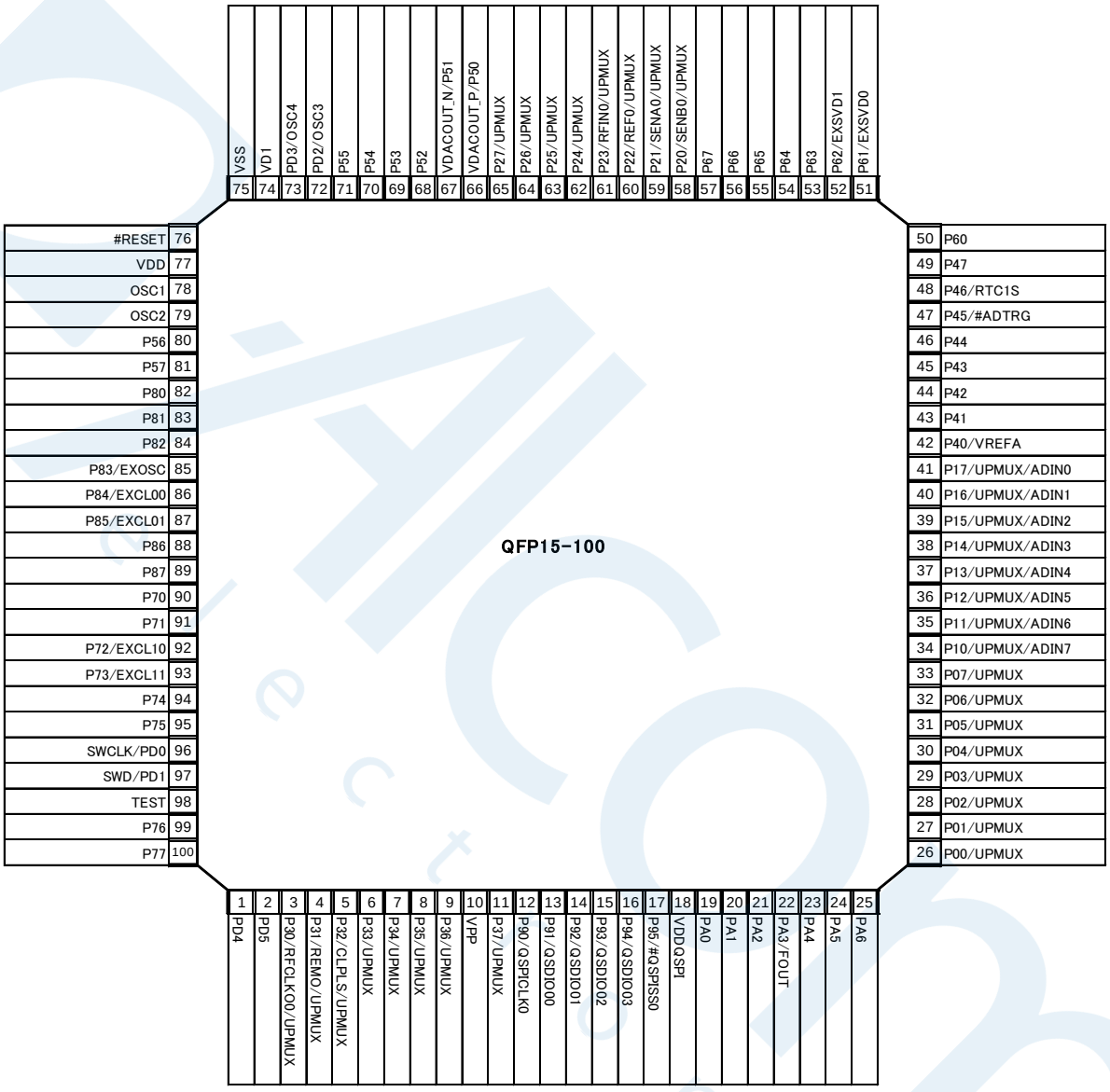
QFP13-64


QFP13-64
1 P30/RFCLKO0/UPMUX
2 P31/REMO/UPMUX
3 P32/CLPLS/UPMUX
4 P33/UPMUX
5 P34/UPMUX
6 VPP
7 P90/QSPICLK0
8 P91/QSDIO00
9 P92/QSDIO01
10 P93/QSDIO02
11 P94/QSDIO03
12 P95/#QSPISS0
13 VDDQSPI
14 PA1
15 PA2
16 PA3/FOUT
17 P03/UPMUX
18 P04/UPMUX
19 P05/UPMUX
20 P06/UPMUX
21 P11/UPMUX/ADIN6
22 P12/UPMUX/ADIN5
23 P13/UPMUX/ADIN4
24 P14/UPMUX/ADIN3
25 P15/UPMUX/ADIN2
26 P16/UPMUX/ADIN1
27 P17/UPMUX/ADIN0
28 P40/VREFA
29 P43
30 P44
31 P45/#ADTRG
32 P46/RTC1S
33 P61/EXSVD0
34 P62/EXSVD1
35 P20/SENB0/UPMUX
36 P21/SENA0/UPMUX
37 P22/REF0/UPMUX
38 P23/RFIN0/UPMUX
39 P24/UPMUX
40 P25/UPMUX
41 P26/UPMUX
42 P27/UPMUX
43 VDACOUT_P/P50
44 VDACOUT_N/P51
45 PD2/OSC3
46 PD3/OSC4
47 VD1
48 VSS
49 #RESET
50 VDD
51 OSC1
52 OSC2
53 P81
54 P82
55 P83/EXOSC
56 P84/EXCL00
57 P85/EXCL01
58 P70
59 P71
60 P72/EXCL10
61 P73/EXCL11
62 SWCLK/PD0
63 SWD/PD1
64 TEST

TQFP14-80pin



QFP15-100pin



■ Pin Descriptions

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:	I	= Input
	O	= Output
	I/O	= Input/output
	P	= Power supply
	A	= Analog signal
	Hi-Z	= High impedance state
Initial state:	I (Pull-up)	= Input with pulled up
	I (Pull-down)	= Input with pulled down
	Hi-Z	= High impedance state
	O (H)	= High level output
	O (L)	= Low level output
Tolerant fail-safe structure:		
	✓	= Over voltage tolerant fail-safe type I/O cell included

Pin name	Pin function	I/O	Initial	Tolerant fail-safe structure	Description
VDD	VDD	P	-	-	Power(+)
VSS	VSS	P	-	-	GND
VPP	VPP	P	-	-	Flash Programing Power
VD1	VD1	A	-	-	
VDDQSPI	VDDQSPI	P	-	-	SPI Flash interface voltage supply.
OSC1	OSC1	A	-	-	OSC1 oscillator input
OSC2	OSC2	A	-	-	OSC1 oscillator output
TEST	TEST	I	I(Pull-down)	-	Test mode enable
#RESET	#RESET	I	I(Pull-up)	-	Reset input
P00	P00	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P01	P01	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P02	P02	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P03	P03	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P04	P04	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P05	P05	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P06	P06	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–

P07	P07 – UPMUX –	I/O	Hi-Z	✓	I/O port – UPMUX –
P10	P10 – UPMUX ADIN7	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P11	P11 – UPMUX ADIN6	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P12	P12 – UPMUX ADIN5	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P13	P13 – UPMUX ADIN4	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P14	P14 – UPMUX ADIN3	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P15	P15 – UPMUX ADIN2	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P16	P16 – UPMUX ADIN1	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P17	P17 – UPMUX ADIN0	I/O	Hi-Z	-	I/O port – UPMUX ADC ch.0
P20	P20 SENB0 UPMUX –	I/O	Hi-Z	✓	I/O port RFC UPMUX –
P21	P21 SENA0 UPMUX –	I/O	Hi-Z	✓	I/O port RFC UPMUX –
P22	P22 REF0 UPMUX –	I/O	Hi-Z	✓	I/O port RFC UPMUX –
P23	P23 RFIN0 UPMUX -	I/O	Hi-Z	✓	I/O port RFC UPMUX -
P24	P24 - UPMUX –	I/O	Hi-Z	✓	I/O port - UPMUX –
P25	P25 - UPMUX -	I/O	Hi-Z	✓	I/O port - UPMUX -

P26	P26	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P27	P27	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P30	P30	I/O	Hi-Z	✓	I/O port
	RFCLKO0				RFC
	UPMUX				UPMUX
	–				–
P31	P31	I/O	Hi-Z	✓	I/O port
	REMO				REMC2
	UPMUX				UPMUX
	–				–
P32	P32	I/O	Hi-Z	✓	I/O port
	CLPLS				REMC2
	UPMUX				UPMUX
	–				–
P33	P33	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P34	P34	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P35	P35	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P36	P36	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P37	P37	I/O	Hi-Z	✓	I/O port
	–				–
	UPMUX				UPMUX
	–				–
P40	P40	I/O	Hi-Z	-	I/O port
	–				–
	–				–
	VREFA				ADC ch.0
P41	P41	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P42	P42	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P43	P43	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P44	P44	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–

P45	P45	I/O	Hi-Z	✓	I/O port
	#ADTRG				ADC
	–				–
	–				–
P46	P46	I/O	Hi-Z	✓	I/O port
	RTC1S				RTCA
	–				–
	–				–
P47	P47	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P50	VDACOUT_P	I/O	O(L)	✓	VDAC(default)
	P50				I/O port
	–				–
	–				–
P51	VDACOUT_N	I/O	O(L)	✓	VDAC(default)
	P51				I/O port
	–				–
	–				–
P52	P52	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P53	P53	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P54	P54	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P55	P55	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P56	P56	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P57	P57	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P60	P60	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
P61	P61	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	EXSVD0				SVD3 Ch.0
P62	P62	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	EXSVD1				SVD3 Ch.0
P63	P63	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–

P64	P64 – – –	I/O	Hi-Z	✓	I/O port – – –
P65	P65 – – –	I/O	Hi-Z	✓	I/O port – – –
P66	P66 – – –	I/O	Hi-Z	✓	I/O port – – –
P67	P67 – – –	I/O	Hi-Z	✓	I/O port – – –
P70	P70 – – –	I/O	Hi-Z	✓	I/O port – – –
P71	P71 – – –	I/O	Hi-Z	✓	I/O port – – –
P72	P72 EXCL10 – –	I/O	Hi-Z	✓	I/O port T16B Ch.1 – –
P73	P73 EXCL11 – –	I/O	Hi-Z	✓	I/O port T16B Ch.1 – –
P74	P74 – – –	I/O	Hi-Z	✓	I/O port – – –
P75	P75 – – –	I/O	Hi-Z	✓	I/O port – – –
P76	P76 – – –	I/O	Hi-Z	✓	I/O port – – –
P77	P77 – – –	I/O	Hi-Z	✓	I/O port – – –
P80	P80 – – –	I/O	Hi-Z	✓	I/O port – – –
P81	P81 – – –	I/O	Hi-Z	✓	I/O port – – –
P82	P82 – – –	I/O	Hi-Z	✓	I/O port – – –

P83	P83 EXOSC – –	I/O	Hi-Z	✓	I/O port CLG – –
P84	P84 EXCL00 – –	I/O	Hi-Z	✓	I/O port T16B Ch.0 – –
P85	P85 EXCL01 – –	I/O	Hi-Z	✓	I/O port T16B Ch.0 – –
P86	P86 – – –	I/O	Hi-Z	✓	I/O port – – –
P87	P87 – – –	I/O	Hi-Z	✓	I/O port – – –
P90	P90 QSPICLK0 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
P91	P91 QSDIO00 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
P92	P92 QSDIO01 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
P93	P93 QSDIO02 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
P94	P94 QSDIO03 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
P95	P95 #QSPISS0 – –	I/O	Hi-Z	✓	I/O port QSPI Ch.0 – –
PA0	PA0 – – –	I/O	Hi-Z	✓	I/O port – – –
PA1	PA1 – – –	I/O	Hi-Z	✓	I/O port – – –
PA2	PA2 – – –	I/O	Hi-Z	✓	I/O port – – –
PA3	PA3 FOUT – –	I/O	Hi-Z	✓	I/O port CLG – –

PA4	PA4	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
PA5	PA5	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
PA6	PA6	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
PD0	SWCLK	I/O	(Pull-up)	✓	DBG(default)
	PD0				I/O port
	–				–
	–				–
PD1	SWD	I/O	(Pull-up)	✓	DBG(default)
	PD1				I/O port
	–				–
	–				–
PD2	PD2	I/O	Hi-Z	-	I/O port
	–				–
	–				–
	OSC3				CLG
PD3	PD3	I/O	Hi-Z	-	I/O port
	–				–
	–				–
	OSC4				CLG
PD4	PD4	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–
PD5	PD5	I/O	Hi-Z	✓	I/O port
	–				–
	–				–
	–				–

Note:
In the peripheral circuit descriptions, the assigned signal name is used as the pin name.

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below.

Table 1.3.3.2 Peripheral Circuit Input/output Function Selectable by UPMUX

Peripheral	Signal	I/O	Ch.No.		Function
I2C	SCLn	I/O	n=0,1,2	-	I2C Ch.n clock input/output
	SDAn	I/O		-	I2C Ch.n data input/output
UART	USINn	I	n=0,1,2	-	UART Ch,n data input
	USOUTn	O		-	UART Ch,n data output
SPI	SDIn	I	n=0,1,2	-	SPIA ch.n data input
	SDOn	O		-	SPIA ch.n data output
	SPICLKn	I/O		-	SPIA Ch.n clock input/output
	#SPISSn	I		-	SPIA Ch.n slave-select input
PWM timer	TOUTn0/CAPn0	I/O	n=0,1	-	16-bit PWM timer Ch.n PWM output / caputure input 0
	TOUTn1/CAPn1	I/O		-	16-bit PWM timer Ch.n PWM output / caputure input 1
	TOUTn2/CAPn2	I/O		-	16-bit PWM timer Ch.n PWM output / caputure input 2
	TOUTn3/CAPn3	I/O		-	16-bit PWM timer Ch.n PWM output / caputure input 3

Note: Do not assign a function to two or more pins simultaneously.

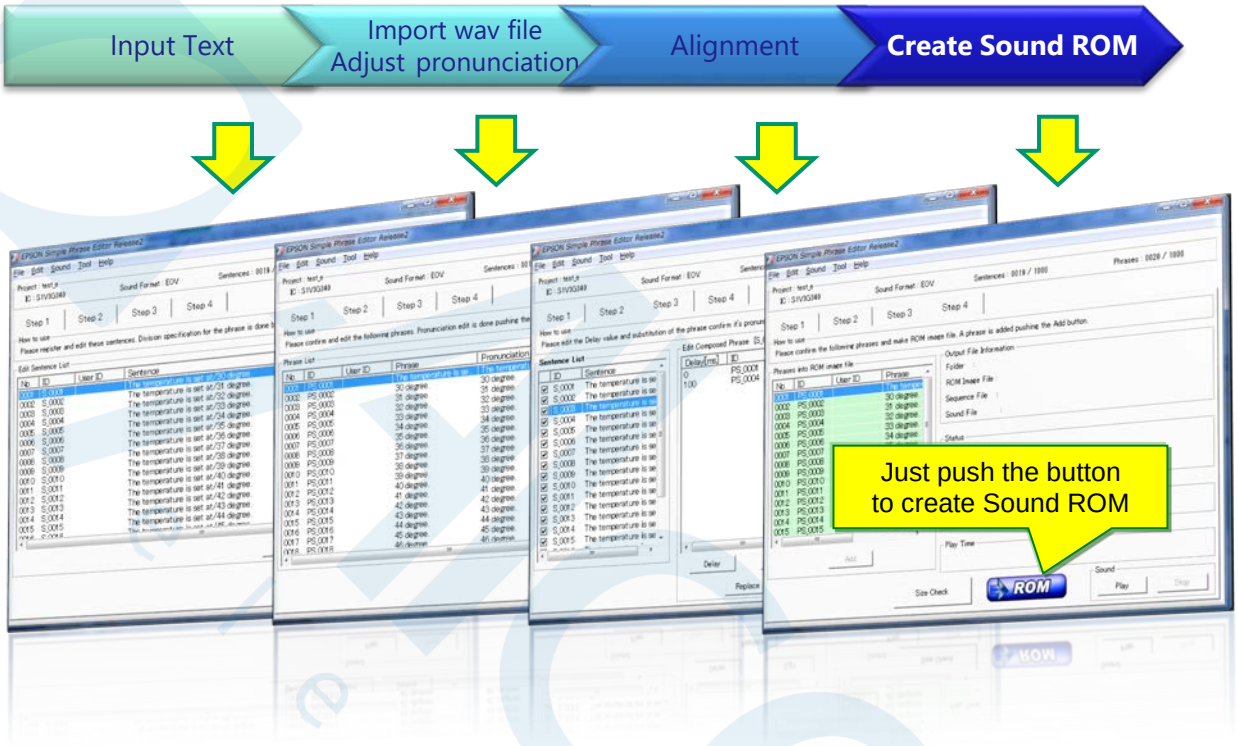
Pin Details

QFP15 -100 Pin. No	TQFP14 -80 Pin. No	QFP13 -64 Pin. No	TQFP12 -48 Pin. No	Pin Name	Function
1	1	—	—	PD4	PD4
2	—	—	—	PD5	PD5
3	2	1	1	P30	P30/RFCLKO0/UPMUX
4	3	2	2	P31	P31/REMO/UPMUX
5	4	3	3	P32	P32/CLPLS/UPMUX
6	5	4	—	P33	P33/UPMUX
7	6	5	—	P34	P34/UPMUX
8	7	—	—	P35	P35/UPMUX
9	—	—	—	P36	P36/UPMUX
10	8	6	4	VPP	VPP
11	—	—	—	P37	P37/UPMUX
12	9	7	5	P90	P90/QSPICLK0
13	10	8	6	P91	P91/QSDIO00
14	11	9	7	P92	P92/QSDIO01
15	12	10	8	P93	P93/QSDIO02
16	13	11	9	P94	P94/QSDIO03
17	14	12	10	P95	P95/#QSPISS0
18	15	13	11	VDDQSPI	VDDQSPI
19	16	—	—	PA0	PA0
20	17	14	—	PA1	PA1
21	18	15	—	PA2	PA2
22	19	16	12	PA3	PA3/FOUT
23	20	—	—	PA4	PA4
24	—	—	—	PA5	PA5
25	—	—	—	PA6	PA6
26	—	—	—	P00	P00/UPMUX
27	—	—	—	P01	P01/UPMUX
28	—	—	—	P02	P02/UPMUX
29	21	17	13	P03	P03/UPMUX
30	22	18	14	P04	P04/UPMUX
31	23	19	15	P05	P05/UPMUX
32	24	20	16	P06	P06/UPMUX
33	25	—	—	P07	P07UPMUX
34	26	—	—	P10	P10/UPMUX/ADIN7
35	27	21	—	P11	P11/UPMUX/ADIN6
36	28	22	—	P12	P12/UPMUX/ADIN5
37	29	23	17	P13	P13/UPMUX/ADIN4
38	30	24	18	P14	P14/UPMUX/ADIN3
39	31	25	19	P15	P15/UPMUX/ADIN2
40	32	26	20	P16	P16/UPMUX/ADIN1
41	33	27	21	P17	P17/UPMUX/ADIN0
42	34	28	22	P40	P40/VREFA
43	35	—	—	P41	P41
44	36	—	—	P42	P42
45	37	29	—	P43	P43
46	38	30	—	P44	P44
47	39	31	23	P45	P45/#ADTRG
48	40	32	24	P46	P46/RTC1S
49	—	—	—	P47	P47
50	—	—	—	P60	P60
51	41	33	25	P61	P61/EXSVD0
52	42	34	26	P62	P62/EXSVD1
53	43	—	—	P63	P63
54	44	—	—	P64	P64
55	—	—	—	P65	P65
56	—	—	—	P66	P66

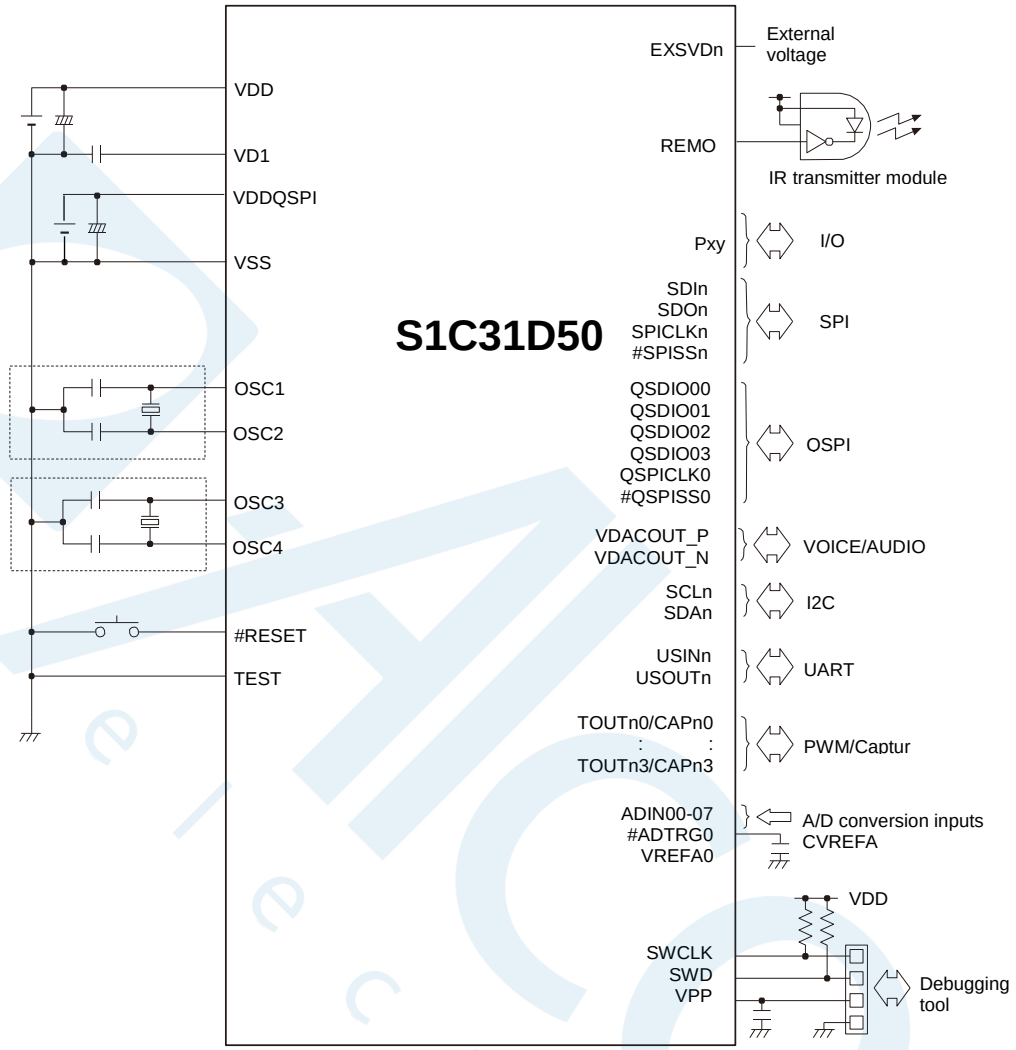
57	—	—	—	P67	P67
58	45	35	27	P20	P20/SENB0/UPMUX
59	46	36	28	P21	P21/SENA0/UPMUX
60	47	37	29	P22	P22/REF0/UPMUX
61	48	38	30	P23	P23/RFIN0/UPMUX
62	49	39	—	P24	P24/UPMUX
63	50	40	—	P25	P25/UPMUX
64	51	41	—	P26	P26/UPMUX
65	52	42	—	P27	P27/UPMUX
66	53	43	31	P50	P50/VDACOUT_P
67	54	44	32	P51	P51/VDACOUT_N
68	55	—	—	P52	P52
69	56	—	—	P53	P53
70	—	—	—	P54	P54
71	—	—	—	P55	P55
72	57	45	33	PD2	PD2/OCS3
73	58	46	34	PD3	PD3/OSC4
74	59	47	35	VD1	VD1
75	60	48	36	VSS	VSS
76	61	49	37	#RESET	#RESET
77	62	50	38	VDD	VDD
78	63	51	39	OSC1	OSC1
79	64	52	40	OSC2	OSC2
80	—	—	—	P56	P56
81	—	—	—	P57	P57
82	65	—	—	P80	P80
83	66	53	—	P81	P81
84	67	54	—	P82	P82
85	68	55	41	P83	P83/EXOSC
86	69	56	42	P84	P84/EXCL00
87	70	57	43	P85	P85/EXCL01
88	71	—	—	P86	P86
89	72	—	—	P87	P87
90	73	58	—	P70	P70
91	74	59	—	P71	P71
92	75	60	44	P72	P72/EXCL10
93	76	61	45	P73	P73/EXCL11
94	77	—	—	P74	P74
95	—	—	—	P75	P75
96	78	62	46	PD0	PD0/SWCLK
97	79	63	47	PD1	PD1/SWD
98	80	64	48	TEST	TEST
99	—	—	—	P76	P76
100	—	—	—	P77	P77

■ EPSON Voice Creation PC Tool

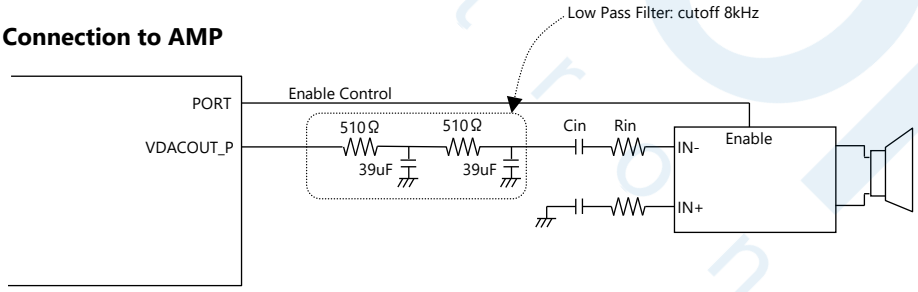
EPSON Voice creation PC tool makes voice related development easy because of no-studio recording, no narrator arrangement. This tool supports English, Chinese, Japanese and Korean(all female voice), and easily creation, modification can be done, by “wav file” import function, existing wav file can be used.



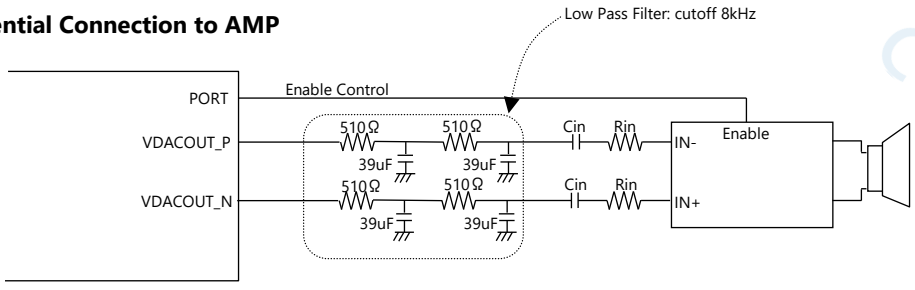
■ Basic External Connection Diagram

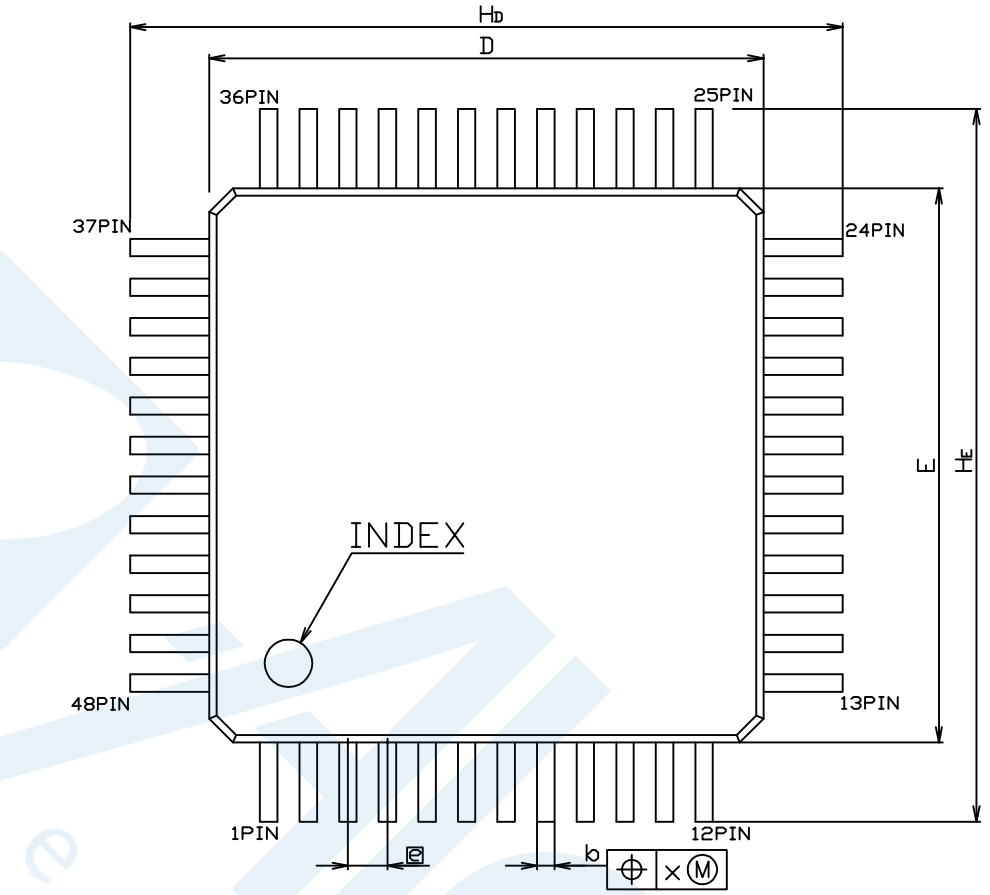


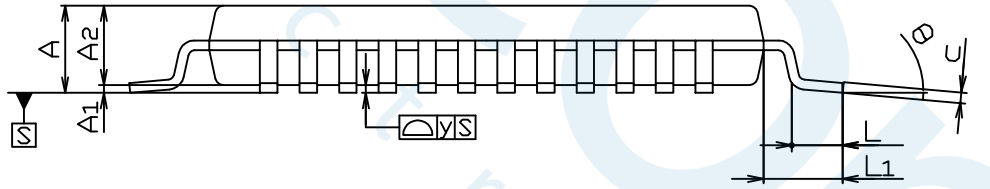
Single Connection to AMP



Differential Connection to AMP







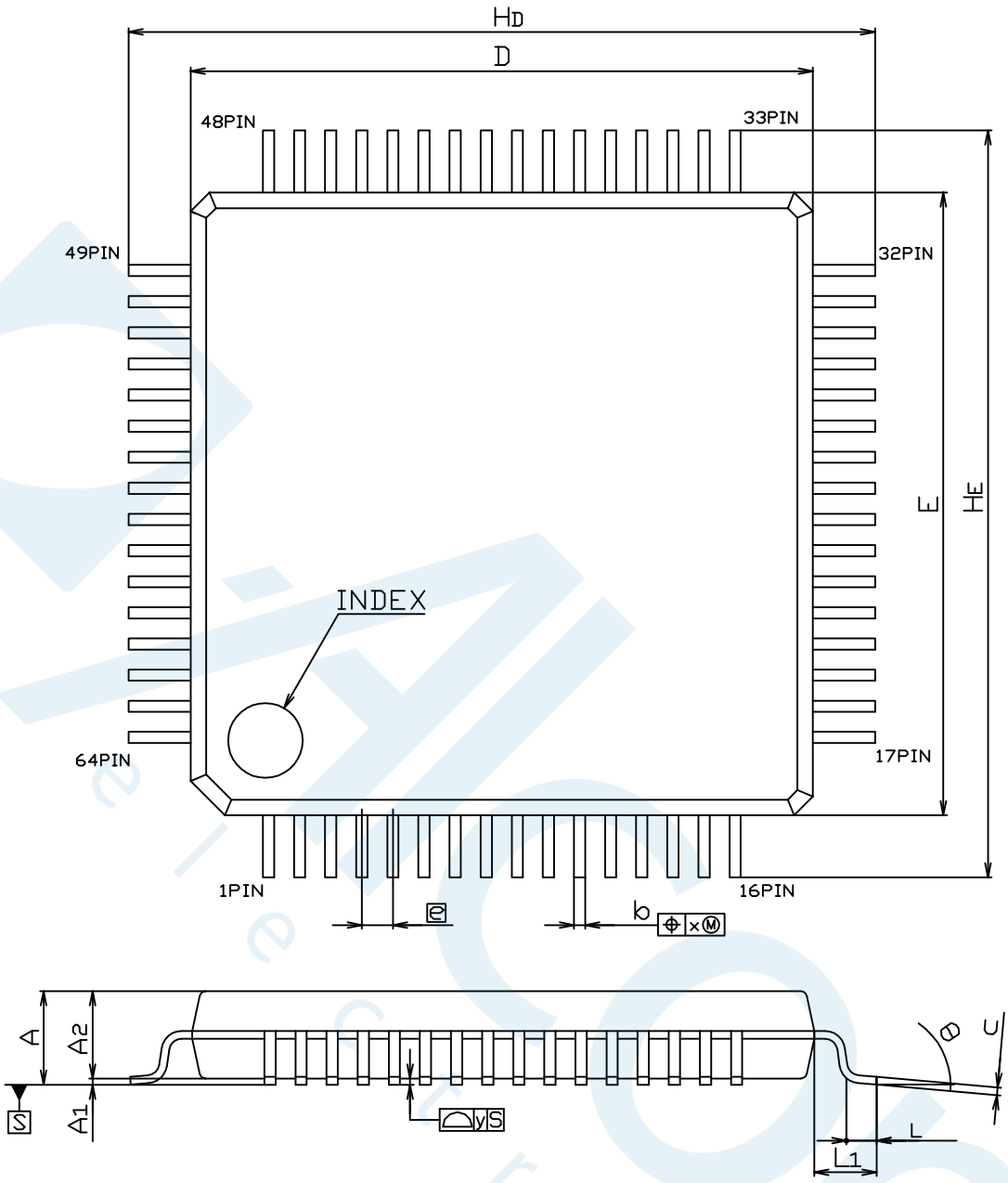
Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.90	7.00	7.10
E	6.90	7.00	7.10
A	–	–	1.20
A_1	0.00	0.10	0.20
A_2	0.90	1.00	1.10
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.70
L_1	0.80	1.00	1.20
H_D	8.60	9.00	9.40
H_E	8.60	9.00	9.40
x	–	–	0.08
y	–	–	0.10

Unit ; mm

TITLE

P-TQFP048-0707-0.50(TQFP12-48PIN)

SEIKO EPSON CORP.



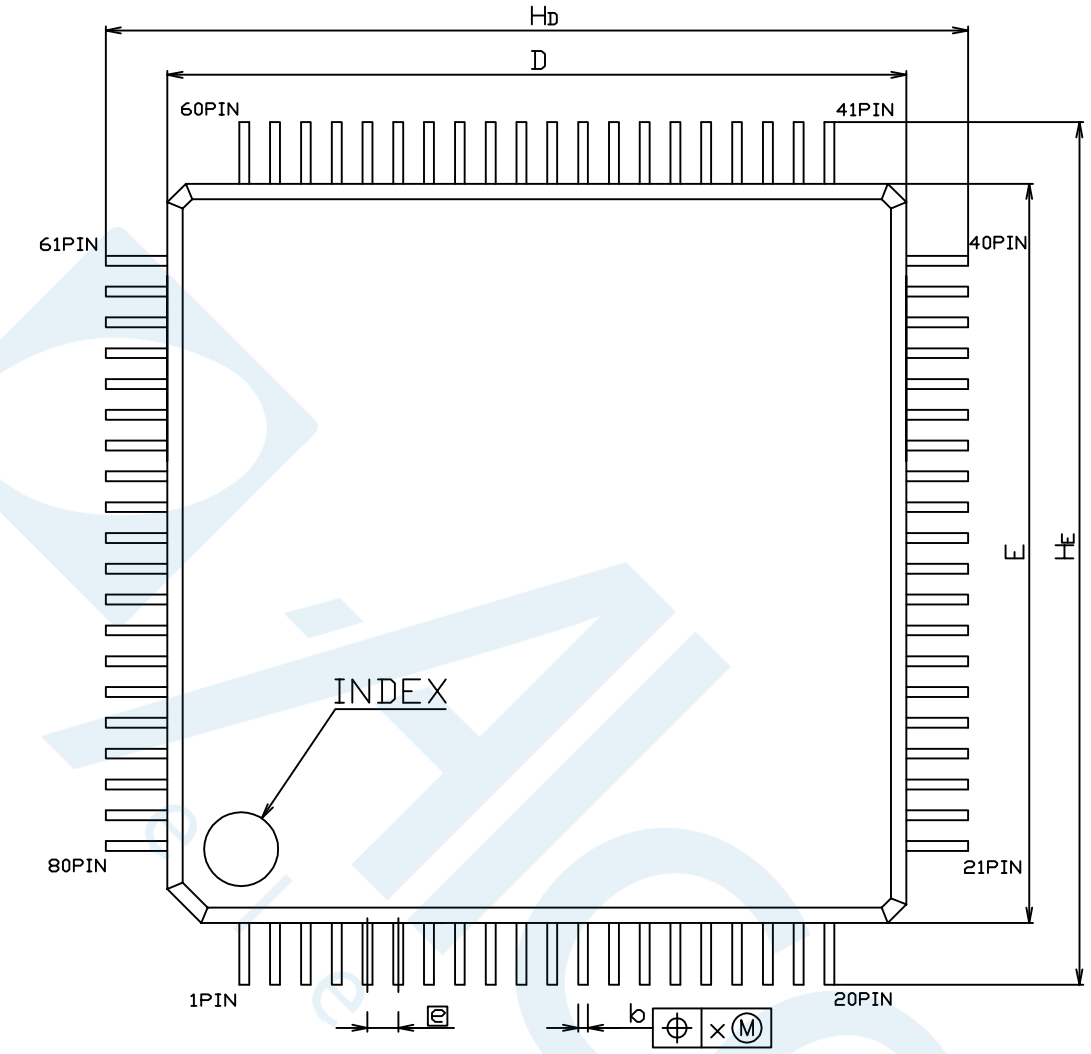
Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	9.90	10.00	10.10
D	9.90	10.00	10.10
A	–	–	1.70
A_1	0.00	0.10	0.20
A_2	1.30	1.40	1.50
e	–	0.50	–
b	0.13	0.20	0.27
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.75
L_1	0.80	1.00	1.20
H_E	11.60	12.00	12.40
H_D	11.60	12.00	12.40
x	–	–	0.08
y	–	–	0.08

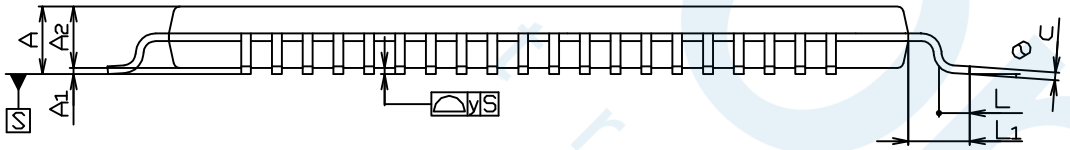
Unit ; mm

TITLE

P-LQFP064-1010-0.50(QFP13-64PIN)

SEIKO EPSON CORP.





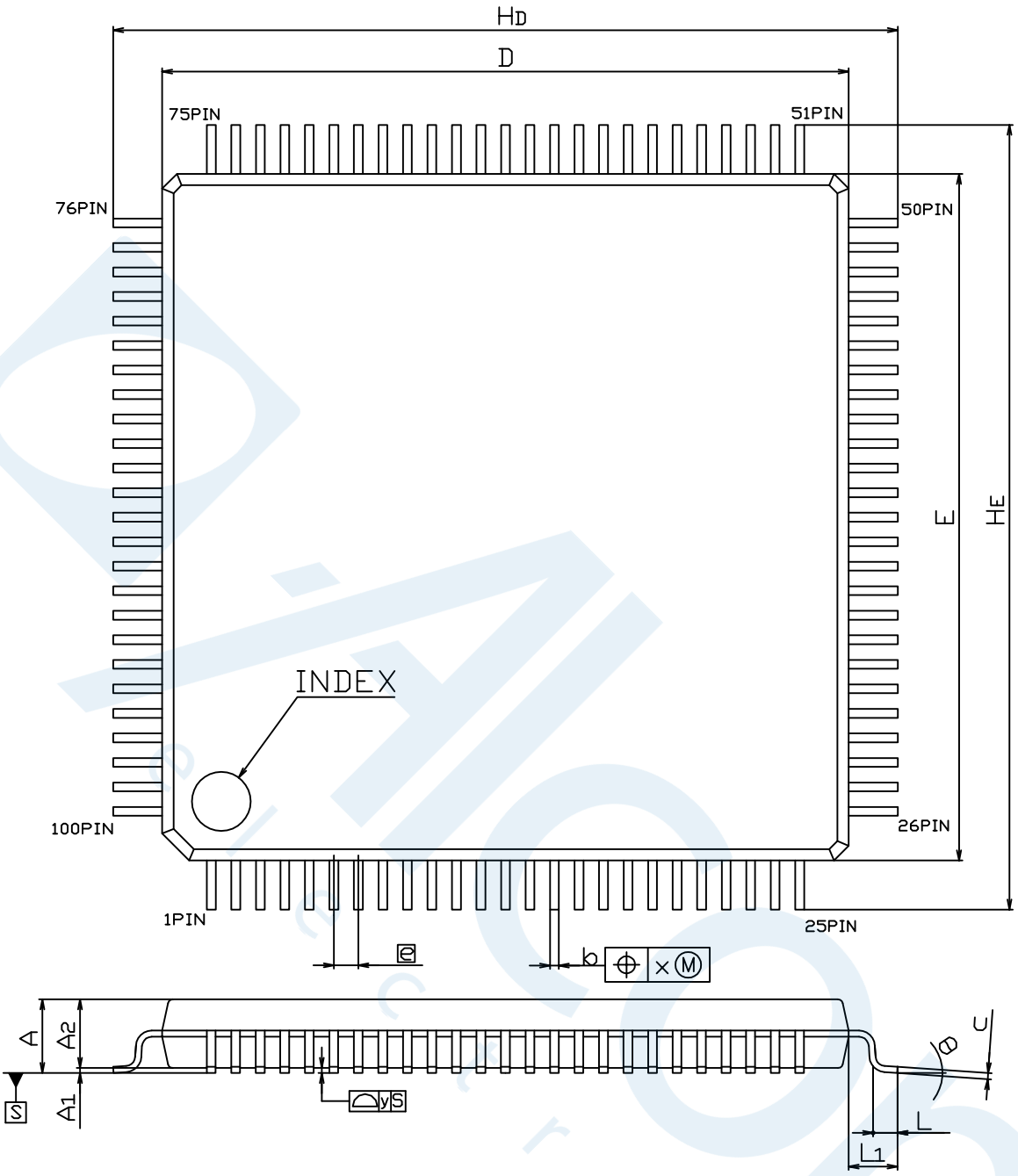
Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.90	12.00	12.10
E	11.90	12.00	12.10
A	–	–	1.20
A_1	0.00	0.10	0.20
A_2	0.90	1.00	1.10
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	0.15	0.20
θ	0°	3°	8°
L	0.30	0.50	0.75
L_1	0.80	1.00	1.20
H_D	13.60	14.00	14.40
H_E	13.60	14.00	14.40
x	–	–	0.08
y	–	–	0.08

Unit ; mm

TITLE

P-TQFP080-1212-0.50(TQFP14-80PIN)

SEIKO EPSON CORP.



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.90	14.00	14.10
E	13.90	14.00	14.10
A	–	–	1.70
A_1	0	0.10	0.20
A_2	1.30	1.40	1.50
e	–	0.50	–
b	0.17	0.22	0.27
c	0.09	0.15	0.20
θ	0°	5°	10°
L	0.30	0.50	0.75
L_1	0.80	1.00	1.20
H_D	15.60	16.00	16.40
H_E	15.60	16.00	16.40
x	–	–	0.08
y	–	–	0.08

Unit ; mm

TITLE

P-LQFP100-1414-0.50(QFP15-100PIN)

SEIKO EPSON CORP.

■ Revision History

Date	Revision details			
	Rev.	Page	Type	Details
2018/7/30	1.00	All	New	New release