



EFM32PG23 Gecko Family Data Sheet

The EFM32PG23 Gecko family of microcontrollers is part of the Series 2 Gecko portfolio. EFM32PG23 Gecko MCUs are ideal for enabling energy-friendly embedded applications.

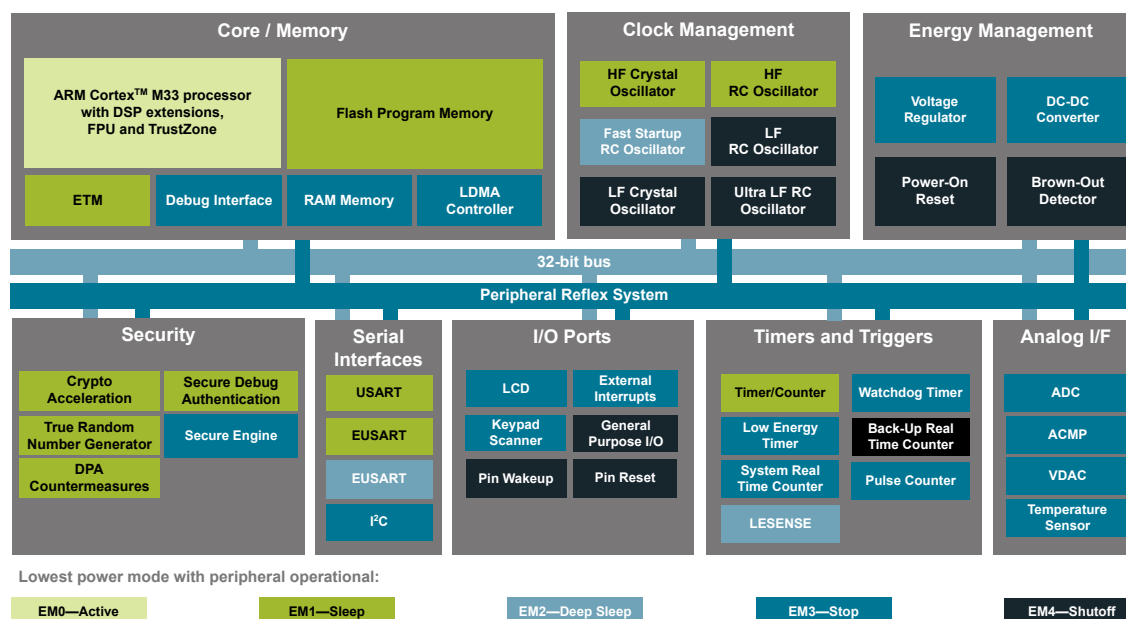
The highly efficient solution contains a 80 MHz Cortex-M33 with rich analog and communication peripherals to provide an industry-leading, energy efficient MCU for consumer and industrial applications.

Gecko applications include:

- Metering
- Industrial Automation
- Test and Measurement
- Appliances
- Portable Medical Devices

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 80 MHz maximum operating frequency
- Up to 512 kB of flash and 64 kB of RAM
- Robust peripheral set and up to 34 GPIO
- Low energy operation
 - 21 uA/MHz (EM0)
 - 1.03 uA sleep (EM2)
- 16-channel ADC with options for 12, 16, or 20-bit resolution
- Best-in-class security with Secure Vault



1. Feature List

The EFM32PG23 highlighted features are listed below.

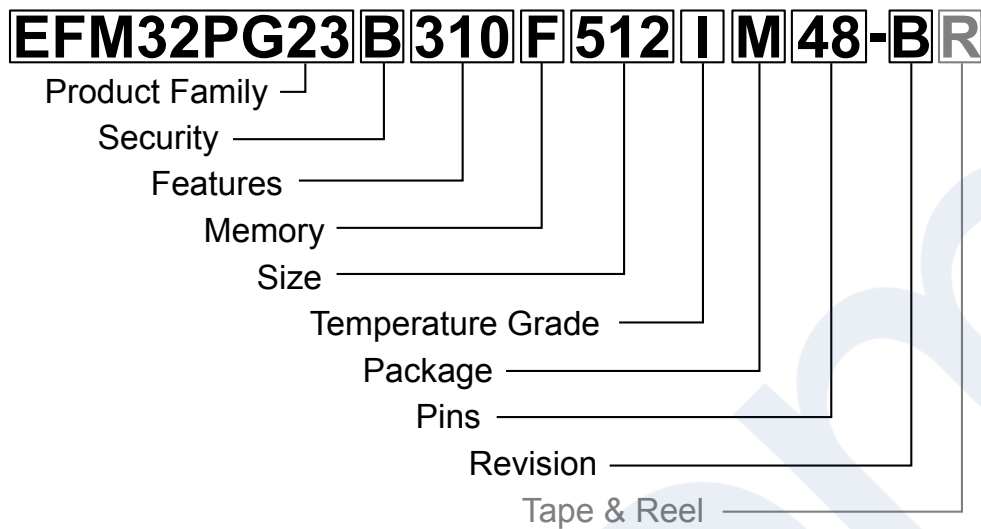
- **Low Power System-on-Chip**
 - High Performance 32-bit 80 MHz ARM Cortex[®]-M33 with DSP instruction and floating-point unit for efficient signal processing
 - Up to 512 kB flash program memory
 - Up to 64 kB RAM data memory
- **Low Energy Consumption**
 - 21 μ A/MHz in Active Mode (EM0) at 80 MHz
 - 1.33 μ A EM2 DeepSleep current (64 kB RAM retention and RTC running from LFXO)
 - 1.03 μ A EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Secure Vault**
 - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
 - True Random Number Generator (TRNG)
 - ARM[®] TrustZone[®]
 - Secure Boot (Root of Trust Secure Loader)
 - Secure Debug Unlock
 - DPA Countermeasures
 - Secure Key Management with PUF
 - Anti-Tamper
 - Secure Attestation
- **Wide Operating Range**
 - 1.71 V to 3.8 V single power supply
 - -40 °C to 125 °C
- **Wide selection of MCU peripherals**
 - Analog to Digital Converter (IADC) with flexible performance
 - 12, 16, or 20-bit output
 - High Speed Mode* up to 2 Msps
 - High Accuracy Mode* up to 16 bits ENOB at 3.8 ksp/s
 - 2 \times Analog Comparator (ACMP)
 - 2-Channel Digital to Analog Converter (VDAC)
 - Low-Energy Sensor Interface (LESENSE)
 - Up to 34 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller
 - 12 Channel Peripheral Reflex System (PRS)
 - 4 \times 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 1 \times 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 32-bit Real Time Counter
 - 24-bit Low Energy Timer for waveform generation
 - 16-bit Pulse Counter with asynchronous operation (PCNT)
 - 2 \times Watchdog Timer
 - 3 \times Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
 - 1 \times Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I²S)
 - 2 \times I²C interface with SMBus support
 - Integrated Low-Energy LCD Controller supporting up to 80 segments
 - Keypad scanner supporting up to 6 \times 8 matrix (KEYSCAN)
 - Die temperature sensor with typical \pm 1.5 °C accuracy across temperature range
- **Packages**
 - **QFN40** 5 mm \times 5 mm \times 0.85 mm
 - **QFN48** 6 mm \times 6 mm \times 0.85 mm

* IADC High Speed and High Accuracy modes available only on select part numbers. All devices support "Normal" operation mode with speeds up to 1 Msps.

2. Ordering Information

Table 2.1. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | Secure Vault | GPIO | LCD | IADC High-Speed / High-Accuracy | Package / Pinout | Temp Range |
|-------------------------|------------|----------|--------------|------|-----|---------------------------------|------------------------|---------------|
| EFM32PG23B310F64IM48-C | 64 | 32 | High | 32 | Yes | Yes | QFN48 with VREF Inputs | -40 to 125 °C |
| EFM32PG23B310F512IM48-C | 512 | 64 | High | 32 | Yes | Yes | QFN48 with VREF Inputs | -40 to 125 °C |
| EFM32PG23B310F256IM48-C | 256 | 64 | High | 32 | Yes | Yes | QFN48 with VREF Inputs | -40 to 125 °C |
| EFM32PG23B310F128IM48-C | 128 | 64 | High | 32 | Yes | Yes | QFN48 with VREF Inputs | -40 to 125 °C |
| EFM32PG23B210F64IM48-C | 64 | 32 | High | 34 | Yes | No | QFN48 | -40 to 125 °C |
| EFM32PG23B210F512IM48-C | 512 | 64 | High | 34 | Yes | No | QFN48 | -40 to 125 °C |
| EFM32PG23B210F256IM48-C | 256 | 64 | High | 34 | Yes | No | QFN48 | -40 to 125 °C |
| EFM32PG23B210F128IM48-C | 128 | 64 | High | 34 | Yes | No | QFN48 | -40 to 125 °C |
| EFM32PG23B200F64IM40-C | 64 | 32 | High | 29 | Yes | No | QFN40 | -40 to 125 °C |
| EFM32PG23B200F512IM40-C | 512 | 64 | High | 29 | Yes | No | QFN40 | -40 to 125 °C |
| EFM32PG23B200F256IM40-C | 256 | 64 | High | 29 | Yes | No | QFN40 | -40 to 125 °C |
| EFM32PG23B200F128IM40-C | 128 | 64 | High | 29 | Yes | No | QFN40 | -40 to 125 °C |



| Field | Options |
|-----------------------|--|
| Product Family | <ul style="list-style-type: none"> • EFM32PG23: Gecko 23 Family |
| Security | <ul style="list-style-type: none"> • A: Secure Vault Mid • B: Secure Vault High |
| Features [f1][f2][f3] | <ul style="list-style-type: none"> • f1 <ul style="list-style-type: none"> • 3: Dedicated VREFP/N inputs. IADC supports High Speed, High Accuracy, and Normal modes • 2: No dedicated VREFP/N inputs. IADC supports Normal mode only, with VREFP on GPIO (PA00) • f2 <ul style="list-style-type: none"> • 1: Dedicated AIN0 and AIN1 inputs to IADC available • 0: No dedicated AIN0 and AIN1 inputs • f3 <ul style="list-style-type: none"> • 0: Unused |
| Memory | <ul style="list-style-type: none"> • F: Flash |
| Size | <ul style="list-style-type: none"> • Memory Size in kBytes |
| Temperature Grade | <ul style="list-style-type: none"> • G: -40 to +85 °C • I: -40 to +125 °C |
| Package | <ul style="list-style-type: none"> • M: QFN |
| Pins | <ul style="list-style-type: none"> • Number of Package Pins |
| Revision | <ul style="list-style-type: none"> • B: Revision B |
| Tape & Reel | <ul style="list-style-type: none"> • R: Tape & Reel (optional) |

Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFM32PG23 Gecko product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG23 Reference Manual.

A block diagram of the EFM32PG23 family is shown in [Figure 3.1 Detailed EFM32PG23 Block Diagram on page 8](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

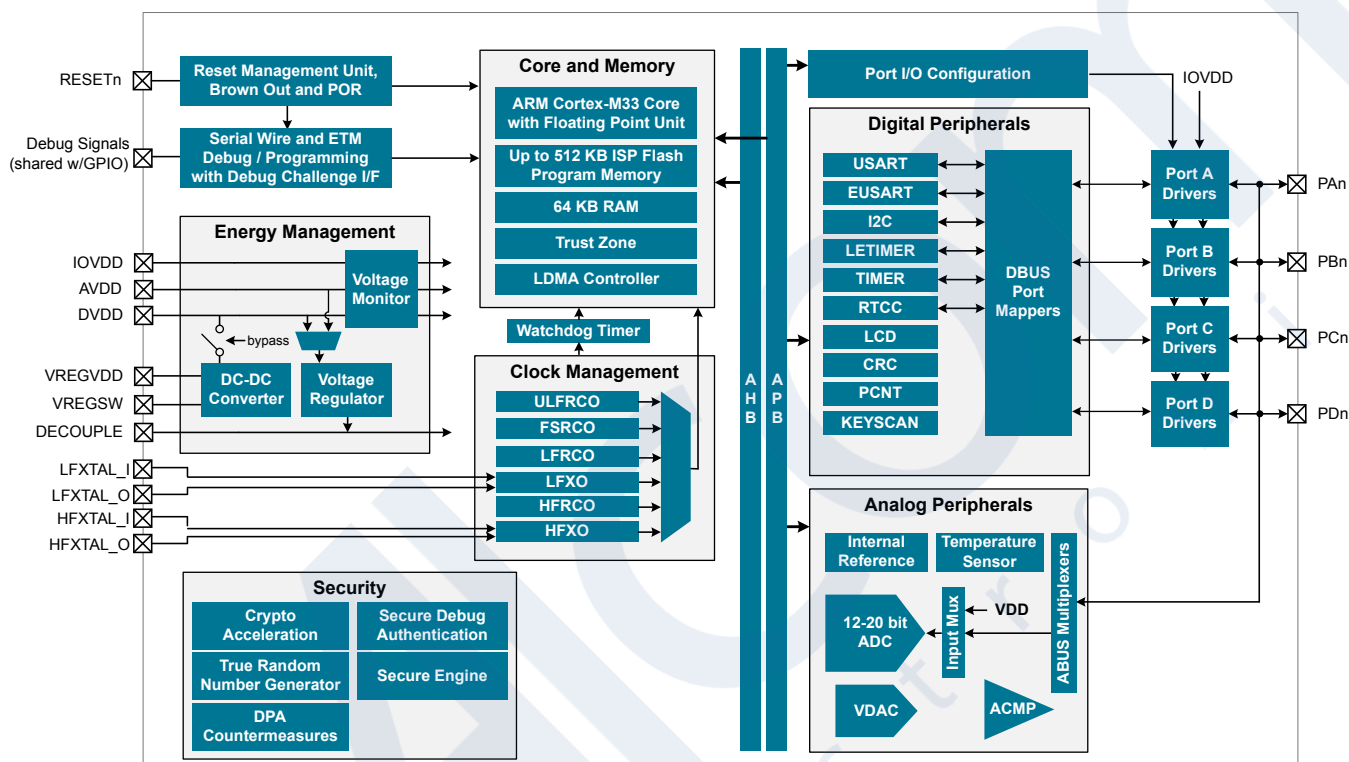


Figure 3.1. Detailed EFM32PG23 Block Diagram

3.2 General Purpose Input/Output (GPIO)

EFM32PG23 has up to 34 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in [6.4 Alternate Function Table](#).

3.3 Keypad Scanner (KEYSCAN)

A low-energy keypad scanner (KEYSCAN) is included, which can scan up to a 6 x 8 matrix of keyboard switches. The KEYSKAN peripheral contains logic for debounce and settling time, allowing it to scan through the switch matrix autonomously in EM0 and EM1, and interrupt the processor when a key press is detected. A wake-on-keypress feature is also supported, allowing for the detection of any key press down to EM3.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32PG23. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32PG23 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See [3.13 Configuration Summary](#) for information on the feature set of each timer.

3.5.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.5.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1 the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.6.3 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Note that not all instances of I²C are available in all energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.6.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Secure Vault Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFM32PG23 family includes devices with Secure Vault High and Secure Vault Mid capabilities, which are summarized in the table below.

Table 3.1. Secure Vault Features

| Feature | Secure Vault Mid | Secure Vault High |
|---|--|--|
| True Random Number Generator (TRNG) | Yes | Yes |
| Secure Boot with Root of Trust and Secure Loader (RTSL) | Yes | Yes |
| Secure Debug with Lock/Unlock | Yes | Yes |
| DPA Countermeasures | Yes | Yes |
| Anti-Tamper | | Yes |
| Secure Attestation | | Yes |
| Secure Key Management | | Yes |
| Symmetric Encryption | <ul style="list-style-type: none"> AES 128 / 192 / 256 bit <ul style="list-style-type: none"> ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC | <ul style="list-style-type: none"> AES 128 / 192 / 256 bit <ul style="list-style-type: none"> ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC ChaCha20 |
| Public Key Encryption - ECDSA / ECDH / EdDSA | <ul style="list-style-type: none"> p192 and p256 | <ul style="list-style-type: none"> p192, p256, p384 and p521 Curve25519 (ECDH) Ed25519 (EdDSA) |
| Key Derivation | <ul style="list-style-type: none"> ECJ-PAKE p192 and p256 | <ul style="list-style-type: none"> ECJ-PAKE p192, p256, p384, and p521 PBKDF2 HKDF |
| Hashes | <ul style="list-style-type: none"> SHA-1 SHA-2/256 | <ul style="list-style-type: none"> SHA-1 SHA-2 256, 384, and 512 Poly1305 |

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see *AN1218: Series 2 Secure Boot with RTSL*.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see *AN1190: Series 2 Secure Debug*.

3.7.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.7.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.7.7 Anti-Tamper

Secure Vault High devices provide internal tamper monitoring the system such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as case tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see *AN1247: Anti-Tamper Protection Configuration and Use*.

3.7.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see *AN1268: Authenticating Silicon Labs Devices Using Device Certificates*.

3.8 Analog

3.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. Flexible controls allow fine-tuned performance and speed to meet the needs of a wide variety of applications. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

The IADC supports three operational modes:

- Normal Mode (all devices): Flexible speed and performance, 12-16 bits output resolution
 - 11.7 bits ENOB performance at 1 Msps (OSR = 2)
 - 14.3 bits ENOB performance at 76.9 ksps (OSR = 32)
- High Speed Mode (select devices): Doubles output speed of Normal mode with similar performance, 12-16 bits output resolution
 - 11.7 bits ENOB performance at 2 Msps (OSR = 2)
 - 14.3 bits ENOB performance at 153.8 ksps (OSR = 32)
- High Accuracy Mode (select devices): Optimized for low-rate, high performance applications, with 20 bit output resolution
 - 16 bits ENOB performance at 3.8 ksps (OSR = 256)
 - 15 bits ENOB performance at 15.3 ksps (OSR = 64)

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.4 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD with up to 4x20 segments. A voltage boost function enables it to provide the LCD with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD peripheral supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Power

The EFM32PG23 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32PG23 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.9.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.9.2 Voltage Scaling

The EFM32PG23 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.9.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, provides high efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 60 mA for device operation. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

3.9.4 Power Domains

Peripherals may exist on several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

Note: Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2 Peripheral Power Subdomains on page 16 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 3.2. Peripheral Power Subdomains

| Always On in EM2/EM3 | | Selectively On in EM2/3 | | | |
|----------------------|--------|-------------------------|-------------------|-------------------|---------|
| PDHV ¹ | PD0A | PD0B ² | PD0C ² | PD0D ² | PD0E |
| LFRCO | SYSRTC | LETIMER0 | HFRCOEM23 | DEBUG | GPIO |
| LFXO | FSRCO | IADC0 | HFXO | WDOG0 | KEYSCAN |
| BURTC | LCD | PCNT0 | | WDOG1 | PRS |
| ULFRCO | | ACMP0 | | EUSART0 | |
| | | ACMP1 | | I2C0 | |
| | | LESENSE | | | |
| | | VDAC0 | | | |

Note:

1. Peripherals on PDHV are also available in EM4.
2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32PG23. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFM32PG23 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

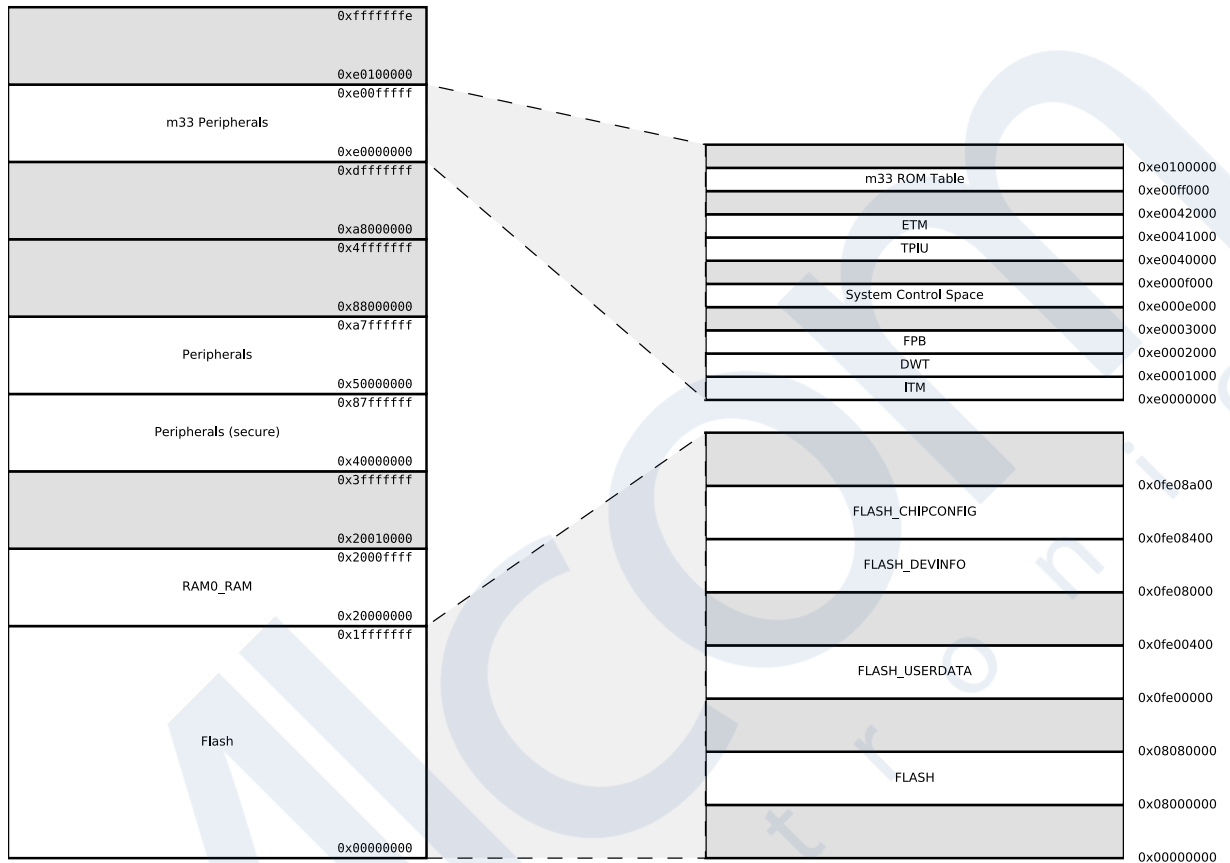


Figure 3.2. EFM32PG23 Memory Map — Core Peripherals and Code Space

3.13 Configuration Summary

The features of the EFM32PG23 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

| Module | Lowest Energy Mode | Configuration |
|---|--|--------------------------|
| I2C0 | EM2/EM3 ¹ | |
| I2C1 | EM1 | |
| IADC0 | EM2/EM3 | |
| LETIMER0 | EM2/EM3 ¹ | |
| TIMER0 | EM1 | 32-bit, 3-channels, +DTI |
| TIMER1 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER2 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER3 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER4 | EM1 | 16-bit, 3-channels, +DTI |
| EUSART0 | EM1 - Full high-speed operation, all modes EM2 ¹ - Low-energy UART operation, 9600 Baud EM2 or EM3 ¹ - Low-energy SPI secondary receiver | |
| EUSART1 | EM1 - Full high-speed operation | |
| EUSART2 | EM1 - Full high-speed operation | |
| USART0 | EM1 | +IrDA, +I2S, +SmartCard |
| Note: 1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1. | | |

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A=25\text{ }^\circ\text{C}$ and all supplies at 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFM32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFM32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD and DVDD
 - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD ($VREGVDD \geq DVDD$)
 - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB ($VREGVDD = DVDD$)
- $DVDD \geq DECOUPLE$
- AVDD, IOVDD: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.

4.2 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <https://www.silabs.com/about-us/corporate-responsibility/commitment-to-quality>.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|----------------|------|-----|--------------------------|-------------|
| Storage temperature range | T _{STG} | | -50 | — | +150 | °C |
| Voltage on any supply pin | V _{DDMAX} | | -0.3 | — | 3.8 | V |
| Junction temperature | T _{JMAX} | -I grade | — | — | +125 | °C |
| Voltage ramp rate on any supply pin | V _{DDRAMPMAX} | | — | — | 1.0 | V / μ s |
| Voltage on HFXO pins | V _{HFXOPIN} | | -0.3 | — | 1.2 | V |
| DC voltage on any GPIO pin ¹ | V _{DIGPIN} | | -0.3 | — | V _{IOVDD} + 0.3 | V |
| DC voltage on RESETn pin ² | V _{RESETn} | | -0.3 | — | 3.8 | V |
| Total current into VDD power lines | I _{VDDMAX} | Source | — | — | 200 | mA |
| Total current into VSS ground lines | I _{VSSMAX} | Sink | — | — | 200 | mA |
| Current per I/O pin | I _{IOMAX} | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | I _{IOALLMAX} | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |

Note:

1. When operating as an LCD driver, the output voltage on a GPIO may safely exceed this specification. The pin output voltage may be up to 3.8 V in this case.
2. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------|--|------|-----|------|---------|
| Operating ambient temperature range | T_A | -I temperature grade ¹ | -40 | — | +125 | ° C |
| DVDD supply voltage | V_{DVDD} | EM0/1 | 1.71 | 3.3 | 3.8 | V |
| | | EM2/3/4 ² | 1.71 | 3.3 | 3.8 | V |
| AVDD supply voltage | V_{AVDD} | | 1.71 | 3.3 | 3.8 | V |
| IOVDD operating supply voltage | V_{IOVDD} | | 1.71 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage | $V_{VREGVDD}$ | DCDC in regulation | 2.2 | 3.3 | 3.8 | V |
| | | DCDC in bypass 60 mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.71 | 3.3 | 3.8 | V |
| DECOUPLE output capacitor ³ | $C_{DECOUPLE}$ | 1.0 μ F \pm 10% X8L capacitor used for performance characterization. | 0.75 | 1.0 | 2.75 | μ F |
| HCLK and SYSCLK frequency | f_{HCLK} | VSCALE2, MODE = WS1 | — | — | 80 | MHz |
| | | VSCALE2, MODE = WS0 | — | — | 40 | MHz |
| | | VSCALE1, MODE = WS0 | — | — | 40 | MHz |
| PCLK frequency | f_{PCLK} | VSCALE2 or VSCALE1 | — | — | 40 | MHz |
| EM01 Group A clock frequency | $f_{EM01GRPACLK}$ | VSCALE2 | — | — | 80 | MHz |
| | | VSCALE1 | — | — | 40 | MHz |
| EM01 Group C clock frequency | $f_{EM01GRPCCLK}$ | VSCALE2 | — | — | 80 | MHz |
| | | VSCALE1 | — | — | 40 | MHz |
| External Clock Input | f_{CLKIN} | VSCALE2 or VSCALE1 | — | — | 40 | MHz |
| DPLL Reference Clock | $f_{DPLLREFCLK}$ | VSCALE2 or VSCALE1 | — | — | 40 | MHz |

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. $T_A = T_{JMAX} - (THETA_{JA} \times PowerDissipation)$. Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.

4.4 DC-DC Converter

Test conditions: $L_{DCDC} = 2.2 \mu\text{H}$ (Samsung CIG22H2R2MNE), $C_{DCDC} = 4.7 \mu\text{F}$ (TDK CGA5L3X8R1C475K160AB), $V_{VREGVDD} = 3.3 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|------------|-------|-----|---------------|
| Input voltage range at VREGVDD pin | $V_{VREGVDD}$ | DCDC in regulation, $I_{LOAD} = 60 \text{ mA}$, EM0/EM1 mode | 2.2 | — | 3.8 | V |
| | | DCDC in regulation, $I_{LOAD} = 5 \text{ mA}$, EM0/EM1 or EM2/EM3 mode | 1.8 | — | 3.8 | V |
| | | Bypass Mode, $I_{LOAD} \leq 60 \text{ mA}$ | 1.8 | — | 3.8 | V |
| Regulated output voltage | V_{OUT} | | — | 1.8 | — | V |
| Regulation DC accuracy | ACC_{DC} | $V_{VREGVDD} \geq 2.2 \text{ V}$, Steady state in EM0/EM1 mode or EM2/EM3 mode | -2.5 | — | 4.0 | % |
| Regulation total accuracy | ACC_{TOT} | All error sources (including DC errors, overshoot, undershoot) | -5 | — | 7 | % |
| Steady-state output ripple | V_R | $I_{LOAD} = 20 \text{ mA}$ in EM0/EM1 mode | — | 12 | — | mVpp |
| DC line regulation | V_{REG} | $I_{LOAD} = 60 \text{ mA}$ in EM0/EM1 mode, $V_{VREGVDD} \geq 2.2 \text{ V}$ | — | -2.6 | — | mV/V |
| Efficiency | EFF | Load current between 100 μA and 60 mA in EM0/EM1 mode | — | 90 | — | % |
| | | Load current between 10 μA and 5 mA in EM2/EM3 mode | — | 89 | — | % |
| DC load regulation | I_{REG} | Load current between 100 μA and 60 mA in EM0/EM1 mode | — | -0.08 | — | mV/mA |
| Output load current | I_{LOAD} | EM0/EM1 mode, DCDC in regulation | — | — | 60 | mA |
| | | EM2/EM3 mode, DCDC in regulation | — | — | 5 | mA |
| | | Bypass mode, $1.8 \text{ V} \leq V_{VREGVDD} \leq 3.8 \text{ V}$ | — | — | 60 | mA |
| Nominal output capacitor | C_{DCDC} | 4.7 $\mu\text{F} \pm 10\%$ X7R capacitor used for performance characterization ¹ | — | 4.7 | 10 | μF |
| Nominal inductor | L_{DCDC} | $\pm 20\%$ tolerance | — | 2.2 | — | μH |
| Nominal input capacitor | C_{IN} | | C_{DCDC} | — | — | μF |
| Resistance in bypass mode | R_{BYP} | Bypass switch from VREGVDD to DVDD, $V_{VREGVDD} = 1.8 \text{ V}$ | — | 0.45 | 0.8 | Ω |
| | | Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD} = 1.8 \text{ V}$ | — | 0.6 | 0.9 | Ω |
| Supply monitor threshold programming range | V_{CMP_RNG} | Programmable in 0.1 V steps | 2 | — | 2.3 | V |
| Supply monitor threshold accuracy | V_{CMP_ACC} | Supply falling edge trip point | -5 | — | 5 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|------------------|---|-----|-----|-----|---------|
| Supply monitor threshold hysteresis | V_{CMP_HYST} | Positive hysteresis on the supply rising edge referred to the falling edge trip point | — | 4 | — | % |
| Supply monitor response time | t_{CMP_DELAY} | Supply falling edge at -100 mV / μ s | — | 0.6 | — | μ s |

Note:

1. TDK CGA5L3X8R1C475K160AB used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 3.6 μ F.

4.5 Thermal Characteristics

Table 4.4. Thermal Characteristics

| Package | Board | Parameter | Symbol | Test Condition | Value | Unit |
|------------------|--|--|---------------|--|-------|----------------|
| 40QFN (5x5mm) | JEDEC - High Thermal Cond. (2s2p) ¹ | Thermal Resistance, Junction to Ambient | Θ_{JA} | Still Air | 29.2 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Board | Θ_{JB} | | 15.2 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Top Center | Ψ_{JT} | | 0.3 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Board | Ψ_{JB} | | 11.2 | $^{\circ}$ C/W |
| | No Board | Thermal Resistance, Junction to Case | Θ_{JC} | Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow. | 24.6 | $^{\circ}$ C/W |
| 48QFN (6x6mm) | JEDEC - High Thermal Cond. (2s2p) ¹ | Thermal Resistance, Junction to Ambient | Θ_{JA} | Still Air | 27.7 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Board | Θ_{JB} | | 14.6 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Top Center | Ψ_{JT} | | 0.69 | $^{\circ}$ C/W |
| | | Thermal Resistance, Junction to Board | Ψ_{JB} | | 11.85 | $^{\circ}$ C/W |
| | No Board | Thermal Resistance, Junction to Case | Θ_{JC} | Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow. | 23.0 | $^{\circ}$ C/W |

Note:

1. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.

4.6 Current Consumption

4.6.1 MCU current consumption using DC-DC at 3.3 V input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.3 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption using DC-DC at 3.3 V input

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 80 MHz HFRCO, CPU running Prime from flash, VSCALE2 | — | 23 | — | μA/MHz |
| | | 80 MHz HFRCO, CPU running while loop from flash, VSCALE2 | — | 21 | — | μA/MHz |
| | | 80 MHz HFRCO, CPU running CoreMark loop from flash, VSCALE2 | — | 31 | — | μA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 27 | — | μA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 26 | — | μA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 36 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 22 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 24 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 29 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 206 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 80 MHz HFRCO, VSCALE2 | — | 11 | — | μA/MHz |
| | | 39 MHz crystal | — | 18 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 14 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 16 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 21 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 197 | — | μA/MHz |
| Current consumption in EM2 mode, VSCALE0 | I _{EM2_VS} | 64 kB RAM retention, RTC running from LFXO | — | 1.33 | — | μA |
| | | 64 kB RAM retention, RTC running from LFRCO | — | 1.33 | — | μA |
| | | 16 kB RAM retention, RTC running from LFRCO | — | 1.03 | — | μA |
| | | 16 kB RAM retention, RTC running from LFXO | — | 1.03 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|--|-----|------|-----|------|
| Current consumption in EM3 mode, VSCALE0 | I _{EM3_VS} | 64 kB RAM retention, RTC running from ULFRCO | — | 1.16 | — | μA |
| | | 16 kB RAM retention, RTC running from ULFRCO | — | 0.86 | — | μA |
| Current consumption for retained RAM bank in EM2 or EM3 | I _{RAM} | Per 16 kB RAM bank | — | 0.1 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹ | I _{PD0B_VS} | | — | 0.85 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹ | I _{PD0C_VS} | | — | 0.13 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹ | I _{PD0D_VS} | | — | 0.98 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹ | I _{PD0E_VS} | | — | 0.06 | — | μA |

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.9.4 Power Domains](#) for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

4.6.2 MCU current consumption at 3.3 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 3.3 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU current consumption at 3.3 V

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|---|-----|-----|------|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 80 MHz HFRCO, CPU running Prime from flash, VSCALE2 | — | 37 | — | μA/MHz |
| | | 80 MHz HFRCO, CPU running while loop from flash, VSCALE2 | — | 33 | TBD | μA/MHz |
| | | 80 MHz HFRCO, CPU running CoreMark loop from flash, VSCALE2 | — | 49 | — | μA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 44 | — | μA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 42 | — | μA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 58 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 35 | 56 | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 38 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 46 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 329 | 1100 | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 80 MHz HFRCO, VSCALE2 | — | 18 | TBD | μA/MHz |
| | | 39 MHz crystal | — | 29 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 22 | 42 | μA/MHz |
| | | 26 MHz HFRCO | — | 25 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 33 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 315 | 1086 | μA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|--|-----|------|------|------|
| Current consumption in EM2 mode, VSCALE0 | I _{EM2_VS} | 64 kB RAM retention, RTC running from LFXO | — | 2.1 | — | μA |
| | | 64 kB RAM retention, RTC running from LFRCO | — | 2.1 | TBD | μA |
| | | 16 kB RAM retention, RTC running from LFRCO | — | 1.67 | — | μA |
| | | 16 kB RAM retention, RTC running from LFXO | — | 1.68 | — | μA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained | — | 1.71 | — | μA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained | — | 1.69 | — | μA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained | — | 1.62 | — | μA |
| Current consumption in EM3 mode, VSCALE0 | I _{EM3_VS} | 64 kB RAM retention, RTC running from ULFRCO | — | 1.75 | — | μA |
| | | 16 kB RAM retention, RTC running from ULFRCO | — | 1.34 | TBD | μA |
| Current consumption for retained RAM bank in EM2 or EM3 | I _{RAM} | Per 16 kB RAM bank | — | 0.14 | — | μA |
| Current consumption in EM4 mode | I _{EM4} | No BURTC, no LF oscillator | — | 0.32 | 0.65 | μA |
| | | BURTC with LFXO | — | 0.70 | — | μA |
| Current consumption during reset | I _{RST} | Hard pin reset held | — | 462 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹ | I _{PD0B_VS} | | — | 1.37 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹ | I _{PD0C_VS} | | — | 0.20 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹ | I _{PD0D_VS} | | — | 1.57 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹ | I _{PD0E_VS} | | — | 0.09 | — | μA |

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.9.4 Power Domains](#) for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

4.6.3 MCU current consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU current consumption at 1.8 V

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|---|-----|------|-----|--------|
| Current consumption in EM0 mode with all peripherals disabled | I _{ACTIVE} | 80 MHz HFRCO, CPU running Prime from flash, VSCALE2 | — | 37 | — | μA/MHz |
| | | 80 MHz HFRCO, CPU running while loop from flash, VSCALE2 | — | 33 | — | μA/MHz |
| | | 80 MHz HFRCO, CPU running CoreMark loop from flash, VSCALE2 | — | 49 | — | μA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 44 | — | μA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 42 | — | μA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 58 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 35 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 38 | — | μA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 46 | — | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 323 | — | μA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | I _{EM1} | 80 MHz HFRCO, VSCALE2 | — | 18 | — | μA/MHz |
| | | 39 MHz crystal | — | 29 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 22 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 25 | — | μA/MHz |
| | | 16 MHz HFRCO | — | 32 | — | μA/MHz |
| | | 1 MHz HFRCO | — | 309 | — | μA/MHz |
| Current consumption in EM2 mode, VSCALE0 | I _{EM2_VS} | 64 kB RAM retention, RTC running from LFXO | — | 1.92 | — | μA |
| | | 64 kB RAM retention, RTC running from LFRCO | — | 1.92 | — | μA |
| | | 16 kB RAM retention, RTC running from LFRCO | — | 1.47 | — | μA |
| | | 16 kB RAM retention, RTC running from LFXO | — | 1.5 | — | μA |
| Current consumption in EM3 mode, VSCALE0 | I _{EM3_VS} | 64 kB RAM retention, RTC running from ULFRCO | — | 1.6 | — | μA |
| | | 16 kB RAM retention, RTC running from ULFRCO | — | 1.15 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|----------------------------|-----|------|-----|------|
| Current consumption for retained RAM bank in EM2 or EM3 | I _{RAM} | Per 16 kB RAM bank | — | 0.15 | — | μA |
| Current consumption in EM4 mode | I _{EM4} | No BURTC, no LF oscillator | — | 0.16 | — | μA |
| | | BURTC with LFXO | — | 0.52 | — | μA |
| Current consumption during reset | I _{RST} | Hard pin reset held | — | 384 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹ | I _{PD0B_VS} | | — | 1.38 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹ | I _{PD0C_VS} | | — | 0.21 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹ | I _{PD0D_VS} | | — | 1.59 | — | μA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹ | I _{PD0E_VS} | | — | 0.10 | — | μA |

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.9.4 Power Domains](#) for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

4.7 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz, with the DPLL disabled.

Table 4.8. Wake Up, Entry, and Exit times

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------|---|-----|------|-----|---------|
| WakeupTime from EM1 | t_{EM1_WU} | Code execution from flash | — | 3 | — | HCLKs |
| | | Code execution from RAM | — | 1.43 | — | μ s |
| WakeupTime from EM2 | t_{EM2_WU} | Code execution from flash, No Voltage Scaling | — | 13.7 | — | μ s |
| | | Code execution from RAM, No Voltage Scaling | — | 5.1 | — | μ s |
| | | Voltage scaling up one level ¹ | — | 37.8 | — | μ s |
| | | Voltage scaling up two levels ² | — | 51.0 | — | μ s |
| WakeupTime from EM3 | t_{EM3_WU} | Code execution from flash, No Voltage Scaling | — | 13.7 | — | μ s |
| | | Code execution from RAM, No Voltage Scaling | — | 5.1 | — | μ s |
| | | Voltage scaling up one level ¹ | — | 37.8 | — | μ s |
| | | Voltage scaling up two levels ² | — | 51.0 | — | μ s |
| WakeupTime from EM4 | t_{EM4_WU} | Code execution from flash | — | 31.0 | — | ms |
| Entry time to EM1 | t_{EM1_ENT} | Code execution from flash | — | 1.29 | — | μ s |
| Entry time to EM2 | t_{EM2_ENT} | Code execution from flash | — | 5.9 | — | μ s |
| Entry time to EM3 | t_{EM3_ENT} | Code execution from flash | — | 5.7 | — | μ s |
| Entry time to EM4 | t_{EM4_ENT} | Code execution from flash | — | 10.7 | — | μ s |
| Voltage scaling in time in EM0 ³ | t_{SCALE} | Up from VSCALE1 to VSCALE2 | — | 32 | — | μ s |
| | | Down from VSCALE2 to VSCALE1 | — | 172 | — | μ s |

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.8 Flash Characteristics

Table 4.9. Flash Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|----------------------------------|--------|------|-----|---------|
| Flash Supply voltage during write or erase | V_{FLASH} | | 1.71 | — | 3.8 | V |
| Flash data retention ¹ | RET_{FLASH} | | 10 | — | — | years |
| Flash erase cycles before failure ¹ | EC_{FLASH} | | 10,000 | — | — | cycles |
| Program Time | t_{PROG} | one word (32-bits) | TBD | 43.5 | TBD | μs |
| | | average per word over 128 words | TBD | 10.9 | TBD | μs |
| Page Erase Time ² | t_{PERASE} | | TBD | 12.9 | TBD | ms |
| Mass Erase Time ^{3 4} | t_{MERASE} | 512 kB | TBD | 50.4 | TBD | ms |
| Program Current | I_{WRITE} | $T_A = 25\text{ }^\circ\text{C}$ | — | — | 2.4 | mA |
| Page Erase Current | I_{ERASE} | $T_A = 25\text{ }^\circ\text{C}$ | — | — | 1.9 | mA |
| Mass Erase Current | I_{MERASE} | $T_A = 25\text{ }^\circ\text{C}$ | — | — | 1.9 | mA |

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
- Mass Erase is issued by the CPU and erases all of User space.
- Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

4.9 Oscillators

4.9.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.10. High Frequency Crystal Oscillator

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|----------------------------------|------|------|------|------|
| Crystal Frequency | F _{HFXO} | | 38.0 | 39.0 | 40.0 | MHz |
| Supported range of crystal load capacitance ¹ | C _{L_HFXO} | | — | 10 | — | pF |
| Supported crystal maximum equivalent series resistance (ESR) | ESR _{HFXO} | 39.0 MHz ² | — | — | 60 | Ω |
| Supply Current | I _{HFXO} | | — | 498 | — | μA |
| Startup Time ³ | T _{STARTUP} | 39.0 MHz, C _L = 10 pF | — | 178 | — | μs |
| On-chip tuning cap step size ⁴ | SS _{HFXO} | | — | 0.04 | — | pF |

Note:

1. Total load capacitance as seen by the crystal.
2. The crystal should have a maximum ESR less than or equal to this maximum rating.
3. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
4. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.9.2 Low Frequency Crystal Oscillator

Table 4.11. Low Frequency Crystal Oscillator

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|--|------|--------|------|------------|
| Crystal Frequency | F_{LFXO} | | — | 32.768 | — | kHz |
| Supported Crystal equivalent series resistance (ESR) | ESR_{LFXO} | GAIN = 0 | — | — | 80 | k Ω |
| | | GAIN = 1 to 3 | — | — | 100 | k Ω |
| Supported range of crystal load capacitance ¹ | C_{L_LFXO} | GAIN = 0 | 4 | — | 6 | pF |
| | | GAIN = 1 | 6 | — | 10 | pF |
| | | GAIN = 2 (see note ²) | 10 | — | 12.5 | pF |
| | | GAIN = 3 (see note ²) | 12.5 | — | 18 | pF |
| Current consumption | I_{CL12p5} | ESR = 70 k Ω , C_L = 12.5 pF, GAIN ³ = 2, AGC ⁴ = 1 | — | 290 | — | nA |
| Startup Time | $T_{STARTUP}$ | ESR = 70 k Ω , C_L = 7 pF, GAIN ³ = 1, AGC ⁴ = 1 | — | 52 | — | ms |
| On-chip tuning cap step size | SS_{LFXO} | | — | 0.26 | — | pF |
| On-chip tuning capacitor value at minimum setting ⁵ | C_{LFXO_MIN} | CAPTUNE = 0 | — | 4 | — | pF |
| On-chip tuning capacitor value at maximum setting ⁵ | C_{LFXO_MAX} | CAPTUNE = 0x4F | — | 24.5 | — | pF |

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.9.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.12. High Frequency RC Oscillator (HFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------------|---|-----|-----|-----|--------|
| Frequency Accuracy | F _{HFRCO_ACC} | For all production calibrated frequencies | -3 | — | 3 | % |
| Current consumption on all supplies ¹ | I _{HFRCO} | F _{HFRCO} = 4 MHz | — | 28 | — | μA |
| | | F _{HFRCO} = 5 MHz ² | — | 29 | — | μA |
| | | F _{HFRCO} = 7 MHz | — | 59 | — | μA |
| | | F _{HFRCO} = 10 MHz ² | — | 63 | — | μA |
| | | F _{HFRCO} = 13 MHz | — | 77 | — | μA |
| | | F _{HFRCO} = 16 MHz | — | 87 | — | μA |
| | | F _{HFRCO} = 19 MHz | — | 90 | — | μA |
| | | F _{HFRCO} = 20 MHz ² | — | 107 | — | μA |
| | | F _{HFRCO} = 26 MHz | — | 116 | — | μA |
| | | F _{HFRCO} = 32 MHz | — | 139 | — | μA |
| | | F _{HFRCO} = 38 MHz ³ | — | 170 | — | μA |
| | | F _{HFRCO} = 40 MHz ² | — | 172 | — | μA |
| | | F _{HFRCO} = 48 MHz ³ | — | 207 | — | μA |
| | | F _{HFRCO} = 56 MHz ³ | — | 228 | — | μA |
| F _{HFRCO} = 64 MHz ³ | — | 269 | — | μA | | |
| F _{HFRCO} = 80 MHz ³ | — | 285 | — | μA | | |
| Clock out current for HFRCODPLL ⁴ | I _{CLKOUT_HFRCODPLL} | FORCEEN bit of HFRCO0_CTRL = 1 | — | 3.0 | — | μA/MHz |
| Clock Out current for HFRCOEM23 ⁴ | I _{CLKOUT_HFRCOEM23} | FORCEEN bit of HFRCOEM23_CTRL = 1 | — | 1.6 | — | μA/MHz |
| Startup Time ⁵ | T _{STARTUP} | FREQRANGE = 0 to 7 | — | 1.2 | — | μs |
| | | FREQRANGE = 8 to 15 | — | 0.6 | — | μs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------------------|-------------------------|----------------|------|-----|------|------|
| Band Frequency Limits ⁶ | f _{HFRCO_BAND} | FREQRANGE = 0 | 3.71 | — | 5.24 | MHz |
| | | FREQRANGE = 1 | 4.39 | — | 6.26 | MHz |
| | | FREQRANGE = 2 | 5.25 | — | 7.55 | MHz |
| | | FREQRANGE = 3 | 6.22 | — | 9.01 | MHz |
| | | FREQRANGE = 4 | 7.88 | — | 11.6 | MHz |
| | | FREQRANGE = 6 | 11.5 | — | 17.0 | MHz |
| | | FREQRANGE = 7 | 14.1 | — | 20.9 | MHz |
| | | FREQRANGE = 8 | 16.4 | — | 24.7 | MHz |
| | | FREQRANGE = 9 | 19.8 | — | 30.4 | MHz |
| | | FREQRANGE = 10 | 22.7 | — | 34.9 | MHz |
| | | FREQRANGE = 11 | 28.6 | — | 44.4 | MHz |
| | | FREQRANGE = 12 | 33.0 | — | 51.0 | MHz |
| | | FREQRANGE = 13 | 42.2 | — | 64.6 | MHz |
| | | FREQRANGE = 14 | 48.8 | — | 74.8 | MHz |
| FREQRANGE = 15 | 57.6 | — | 87.4 | MHz | | |

Note:

- Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
- This frequency is calibrated for the HFRCOEM23 only.
- This frequency is calibrated for the HFRCODPLL only.
- When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
- Hardware delay ensures settling to within $\pm 0.5\%$. Hardware also enforces this delay on a band change.
- The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.9.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.13. Fast Start_Up RC Oscillator (FSRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|--------------------|----------------|------|-----|------|------|
| FSRCO frequency | F _{FSRCO} | | 17.2 | 20 | 21.2 | MHz |

4.9.5 Low Frequency RC Oscillator (LFRCO)

Table 4.14. Low Frequency RC Oscillator (LFRCO)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|------------------|--------------------------------|-----|--------|-----|---------|
| Nominal oscillation frequency | F_{LFRCO} | | — | 32.768 | — | kHz |
| Frequency accuracy | F_{LFRCO_ACC} | | -3 | — | 3 | % |
| Frequency calibration step | F_{TRIM_STEP} | Typical trim step at mid-scale | — | 0.33 | — | % |
| Startup time | $t_{STARTUP}$ | | — | 220 | — | μ s |
| Current consumption | I_{LFRCO} | | — | 186 | — | nA |

4.9.6 Ultra Low Frequency RC Oscillator

Table 4.15. Ultra Low Frequency RC Oscillator

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------|--------------|----------------|-------|-----|-------|------|
| Oscillation Frequency | F_{ULFRCO} | | 0.944 | 1.0 | 1.095 | kHz |

4.10 GPIO Pins (3V GPIO pins)

Table 4.16. GPIO Pins (3V GPIO pins)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|------------------------|---|-------------|------|-------------|------|
| Leakage current | I _{LEAK_IO} | MODEx = DISABLED, IOVDD = 1.71 V | — | 1.9 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.3 V | — | 2.5 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, T _A = 125 °C, Pins PA00, PB00-PB01, and PC06-PC09 | — | — | 250 | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, T _A = 125 °C, all other GPIO | — | — | 200 | nA |
| Input low voltage ¹ | V _{IL} | Any GPIO pin | — | — | 0.3*IOVDD | V |
| | | RESETn | — | — | 0.3*DVDD | V |
| Input high voltage ¹ | V _{IH} | Any GPIO pin | 0.7*IOVDD | — | — | V |
| | | RESETn | 0.7*DVDD | — | — | V |
| Hysteresis of input voltage | V _{HYS} | Any GPIO pin | 0.05*IOVDD | — | — | V |
| | | RESETn | 0.05*DVDD | — | — | V |
| Output high voltage | V _{OH} | Sourcing 20mA, IOVDD = 3.3 V | 0.8 * IOVDD | — | — | V |
| | | Sourcing 8mA, IOVDD = 1.71 V | 0.6 * IOVDD | — | — | V |
| Output low voltage | V _{OL} | Sinking 20mA, IOVDD = 3.3 V | — | — | 0.2 * IOVDD | V |
| | | Sinking 8mA, IOVDD = 1.71 V | — | — | 0.4 * IOVDD | V |
| GPIO rise time | T _{GPIO_RISE} | IOVDD = 3.3 V, C _{load} = 50pF, SLEWRATE = 4, 10% to 90% | — | 8.4 | — | ns |
| | | IOVDD = 1.7 V, C _{load} = 50pF, SLEWRATE = 4, 10% to 90% | — | 13 | — | ns |
| GPIO fall time | T _{GPIO_FALL} | IOVDD = 3.3 V, C _{load} = 50pF, SLEWRATE = 4, 90% to 10% | — | 7.1 | — | ns |
| | | IOVDD = 1.7 V, C _{load} = 50pF, SLEWRATE = 4, 90% to 10% | — | 11.9 | — | ns |
| Pull up/down resistance ² | R _{PULL} | Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0. | 33 | 44 | 55 | kΩ |
| | | RESETn pin. Pull-up to DVDD | 33 | 44 | 55 | kΩ |
| Maximum filtered glitch width | T _{GF} | MODE = INPUT, DOUT = 1 | — | 27 | — | ns |
| RESETn low time to ensure pin reset | T _{RESET} | | 100 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD. | | | | | | |
| 2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD. | | | | | | |



4.11 Analog to Digital Converter (IADC)

Table 4.17. Analog to Digital Converter (IADC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|----------------------|---|------------------|-------------------------|------------------|-------|
| Main analog supply | V _{AVDD} | Normal mode | 1.71 | — | 3.8 | V |
| | | High-Speed mode | 1.71 | — | 3.8 | V |
| | | High-Accuracy mode | 1.71 | — | 3.8 | V |
| Maximum Input Range ¹ | V _{IN_MAX} | Maximum allowable input voltage | 0 | — | AVDD | V |
| Full-Scale Voltage | V _{FS} | Voltage required for Full-Scale measurement | — | V _{REF} / Gain | — | V |
| Input Measurement Range | V _{IN} | Differential Mode - Plus and Minus inputs | -V _{FS} | — | +V _{FS} | V |
| | | Single Ended Mode - One input tied to ground | 0 | — | V _{FS} | V |
| Input Sampling Capacitance | C _s | Analog Gain = 1x | — | 1.8 | — | pF |
| | | Analog Gain = 2x | — | 3.6 | — | pF |
| | | Analog Gain = 3x | — | 5.4 | — | pF |
| | | Analog Gain = 4x | — | 7.2 | — | pF |
| | | Analog Gain = 0.5x | — | 0.9 | — | pF |
| ADC clock frequency | f _{ADC_CLK} | Normal mode, Gain = 1x or 0.5x | — | — | 10 | MHz |
| | | Normal mode, Gain = 2x | — | — | 5 | MHz |
| | | Normal mode, Gain = 3x or 4x | — | — | 2.5 | MHz |
| | | High-Speed mode, Gain = 1x or 0.5x | — | — | 20 | MHz |
| | | High-Speed mode, Gain = 2x | — | — | 10 | MHz |
| | | High-Speed mode, Gain = 3x or 4x | — | — | 5 | MHz |
| | | High-Accuracy mode | — | — | 5 | MHz |
| Input sampling frequency | f _s | Normal Mode | — | f _{ADC_CLK} /4 | — | MHz |
| | | High-Speed Mode | — | f _{ADC_CLK} /4 | — | MHz |
| | | High-Accuracy Mode | — | f _{ADC_CLK} /5 | — | MHz |
| Throughput rate | f _{SAMPLE} | Normal mode, f _{CLK} = 10 MHz, OSR = 2 | — | — | 1 | Msp/s |
| | | Normal mode, f _{CLK} = 10 MHz, OSR = 32 | — | — | 76.9 | ksps |
| | | High-Speed mode, f _{CLK} = 20 MHz, OSR = 2 | — | — | 2 | Msp/s |
| | | High-Accuracy mode, f _{CLK} = 5 MHz, OSR = 92 | — | — | 10.7 | ksps |
| | | High-Accuracy mode, f _{CLK} = 5 MHz, OSR = 256 | — | — | 3.88 | ksps |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------|---|------|----------|-----|-------|
| Current from all supplies, Continuous operation | I _{ADC_CONT} | Normal Mode, 1 Msps, OSR = 2, f _{CLK} = 10 MHz | — | 305 | 385 | μA |
| | | High-Speed Mode, 2 Msps, OSR = 2, f _{CLK} = 20 MHz | — | 550 | TBD | μA |
| | | High-Accuracy Mode, 10.7 ksps, OSR = 92, f _{CLK} = 5 MHz | — | 124 | TBD | μA |
| Current in Standby mode. ADC is not functional but can wake up in 1us. | I _{STBY} | Normal mode | — | 17 | — | μA |
| | | High-Speed mode | — | 21 | — | μA |
| | | High-Accuracy mode | — | 10 | — | μA |
| ADC Startup Time | t _{startup} | From power down state | — | 5 | — | μs |
| | | From standby state | — | 1 | — | μs |
| Normal Mode ADC Resolution ² | Resolution | OSR = 2 | — | 12 | — | bits |
| | | OSR = 32 | — | 16 | — | bits |
| High-Speed Mode ADC Resolution ² | Resolution _{HS} | OSR = 2 | — | 12 | — | bits |
| | | OSR = 32 | — | 16 | — | bits |
| High-Accuracy Mode ADC Resolution | Resolution _{HA} | High Accuracy mode. Typical value is for default OSR = 92 for 10.7 ksps, max value is limited by code length. | — | 16 | 20 | bits |
| Differential Nonlinearity | DNL | Normal mode. Differential Input. OSR = 2 (No missing codes) | -1 | +/- 0.25 | 1.5 | LSB12 |
| | | High Speed mode. Differential Input. OSR = 2 | TBD | +/- 0.25 | TBD | LSB12 |
| | | High-Accuracy mode ³ . Differential Input. 10.7 ksps with OSR = 92 | 1 | — | 1 | LSB16 |
| Integral Nonlinearity | INL | Normal mode. Differential Input, OSR = 2 | -2.5 | +/- 0.65 | 2.5 | LSB12 |
| | | High-Speed mode. Differential Input. | TBD | +/- 0.65 | TBD | LSB12 |
| | | High-Accuracy mode ³ . Differential Input. External VREF = 1.25 V. 10.7 ksps with OSR = 92 | — | +/- 0.25 | — | LSB16 |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|---|------|------|-----|------|
| Effective number of bits ⁴ | ENOB | Normal Mode, Differential Input. Gain = 1x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF=1.21V | 10.7 | 11.7 | — | bits |
| | | Normal Mode, Differential Input. Gain = 1x, OSR = 32, $f_{IN} = 2.5$ kHz, Internal VREF = 1.21 V. | — | 13.5 | — | bits |
| | | Normal Mode, Differential Input. Gain = 1x, OSR = 32, $f_{IN} = 2.5$ kHz, External VREF = 1.25 V. | — | 14.3 | — | bits |
| | | High Speed mode. Differential Input. Gain = 1x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF = 1.21 V | TBD | 11.7 | — | bits |
| | | High-Accuracy mode ³ . Differential Input. Gain = 1x, $f_{IN} = 100$ Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | TBD | 15.5 | — | bits |
| | | High-Accuracy mode ³ . Differential Input. Gain = 1x, $f_{IN} = 100$ Hz, External VREF = 1.25 V. 3.88 ksp/s with OSR = 256 | — | 16.1 | — | bits |
| Signal to Noise + Distortion Ratio Normal Mode ⁴ | SNDR | Differential Input. Gain=1x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF=1.21V | 66 | 72.3 | — | dB |
| | | Differential Input. Gain=2x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF=1.21V | — | 72.3 | — | dB |
| | | Differential Input. Gain=4x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF=1.21V | — | 68.8 | — | dB |
| | | Differential Input. Gain=0.5x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF=1.21V | — | 72.5 | — | dB |
| | | Differential Input. Gain = 1x, OSR = 64, $f_{IN} = 1.25$ kHz, Internal VREF = 1.21 V | — | 83.9 | — | dB |
| Signal to Noise + Distortion Ratio High-Speed mode | SNDR _{HS} | High Speed mode. Differential Input. Gain = 1x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF = 1.21 V | TBD | 72.3 | — | dB |
| | | High Speed mode. Differential Input. Gain = 2x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF = 1.21 V | — | 72.3 | — | dB |
| | | High Speed mode. Differential Input. Gain = 4x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF = 1.21 V | — | 68.8 | — | dB |
| | | High Speed mode. Differential Input. Gain = 0.5x, OSR = 2, $f_{IN} = 10$ kHz, Internal VREF = 1.21 V | — | 72.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|-----|-------|-----|------|
| Signal to Noise + Distortion Ratio High-Accuracy mode ³ | SNDR _{HA} | High-Accuracy. Differential Input. Gain = 1x, f_{IN} = 100 Hz, External VREF = 1.25 V. 3.88 ksp/s with OSR = 256 | — | 98.7 | — | dB |
| | | High-Accuracy. Differential Input. Gain = 1x, f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | TBD | 94.8 | — | dB |
| | | High-Accuracy. Differential Input. Gain = 2x, f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | — | 93.5 | — | dB |
| | | High-Accuracy. Differential Input. Gain = 4x, f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | — | 91.0 | — | dB |
| | | High-Accuracy. Differential Input. Gain = 0.5x, f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | — | 94.7 | — | dB |
| Total Harmonic Distortion | THD | Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V | — | -80.8 | -70 | dB |
| | | High Speed mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V | — | -80.8 | TBD | dB |
| | | High-Accuracy mode ³ , Differential Input. f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | — | -110 | TBD | dB |
| Spurious-Free Dynamic Range | SFDR | Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V | 72 | 86.5 | — | dB |
| | | High Speed mode, Differential Input. Gain = 1x, f_{IN} = 10 kHz, Internal VREF = 1.21 V | TBD | 86.5 | — | dB |
| | | High-Accuracy mode ³ , Differential Input. f_{IN} = 100 Hz, External VREF = 1.25 V. 10.7 ksp/s with OSR = 92 | TBD | 118.1 | — | dB |
| Common Mode Rejection Ratio | CMRR | Normal mode. DC to 100 Hz | — | 87.0 | — | dB |
| | | Normal mode. AC high frequency. | — | 68.6 | — | dB |
| | | High-Speed mode. DC to 100 Hz | — | 86.3 | — | dB |
| | | High-Speed mode. AC high frequency. | — | 59.0 | — | dB |
| | | High-Accuracy mode ³ . DC to 100 Hz | — | 93.8 | — | dB |
| | | High Accuracy mode ³ . AC high frequency. | — | 87.0 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|---|------|-------|------|-------|
| Power Supply Rejection Ratio | PSRR | Normal mode. DC to 100 Hz | — | 80.4 | — | dB |
| | | Normal mode. AC high frequency, using internal VBGR | — | 33.4 | — | dB |
| | | Normal mode. AC high frequency, using VREF pad | — | 65.2 | — | dB |
| | | High Speed modes. DC to 100 Hz | — | 79.8 | — | dB |
| | | High-Speed mode. AC high frequency, using internal VBGR | — | 31.0 | — | dB |
| | | High Speed mode. AC high frequency, using VREF pad | — | 65.0 | — | dB |
| | | High Accuracy mode ³ . DC to 100 Hz | — | 124 | — | dB |
| | | High-Accuracy mode ³ . AC high frequency, using external VREF pin. | — | 85.0 | — | dB |
| External reference voltage range ¹ | V _{EVREF} | | 1.0 | — | AVDD | V |
| Offset Error, Normal mode | OFFSET | GAIN = 1 and 0.5, Differential Input | -3 | 0.27 | 3 | LSB12 |
| | | GAIN = 2, Differential Input | -4 | 0.27 | 4 | LSB12 |
| | | GAIN = 3, Differential Input | -4 | 0.25 | 4 | LSB12 |
| | | GAIN = 4, Differential Input | -4 | 0.29 | 4 | LSB12 |
| Offset Error, High-speed mode | OFFSET _{HS} | GAIN = 1 and 0.5, Differential Input | -3 | 0.27 | 3 | LSB12 |
| | | GAIN = 2, Differential Input | -4 | 0.27 | 4 | LSB12 |
| | | GAIN = 3, Differential Input | -4 | 0.25 | 4 | LSB12 |
| | | GAIN = 4, Differential Input | -4 | 0.29 | 4 | LSB12 |
| Offset Error, High-accuracy mode ³ | OFFSET _{HA} | All GAIN settings, Differential Input | TBD | 3 | TBD | LSB16 |
| Gain Error, Normal mode | GE | GAIN = 1 and 0.5, using external VREF, direct mode. | -0.3 | 0.069 | 0.3 | % |
| | | GAIN = 2, using external VREF, direct mode. | -0.4 | 0.151 | 0.4 | % |
| | | GAIN = 3, using external VREF, direct mode. | -0.7 | 0.186 | 0.7 | % |
| | | GAIN = 4, using external VREF, direct mode. | -1.1 | 0.227 | 1.1 | % |
| | | Internal VREF ⁵ , all GAIN settings | -1.5 | 0.023 | 1.5 | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|---|------|-------|-----|------|
| Gain Error, High-speed mode | GE _{HS} | GAIN = 1 and 0.5, using external VREF, direct mode. | -0.3 | 0.069 | 0.3 | % |
| | | GAIN = 2, using external VREF, direct mode. | -0.4 | 0.151 | 0.4 | % |
| | | GAIN = 3, using external VREF, direct mode. | -0.7 | 0.186 | 0.7 | % |
| | | GAIN = 4, using external VREF, direct mode. | -1.1 | 0.227 | 1.1 | % |
| | | Internal VREF ⁵ , all GAIN settings | -1.5 | 0.023 | 1.5 | % |
| Gain Error, High-accuracy mode ³ | GE _{HA} | GAIN = 1 and 0.5, using external VREF, direct mode. | TBD | 0.06 | TBD | % |
| | | GAIN = 2, using external VREF, direct mode. | TBD | 0.16 | TBD | % |
| | | GAIN = 4, using external VREF, direct mode. | TBD | 0.25 | TBD | % |
| Internal Reference voltage | V _{IVREF} | | — | 1.21 | — | V |

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR = 2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. High-Accuracy mode performance specifications are tested with inputs applied to the dedicated AIN pins.
4. The relationship between ENOB and SNDR is specified according to the equation: $ENOB = (SNDR - 1.76) / 6.02$.
5. Includes error from internal VREF drift.

4.12 Analog Comparator (ACMP)

Table 4.18. Analog Comparator (ACMP)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|---|------|------|------|------|
| ACMP Supply current | I_{ACMP} | BIAS = 2 ¹ , HYST = DISABLED | — | 520 | — | nA |
| | | BIAS = 3 ¹ , HYST = DISABLED | — | 1.9 | — | μA |
| | | BIAS = 4, HYST = DISABLED | — | 5.4 | — | μA |
| | | BIAS = 5, HYST = DISABLED | — | 10.7 | — | μA |
| | | BIAS = 6, HYST = DISABLED | — | 27 | — | μA |
| | | BIAS = 7, HYST = DISABLED | — | 50 | 100 | μA |
| ACMP Supply current with Hysteresis | I_{ACMP_WHYS} | BIAS = 2 ¹ , HYST = SYM30MV | — | 780 | — | nA |
| | | BIAS = 3 ¹ , HYST = SYM30MV | — | 2.8 | — | μA |
| | | BIAS = 4, HYST = SYM30MV | — | 7.3 | — | μA |
| | | BIAS = 5, HYST = SYM30MV | — | 15 | — | μA |
| | | BIAS = 6, HYST = SYM30MV | — | 38 | — | μA |
| | | BIAS = 7, HYST = SYM30MV | — | 71 | — | μA |
| Current consumption from VREFDIV in continuous mode | $I_{VREFDIV}$ | NEGSEL = VREFDIVAVDD | — | 3.4 | — | μA |
| | | NEGSEL = VREFDIV1V25 | — | 4.2 | — | μA |
| | | NEGSEL = VREFDIV2V5 | — | 6.9 | — | μA |
| Current consumption from VREFDIV in sample/hold mode | $I_{VREFDIV_SH}$ | NEGSEL = VREFDIV2V5LP | — | 76 | — | nA |
| | | NEGSEL = VREFDIV1V25LP | — | 73 | — | nA |
| | | NEGSEL = VREFDIVAVDDL | — | 72 | — | nA |
| Current consumption from VSENSEDIV in continuous mode | $I_{VSENSEDIV}$ | NEGSEL = VSENSE01DIV4 | — | 1.8 | — | μA |
| Current consumption from VSENSEDIV in sample/hold mode | $I_{VSENSEDIV_SH}$ | NEGSEL = VSENSE01DIV4LP | — | 58 | — | nA |
| Hysteresis (BIAS = 4) | V_{HYST} | HYST = SYM10MV ² | — | 18 | — | mV |
| | | HYST = SYM20MV ² | — | 34 | — | mV |
| | | HYST = SYM30MV ² | — | 48 | — | mV |
| Reference Voltage | $V_{ACMPREF}$ | Internal 1.25 V Reference | 1.19 | 1.25 | 1.31 | V |
| | | Internal 2.5 V Reference | 2.34 | 2.5 | 2.75 | V |
| Input offset voltage | V_{OFFSET} | BIAS = 2, VCM = 0.15 to AVDD - 0.15 | -25 | — | 25 | mV |
| | | BIAS = 4, VCM = 0.15 to AVDD - 0.15 | -25 | — | 25 | mV |
| | | BIAS = 7, VCM = 0.15 to AVDD - 0.15 | -30 | — | 30 | mV |
| Input Range | V_{IN} | Input Voltage Range | 0 | — | AVDD | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------|----------------|-----|------|-----|------|
| Comparator delay with 100 mV overdrive | T _{DELAY} | BIAS = 2 | — | 0.87 | — | μs |
| | | BIAS = 3 | — | 0.28 | — | μs |
| | | BIAS = 4 | — | 160 | — | ns |
| | | BIAS = 5 | — | 94 | — | ns |
| | | BIAS = 6 | — | 60 | — | ns |
| | | BIAS = 7 | — | 49 | — | ns |
| Capacitive Sense Oscillator Resistance | R _{CSRESSEL} | CSRESSEL = 0 | — | 14 | — | kΩ |
| | | CSRESSEL = 1 | — | 24 | — | kΩ |
| | | CSRESSEL = 2 | — | 43 | — | kΩ |
| | | CSRESSEL = 3 | — | 60 | — | kΩ |
| | | CSRESSEL = 4 | — | 80 | — | kΩ |
| | | CSRESSEL = 5 | — | 99 | — | kΩ |
| | | CSRESSEL = 6 | — | 120 | — | kΩ |

Note:

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 μA of supply current is required.
2. V_{CM} = 1.25 V

4.13 Digital to Analog Converter (VDAC)

Table 4.19. Digital to Analog Converter (VDAC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|------|-------|-------|------------|
| Output voltage | V_{DACOUT} | | 0 | — | VREF | V |
| Output Current | I_{DACOUT} | | -10 | — | 10 | mA |
| DAC clock frequency | f_{DAC} | | — | — | 1 | MHz |
| Sample rate | SR_{DAC} | $f_{DAC} = f_{DAC(max)}$ | — | — | 500 | ksps |
| Resolution | $N_{RESOLUTION}$ | | — | 12 | — | bits |
| Load Capacitance ¹ | C_{LOAD} | High Power and Lower Power Modes | — | — | 50 | pF |
| | | High Capacitance Load Mode | 25 | — | — | nF |
| Load Resistance | R_{LOAD} | | 5 | — | — | k Ω |
| Current consumption, Dynamic, 500 ksps, 1 channel active ² | $I_{DAC_1_500}$ | High Power Mode | — | 255 | — | μ A |
| | | Low Power Mode | — | 150 | — | μ A |
| Current consumption, Dynamic, 500 ksps, 2 channels active ² | $I_{DAC_2_500}$ | High Power Mode | — | 421 | — | μ A |
| | | Low Power Mode | — | 216 | — | μ A |
| Current consumption, Static, 1 channel active ³ | $I_{DAC_1_STAT}$ | High Power Mode | — | 136 | — | μ A |
| | | Low Power Mode | — | 31 | — | μ A |
| | | High Capacitance Mode | — | 44 | — | μ A |
| Current consumption, Static, 2 channels active ³ | $I_{DAC_2_STAT}$ | High Power Mode | — | 263 | TBD | μ A |
| | | Low Power Mode | — | 53 | TBD | μ A |
| | | High Capacitance Mode | — | 78 | — | μ A |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% full scale output, settling to 10 LSB | — | 4.5 | 4.9 | μ s |
| Settling time | $t_{DACSETTLE}$ | High Power Mode, 25% to 75% of full scale, settling to 10 LSB | — | 1.1 | 1.6 | μ s |
| | | Low Power Mode, 25% to 75% of full scale, settling to 1% | — | 2.7 | — | μ s |
| Output impedance | R_{OUT} | Main Output, High Power Mode | — | 2.3 | — | Ω |
| | | Main Output, Low Power Mode | — | 3.2 | — | Ω |
| Power supply rejection ratio ⁴ | PSRR | $V_{out} = 50\%$ full scale, DC output | — | 72 | — | dB |
| Signal to noise and distortion ratio | SNDR _{DAC} | High Power mode, 500 ksps, internal 2.5V reference, 1 kHz sine wave input, BW limited to 250 kHz | 61 | 64.8 | — | dB |
| | | High Power mode, 500 ksps, internal 2.5V reference, 1 kHz sine wave input, BW limited to 22 kHz | 61.8 | 67.4 | — | dB |
| Total Harmonic Distortion | THD | High Power Mode, internal 2.5V reference, 1 kHz sine wave input | — | -68.8 | -62.4 | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|--|------|-----|--------|------|
| Integral Non-Linearity | INL _{DAC} | High Power Mode, Across full temperature range | -5 | — | 5 | LSB |
| Differential Non-Linearity ⁵ | DNL _{DAC} | High Power Mode, Across full temperature range | -1 | — | 1.3 | LSB |
| Offset error ⁶ | V _{OFFSET} | High Power mode | -15 | — | 15 | mV |
| | | Low Power Mode | -25 | — | 25 | mV |
| | | High Capacitance Load mode | -35 | — | 35 | mV |
| Gain error ⁶ | V _{GAIN} | 1.25 V internal reference | -1.5 | — | 1.5 | % |
| | | 2.5 V internal reference | -2 | — | 2 | % |
| | | External Reference | -0.6 | — | 0.6 | % |
| External Reference Voltage ⁷ | V _{EXTREF} | | 1.1 | — | V_AVDD | V |

Note:

1. Main outputs only.
2. Dynamic current specifications are for VDAC circuitry operating at max clock frequency with the output updated at the specified sampling rate using DMA transfers. Output is a 1 kHz sine wave from 10% to 90% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
3. Static current specifications are for VDAC circuitry operating after a one-time update to a static output at 50% full scale, with the VDAC APB clock disabled. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
7. External reference voltage on VREFP pin or PA00 when used for VREFP

4.14 LCD

Table 4.20. LCD

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------|--|------|--------|-----------------------------|------|
| LCD Temperature Range | T _{RANGE} | | -40 | — | 105 | °C |
| Frame rate | f _{LCDFR} | | 30 | — | 100 | Hz |
| LCD supply range ^{1 2} | V _{LCDIN} | | 1.71 | — | 3.8 | V |
| LCD output voltage range ² | V _{LCD} | Step-down mode with external LCD capacitor | 2.4 | — | V _{LCDIN} | V |
| | | Charge pump mode with external LCD capacitor | 2.4 | — | 1.9 * V _{LCDIN} | V |
| Contrast control step size | STEP _{CONTRAST} | Charge pump or Step-down mode | — | 50 | — | mV |
| Contrast control step accuracy ³ | ACC _{CONTRAST} | | — | +/-1.5 | — | % |

Note:

1. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.
2. V_{LCDIN} and V_{LCD} should be a maximum of 2 V above V_{IOVDD} to avoid additional leakage through the GPIO pins used for LCD functions.
3. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

4.15 Temperature Sensor

Table 4.21. Temperature Sensor

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|--|-----|--------|-----|------|
| Temperature sensor range ¹ | T _{RANGE} | | -40 | — | 125 | °C |
| Temperature sensor resolution | T _{RESOLUTION} | | — | 0.25 | — | °C |
| Measurement noise (RMS) | T _{NOISE} | Single measurement | — | 0.6 | — | °C |
| | | 16-sample average (TEMPAVG- NUM = 0) | — | 0.17 | — | °C |
| | | 64-sample average (TEMPAVG- NUM = 1) | — | 0.12 | — | °C |
| Temperature offset | T _{OFF} | Mean error of uncorrected output across full temperature range | — | 3.7 | — | °C |
| Temperature sensor accuracy ^{2 3} | T _{ACC} | Direct output accuracy after mean error (T _{OFF}) removed | — | +/-3 | — | °C |
| | | After linearization in software, no calibration | — | +/-2 | — | °C |
| | | After linearization in software, with single-temperature calibration at 25 °C ⁴ | — | +/-1.5 | — | °C |
| Measurement interval | t _{MEAS} | | — | 250 | — | ms |

Note:

1. The sensor reports absolute die temperature in °K. All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.16 Brown Out Detectors

4.16.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at $T_A = 25\text{ }^\circ\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.22. DVDD BOD

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------|-------------------------|---|------|------|------|---------|
| BOD threshold | V_{DVDD_BOD} | Supply Rising | — | 1.67 | 1.71 | V |
| | | Supply Falling | 1.62 | 1.65 | — | V |
| BOD response time | $t_{DVDD_BOD_DELAY}$ | Supply dropping at 100 mV/ μ s slew rate ¹ | — | 0.95 | — | μ s |
| BOD hysteresis | $V_{DVDD_BOD_HYS_T}$ | | — | 22 | — | mV |

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.16.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.23. LE DVDD BOD

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------|----------------------------|---|-----|-----|------|---------|
| BOD threshold | $V_{DVDD_LE_BOD}$ | Supply Falling | 1.5 | — | 1.71 | V |
| BOD response time | $t_{DVDD_LE_BOD_DELAY}$ | Supply dropping at 2 mV/ μ s slew rate ¹ | — | 50 | — | μ s |
| BOD hysteresis | $V_{DVDD_LE_BOD_HYST}$ | | — | 20 | — | mV |

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.16.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.24. AVDD and IOVDD BODs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------|------------------|---|------|-----|------|---------|
| BOD threshold | V_{BOD} | Supply falling | 1.45 | — | 1.71 | V |
| BOD response time | t_{BOD_DELAY} | Supply dropping at 2 mV/ μ s slew rate ¹ | — | 50 | — | μ s |
| BOD hysteresis | V_{BOD_HYST} | | — | 20 | — | mV |

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.17 Pulse Counter

Table 4.25. Pulse Counter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|--|-----|-----|-----|------|
| Input frequency | F_{IN} | Asynchronous Single and Quadrature Modes | — | — | 1.0 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |
| Setup time in asynchronous external clock mode | $t_{SU_S1N_S0N}$ | S1N (data) to S0N (clock) | 50 | — | — | ns |
| Hold time in asynchronous external clock mode | $t_{HD_S0N_S1N}$ | S0N (clock) to S1N (data) | 50 | — | — | ns |

4.18 USART SPI Main Timing

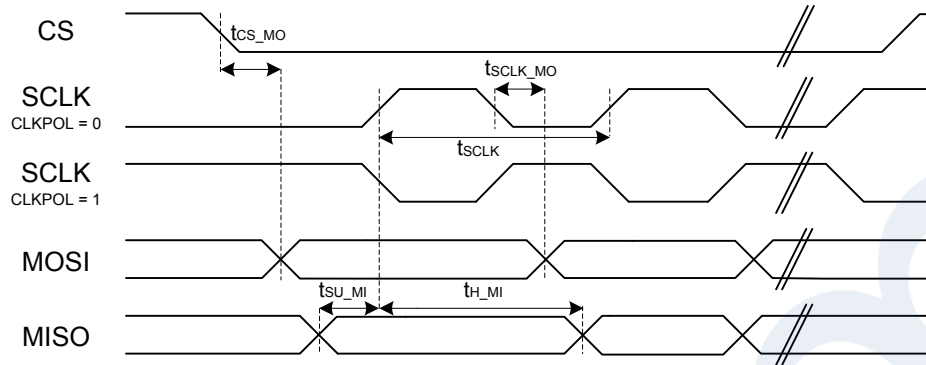


Figure 4.1. SPI Main Timing (SMSDELAY = 0)

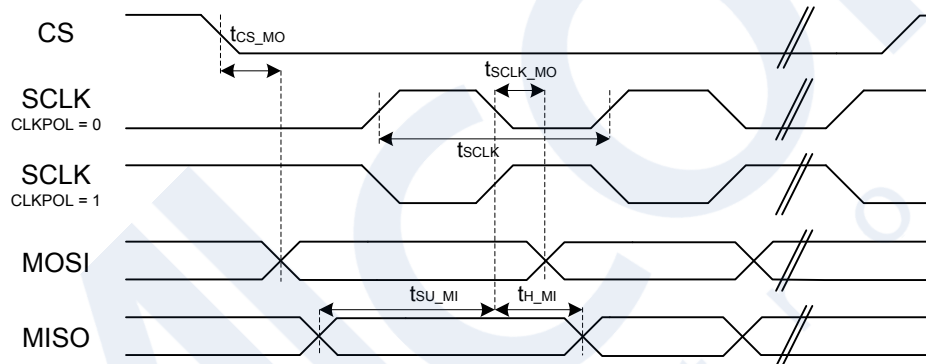


Figure 4.2. SPI Main Timing (SMSDELAY = 1)

4.18.1 USART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.26. USART SPI Main Interface Timing, Voltage Scaling = VSCALE2

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------------|----------------|---------------------|-----|-----|------|
| SCLK period ^{1 2 3} | t _{SCLK} | | 2*t _{PCLK} | — | — | ns |
| CS to MOSI ^{1 2} | t _{CS_MO} | | -17 | — | 22 | ns |
| SCLK to MOSI ^{1 2} | t _{SCLK_MO} | | -12 | — | 12 | ns |
| MISO setup time ^{1 2} | t _{SU_MI} | IOVDD = 1.62 V | 39 | — | — | ns |
| | | IOVDD = 3.3 V | 28 | — | — | ns |
| MISO hold time ^{1 2} | t _{H_MI} | | -10 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.18.2 USART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.27. USART SPI Main Interface Timing, Voltage Scaling = VSCALE1

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------------|----------------|---------------------|-----|-----|------|
| SCLK period ^{1 2 3} | t _{SCLK} | | 2*t _{PCLK} | — | — | ns |
| CS to MOSI ^{1 2} | t _{CS_MO} | | -24 | — | 32 | ns |
| SCLK to MOSI ^{1 2} | t _{SCLK_MO} | | -12 | — | 20 | ns |
| MISO setup time ^{1 2} | t _{SU_MI} | IOVDD = 1.62 V | 47 | — | — | ns |
| | | IOVDD = 3.3 V | 39 | — | — | ns |
| MISO hold time ^{1 2} | t _{H_MI} | | -11 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD}.
3. t_{PCLK} is one period of the selected PCLK.

4.19 USART SPI Secondary Timing

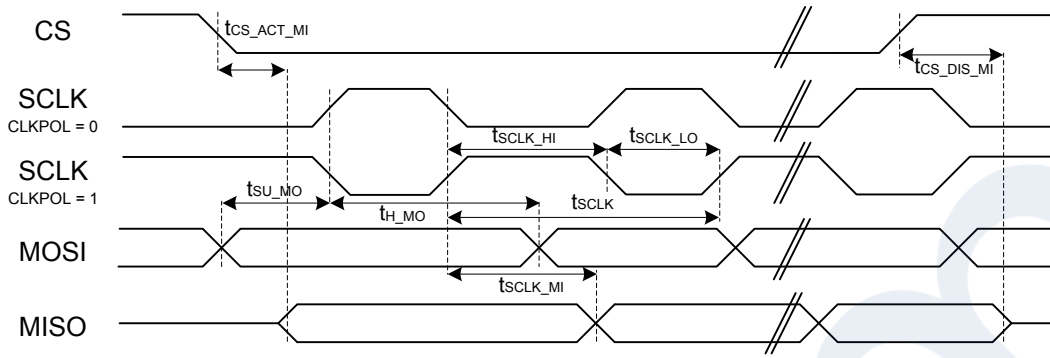


Figure 4.3. SPI Secondary Timing (SSSEARLY = 0)

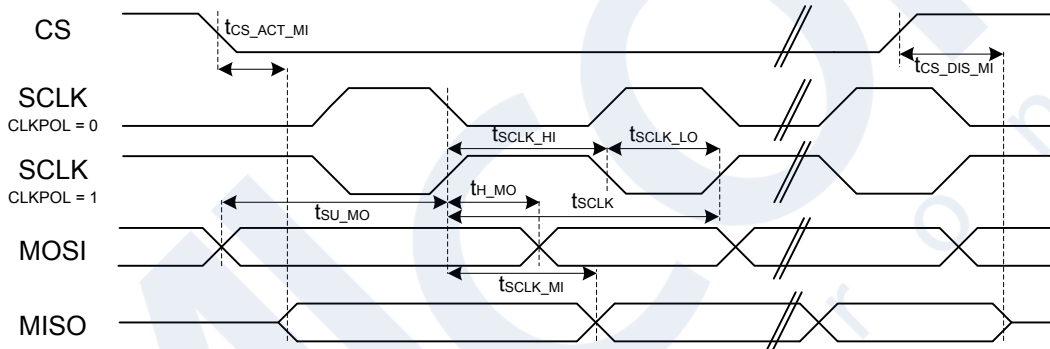


Figure 4.4. SPI Secondary Timing (SSSEARLY = 1)

4.19.1 USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.28. USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------------------|----------------|-------------------------------|-----|-------------------------------|------|
| SCLK period ^{1 2 3} | t _{SCLK} | | 6*t _{PCLK} | — | — | ns |
| SCLK high time ^{1 2 3} | t _{SCLK_HI} | | 2.5*t _{PCLK} | — | — | ns |
| SCLK low time ^{1 2 3} | t _{SCLK_LO} | | 2.5*t _{PCLK} | — | — | ns |
| CS active to MISO ^{1 2} | t _{CS_ACT_MI} | | 18 | — | 75 | ns |
| CS disable to MISO ^{1 2} | t _{CS_DIS_MI} | | 16 | — | 66 | ns |
| MOSI setup time ^{1 2} | t _{SU_MO} | | 6 | — | — | ns |
| MOSI hold time ^{1 2 3} | t _{H_MO} | | 5 | — | — | ns |
| SCLK to MISO ^{1 2 3} | t _{SCLK_MI} | | 14 + 1.5*t _{PCLK} | — | 29 + 2.5*t _{PCLK} | ns |

Note:

- Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
- Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
- t_{PCLK} is one period of the selected PCLK.

4.19.2 USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.29. USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------------------|----------------|-------------------------------|-----|-------------------------------|------|
| SCLK period ^{1 2 3} | t _{SCLK} | | 6*t _{PCLK} | — | — | ns |
| SCLK high time ^{1 2 3} | t _{SCLK_HI} | | 2.5*t _{PCLK} | — | — | ns |
| SCLK low time ^{1 2 3} | t _{SCLK_LO} | | 2.5*t _{PCLK} | — | — | ns |
| CS active to MISO ^{1 2} | t _{CS_ACT_MI} | | 23 | — | 102 | ns |
| CS disable to MISO ^{1 2} | t _{CS_DIS_MI} | | 22 | — | 93 | ns |
| MOSI setup time ^{1 2} | t _{SU_MO} | | 9 | — | — | ns |
| MOSI hold time ^{1 2 3} | t _{H_MO} | | 9 | — | — | ns |
| SCLK to MISO ^{1 2 3} | t _{SCLK_MI} | | 18 + 1.5*t _{PCLK} | — | 36 + 2.5*t _{PCLK} | ns |

Note:

- Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
- Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
- t_{PCLK} is one period of the selected PCLK.

4.20 EUSART SPI Main Timing

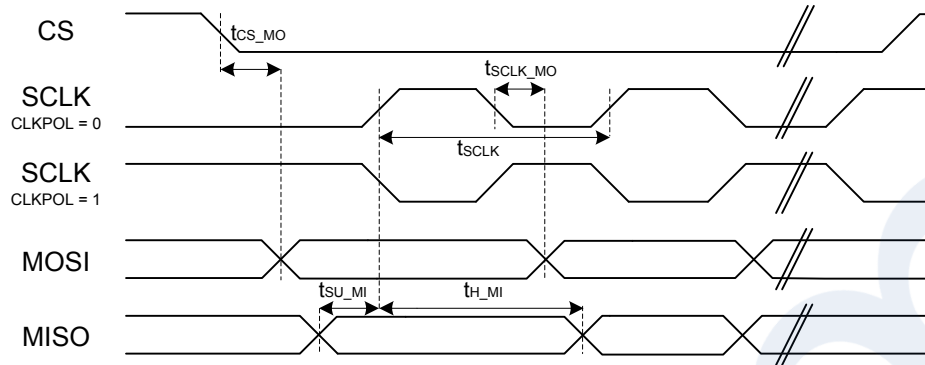


Figure 4.5. SPI Main Timing

4.20.1 EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.30. EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE2

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------|----------------|-----------|-----|-----|------|
| SCLK period ^{1 2 3} | t_{SCLK} | | t_{CLK} | — | — | ns |
| CS to MOSI ^{1 2} | t_{CS_MO} | | -10 | — | 8 | ns |
| SCLK to MOSI ^{1 2} | t_{SCLK_MO} | | -3 | — | 8 | ns |
| MISO setup time ^{1 2} | t_{SU_MI} | | 7 | — | — | ns |
| MISO hold time ^{1 2} | t_{H_MI} | | 3 | — | — | ns |

Note:

- Applies for both CLKPHA = 0 and CLKPHA = 1.
- Measurement done with 15 pF output loading at 10% and 90% of V_{DD} .
- t_{CLK} is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.20.2 EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.31. EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE1

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------------|----------------|------------------|-----|-----|------|
| SCLK period ^{1 2 3} | t _{SCLK} | | t _{CLK} | — | — | ns |
| CS to MOSI ^{1 2} | t _{CS_MO} | | -18 | — | 15 | ns |
| SCLK to MOSI ^{1 2} | t _{SCLK_MO} | | -4 | — | 13 | ns |
| MISO setup time ^{1 2} | t _{SU_MI} | | 12 | — | — | ns |
| MISO hold time ^{1 2} | t _{H_MI} | | 3 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD}.
3. t_{CLK} is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.21 EUSART SPI Secondary Timing

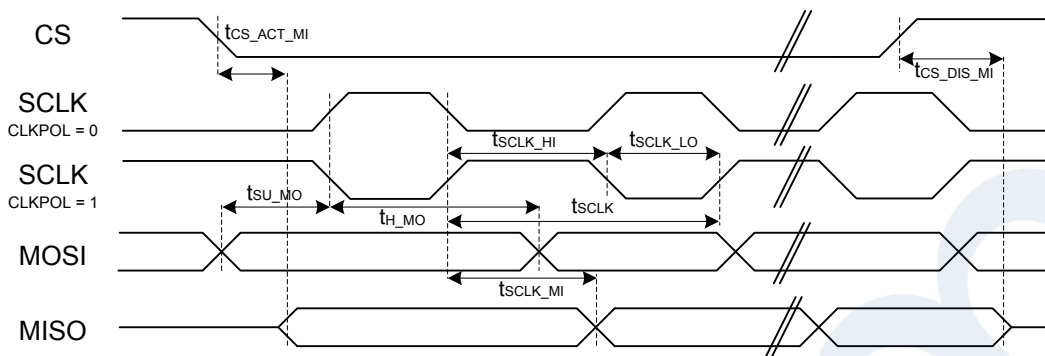


Figure 4.6. SPI Secondary Timing

4.21.1 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.32. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------|----------------|-----|-----|-----|------|
| SCLK high time ^{1 2} | t_{SCLK_HI} | | 50 | — | — | ns |
| SCLK low time ^{1 2} | t_{SCLK_LO} | | 50 | — | — | ns |
| CS active to MISO ^{1 2} | $t_{CS_ACT_MI}$ | | 5 | — | 50 | ns |
| CS disable to MISO ^{1 2} | $t_{CS_DIS_MI}$ | | 7 | — | 40 | ns |
| MOSI setup time ^{1 2} | t_{SU_MO} | | 5 | — | — | ns |
| MOSI hold time ^{1 2} | t_{H_MO} | | 6 | — | — | ns |
| SCLK to MISO ^{1 2} | t_{SCLK_MI} | IOVDD = 1.8 V | 9 | — | 40 | ns |
| | | IOVDD = 3.3 V | 9 | — | 30 | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

4.21.2 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.33. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|----------------|-----|-----|-----|------|
| SCLK high time ^{1 2} | t _{SCLK_HI} | | 50 | — | — | ns |
| SCLK low time ^{1 2} | t _{SCLK_LO} | | 50 | — | — | ns |
| CS active to MISO ^{1 2} | t _{CS_ACT_MI} | | 6 | — | 75 | ns |
| CS disable to MISO ^{1 2} | t _{CS_DIS_MI} | | 6 | — | 60 | ns |
| MOSI setup time ^{1 2} | t _{SU_MO} | | 8 | — | — | ns |
| MOSI hold time ^{1 2} | t _{H_MO} | | 11 | — | — | ns |
| SCLK to MISO ^{1 2} | t _{SCLK_MI} | IOVDD = 1.8 V | 10 | — | 50 | ns |
| | | IOVDD = 3.3 V | 10 | — | 42 | ns |
| Note: | | | | | | |
| 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0). | | | | | | |
| 2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}). | | | | | | |

4.21.3 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE0

Timing specifications at VSCALE0 apply to EUSART0 only, routed to DBUSAB on consecutive pins. All GPIO set to slew rate = 6.

Table 4.34. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE0

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------------|----------------|-----|-----|-----|------|
| SCLK high time ^{1 2} | t _{SCLK_HI} | | 100 | — | — | ns |
| SCLK low time ^{1 2} | t _{SCLK_LO} | | 100 | — | — | ns |
| CS active to MISO ^{1 2} | t _{CS_ACT_MI} | | 8 | — | 112 | ns |
| CS disable to MISO ^{1 2} | t _{CS_DIS_MI} | | 8 | — | 82 | ns |
| MOSI setup time ^{1 2} | t _{SU_MO} | | 12 | — | — | ns |
| MOSI hold time ^{1 2} | t _{H_MO} | | 32 | — | — | ns |
| Note: | | | | | | |
| 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0). | | | | | | |
| 2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}). | | | | | | |

4.22 I2C Electrical Specifications

4.22.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.35. I2C Standard-mode (Sm)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|----------------|-----|-----|-----|---------|
| SCL clock frequency ¹ | f_{SCL} | | 0 | — | 100 | kHz |
| SCL clock low time | t_{LOW} | | 4.7 | — | — | μs |
| SCL clock high time | t_{HIGH} | | 4 | — | — | μs |
| SDA set-up time | t_{SU_DAT} | | 250 | — | — | ns |
| SDA hold time | t_{HD_DAT} | | 0 | — | — | ns |
| Repeated START condition set-up time | t_{SU_STA} | | 4.7 | — | — | μs |
| Repeated START condition hold time | t_{HD_STA} | | 4.0 | — | — | μs |
| STOP condition set-up time | t_{SU_STO} | | 4.0 | — | — | μs |
| Bus free time between a STOP and START condition | t_{BUF} | | 4.7 | — | — | μs |

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.22.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.36. I2C Fast-mode (Fm)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|----------------|-----|-----|-----|---------|
| SCL clock frequency ¹ | f_{SCL} | | 0 | — | 400 | kHz |
| SCL clock low time | t_{LOW} | | 1.3 | — | — | μs |
| SCL clock high time | t_{HIGH} | | 0.6 | — | — | μs |
| SDA set-up time | t_{SU_DAT} | | 100 | — | — | ns |
| SDA hold time | t_{HD_DAT} | | 0 | — | — | ns |
| Repeated START condition set-up time | t_{SU_STA} | | 0.6 | — | — | μs |
| Repeated START condition hold time | t_{HD_STA} | | 0.6 | — | — | μs |
| STOP condition set-up time | t_{SU_STO} | | 0.6 | — | — | μs |
| Bus free time between a STOP and START condition | t_{BUF} | | 1.3 | — | — | μs |

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.22.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.37. I2C Fast-mode Plus (Fm+)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|------|-----|------|------|
| SCL clock frequency ¹ | f _{SCL} | | 0 | — | 1000 | kHz |
| SCL clock low time | t _{LOW} | | 0.5 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.26 | — | — | μs |
| SDA set-up time | t _{SU_DAT} | | 50 | — | — | ns |
| SDA hold time | t _{HD_DAT} | | 0 | — | — | ns |
| Repeated START condition set-up time | t _{SU_STA} | | 0.26 | — | — | μs |
| Repeated START condition hold time | t _{HD_STA} | | 0.26 | — | — | μs |
| STOP condition set-up time | t _{SU_STO} | | 0.26 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 0.5 | — | — | μs |

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HF XO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.23 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version 2.1.4
- Gecko Bootloader size 24 kB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.38. Boot Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------|-------------------|--|-----|------|-----|------|
| Boot time ¹ | t _{BOOT} | Secure boot application check disabled, 50 kB application size | — | 46.4 | — | ms |
| | | Secure boot application check enabled, 50 kB application size | — | 57.2 | — | ms |
| | | Secure boot application check enabled, 150 kB application size | — | 59.9 | — | ms |
| | | Secure boot application check enabled, 350 kB application size | — | 65.2 | — | ms |

Note:

- Secure boot check of second stage bootloader enabled for all measurements.

4.24 Crypto Operation Timing for SE Manager API

Values in this table represent timing from SE Manager API call to return. The Cortex-M33 HCLK frequency is 39.0 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version 2.1.4
- GSDK version 3.2

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.39. StdCmd Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------|-------------------|---|-----|------|-----|---------|
| AES-128 timing | t_{AES128} | AES-128 CCM encryption, PT 1 kB | — | 548 | — | μs |
| | | AES-128 CCM encryption, PT 32 kB | — | 1737 | — | μs |
| | | AES-128 CTR encryption, PT 1 kB | — | 439 | — | μs |
| | | AES-128 CTR encryption, PT 32 kB | — | 1006 | — | μs |
| | | AES-128 GCM encryption, PT 1 kB | — | 492 | — | μs |
| | | AES-128 GCM encryption, PT 32 kB | — | 1061 | — | μs |
| AES-256 timing | t_{AES256} | AES-256 CCM encryption, PT 1 kB | — | 563 | — | μs |
| | | AES-256 CCM encryption, PT 32 kB | — | 2161 | — | μs |
| | | AES-256 CTR encryption, PT 1 kB | — | 446 | — | μs |
| | | AES-256 CTR encryption, PT 32 kB | — | 1220 | — | μs |
| | | AES-256 GCM encryption, PT 1 kB | — | 500 | — | μs |
| | | AES-256 GCM encryption, PT 32 kB | — | 1274 | — | μs |
| ECC P-256 timing | t_{ECC_P256} | ECC key generation, P-256 | — | 5.5 | — | ms |
| | | ECC signing, P-256 | — | 5.9 | — | ms |
| | | ECC verification, P-256 | — | 6.1 | — | ms |
| ECC P-521 timing ¹ | t_{ECC_P521} | ECC key generation, P-521 | — | 30.3 | — | ms |
| | | ECC signing, P-521 | — | 31 | — | ms |
| | | ECC verification, P-521 | — | 36.1 | — | ms |
| ECC P-25519 timing ² | t_{ECC_P25519} | ECC key generation, P-25519 | — | 4.5 | — | ms |
| | | ECC signing, P-25519 | — | 8.9 | — | ms |
| | | ECC verification, P-25519 | — | 6.3 | — | ms |
| ECDH compute secret timing | t_{ECDH} | ECDH compute secret, P-521 ¹ | — | 30.3 | — | ms |
| | | ECDH compute secret, P-25519 ² | — | 4.4 | — | ms |
| | | ECDH compute secret, P-256 | — | 5.7 | — | ms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|------------------------|--------------------------------|-----|------|-----|------|
| ECJPAKE client timing | t _{ECJPAKE_C} | ECJPAKE client write round one | — | 21.5 | — | ms |
| | | ECJPAKE client read round one | — | 11.7 | — | ms |
| | | ECJPAKE client write round two | — | 15.2 | — | ms |
| | | ECJPAKE client read round two | — | 6.4 | — | ms |
| | | ECJPAKE client derive secret | — | 8.7 | — | ms |
| ECJPAKE server timing | t _{ECJPAKE_S} | ECJPAKE server write round one | — | 21.5 | — | ms |
| | | ECJPAKE server read round one | — | 11.7 | — | ms |
| | | ECJPAKE server write round two | — | 15.2 | — | ms |
| | | ECJPAKE server read round two | — | 6.4 | — | ms |
| | | ECJPAKE server derive secret | — | 8.8 | — | ms |
| POLY-1305 timing ¹ | t _{POLY1305} | POLY-1305, PT 1 kB | — | 478 | — | μs |
| | | POLY-1305, PT 32 kB | — | 1140 | — | μs |
| SHA-256 timing | t _{SHA256} | SHA-256, PT 1 kB | — | 263 | — | μs |
| | | SHA-256, PT 32 kB | — | 685 | — | μs |
| SHA-512 timing ¹ | t _{SHA512} | SHA-512, PT 1 kB | — | 260 | — | μs |
| | | SHA-512, PT 32 kB | — | 573 | — | μs |

Note:

- Option is only available on OPNs with Secure Vault High feature set.
- Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

4.25 Crypto Operation Average Current for SE Manager API

Values in this table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version 2.1.4
- GSDK version 3.2

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.40. StdCmd Supply Current

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|------------------------|---|-----|-----|-----|------|
| AES-128 current | I _{AES128} | AES-128 CCM encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-128 CCM encryption, PT 32 kB | — | 4.7 | — | mA |
| | | AES-128 CTR encryption, PT 1 kB | — | 1.6 | — | mA |
| | | AES-128 CTR encryption, PT 32 kB | — | 4.6 | — | mA |
| | | AES-128 GCM encryption, PT 1 kB | — | 1.6 | — | mA |
| | | AES-128 GCM encryption, PT 32 kB | — | 4.6 | — | mA |
| AES-256 current | I _{AES256} | AES-256 CCM encryption, PT 1 kB | — | 1.8 | — | mA |
| | | AES-256 CCM encryption, PT 32 kB | — | 4.8 | — | mA |
| | | AES-256 CTR encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-256 CTR encryption, PT 32 kB | — | 4.7 | — | mA |
| | | AES-256 GCM encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-256 GCM encryption, PT 32 kB | — | 4.7 | — | mA |
| ECC P-256 current | I _{ECCP256} | ECC key generation, P-256 | — | 2.4 | — | mA |
| | | ECC signing, P-256 | — | 2.4 | — | mA |
| | | ECC verification, P-256 | — | 2.4 | — | mA |
| ECC P-521 current ¹ | I _{ECCP521} | ECC key generation, P-521 | — | 2.6 | — | mA |
| | | ECC signing, P-521 | — | 2.6 | — | mA |
| | | ECC verification, P-521 | — | 2.6 | — | mA |
| ECC P-25519 current ² | I _{ECCP25519} | ECC key generation, P-25519 | — | 2.4 | — | mA |
| | | ECC signing, P-25519 | — | 2.4 | — | mA |
| | | ECC verification, P-25519 | — | 2.4 | — | mA |
| ECDH compute secret current | I _{ECDH} | ECDH compute secret, P-521 ¹ | — | 2.6 | — | mA |
| | | ECDH compute secret, P-25519 ² | — | 2.3 | — | mA |
| | | ECDH compute secret, P-256 | — | 2.4 | — | mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|------------------------|--------------------------------|-----|-----|-----|------|
| ECJPAKE client current | I _{ECJPAKE_C} | ECJPAKE client write round one | — | 2.5 | — | mA |
| | | ECJPAKE client read round one | — | 2.5 | — | mA |
| | | ECJPAKE client write round two | — | 2.5 | — | mA |
| | | ECJPAKE client read round two | — | 2.4 | — | mA |
| | | ECJPAKE client derive secret | — | 2.5 | — | mA |
| ECJPAKE server current | I _{ECJPAKE_S} | ECJPAKE server write round one | — | 2.5 | — | mA |
| | | ECJPAKE server read round one | — | 2.5 | — | mA |
| | | ECJPAKE server write round two | — | 2.5 | — | mA |
| | | ECJPAKE server read round two | — | 2.4 | — | mA |
| | | ECJPAKE server derive secret | — | 2.5 | — | mA |
| POLY-1305 current ¹ | I _{POLY1305} | POLY-1305, PT 1 kB | — | 1.5 | — | mA |
| | | POLY-1305, PT 32 kB | — | 2.4 | — | mA |
| SHA-256 current | I _{SHA256} | SHA-256, PT 1 kB | — | 1.5 | — | mA |
| | | SHA-256, PT 32 kB | — | 3.1 | — | mA |
| SHA-512 current ¹ | I _{SHA512} | SHA-512, PT 1 kB | — | 1.5 | — | mA |
| | | SHA-512, PT 32 kB | — | 2.7 | — | mA |

Note:

- Option is only available on OPNs with Secure Vault High feature set.
- Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

4.26 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.26.1 Supply Current

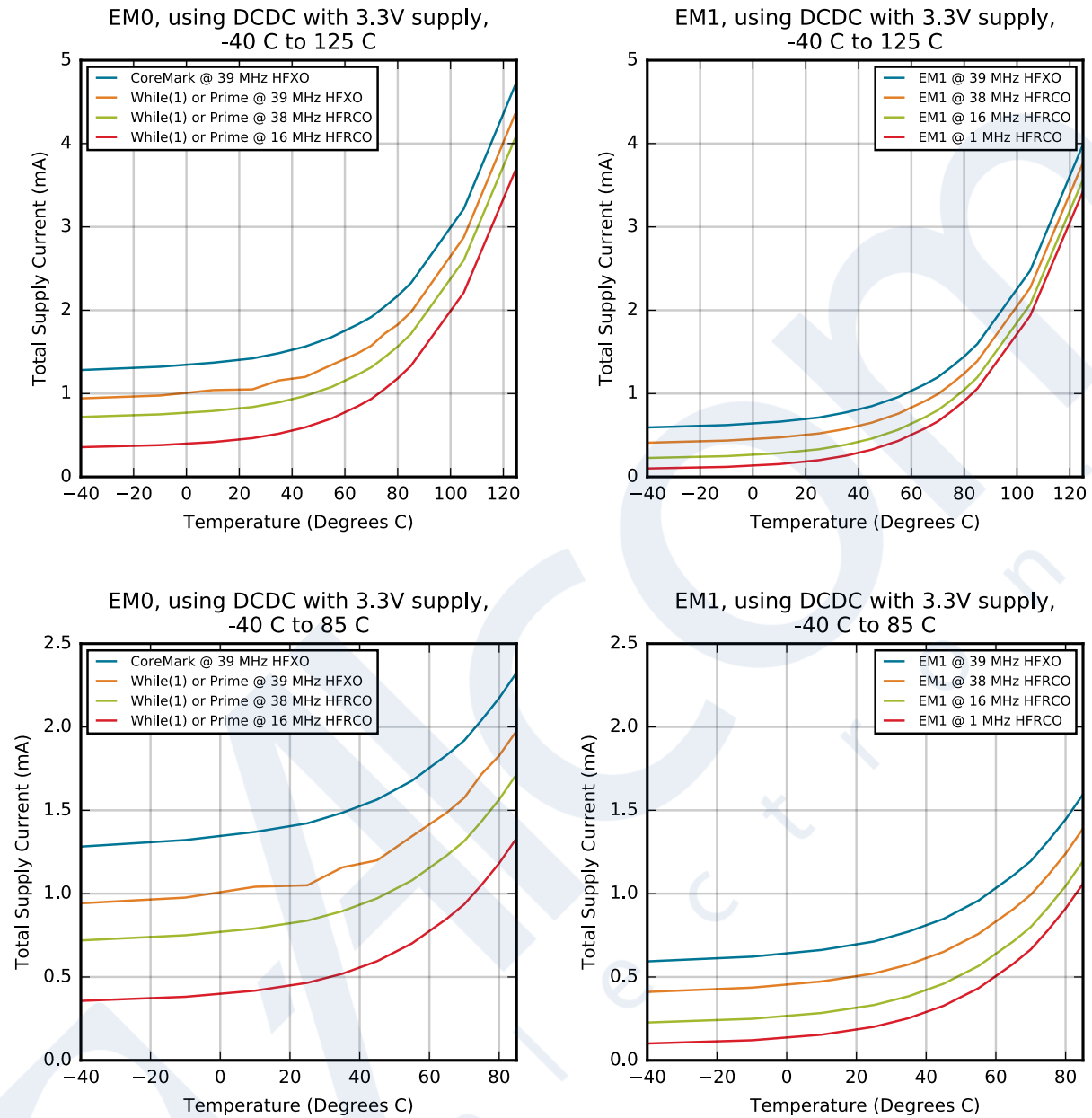


Figure 4.7. EM0 and EM1 Typical Supply Current vs. Temperature

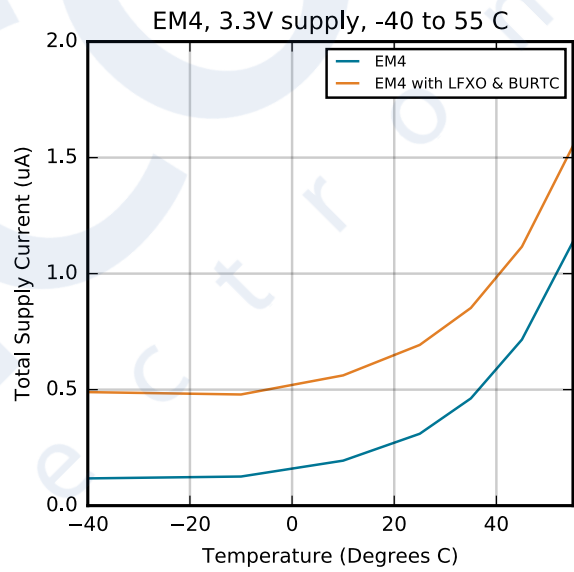
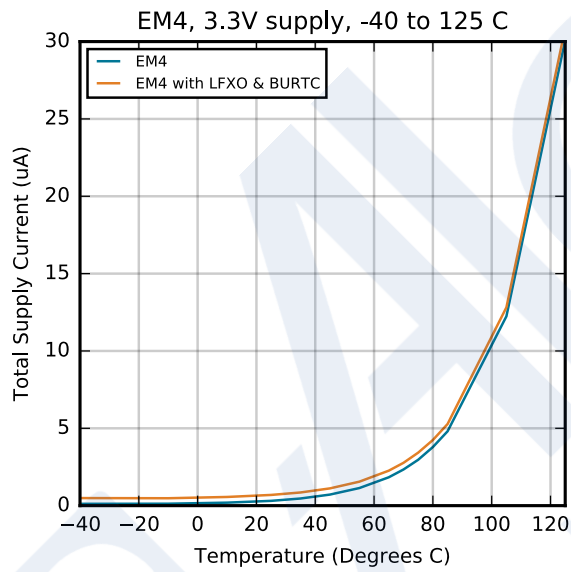
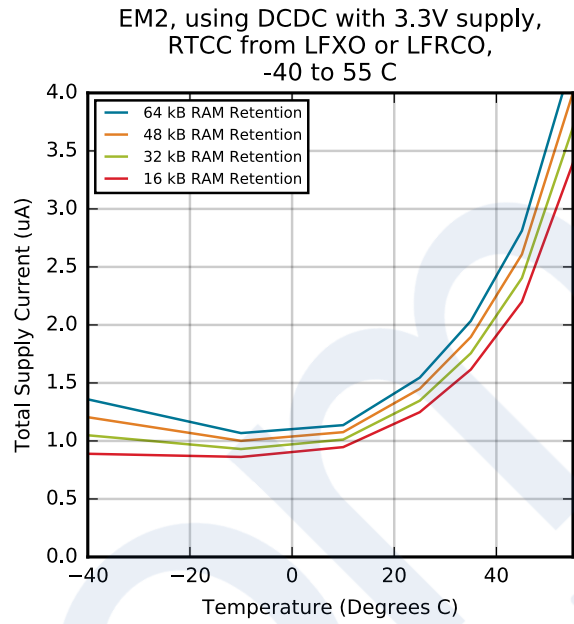
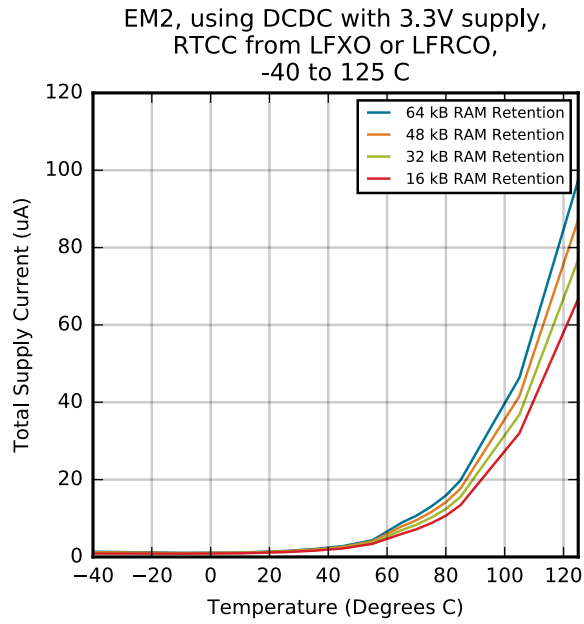


Figure 4.8. EM2 and EM4 Typical Supply Current vs. Temperature

4.26.2 DC-DC Converter

Performance characterized with Samsung CIG22H2R2MNE ($L_{DCDC} = 2.2 \mu\text{H}$) and Samsung CL10B475KQ8NQNC ($C_{DCDC} = 4.7 \mu\text{F}$)

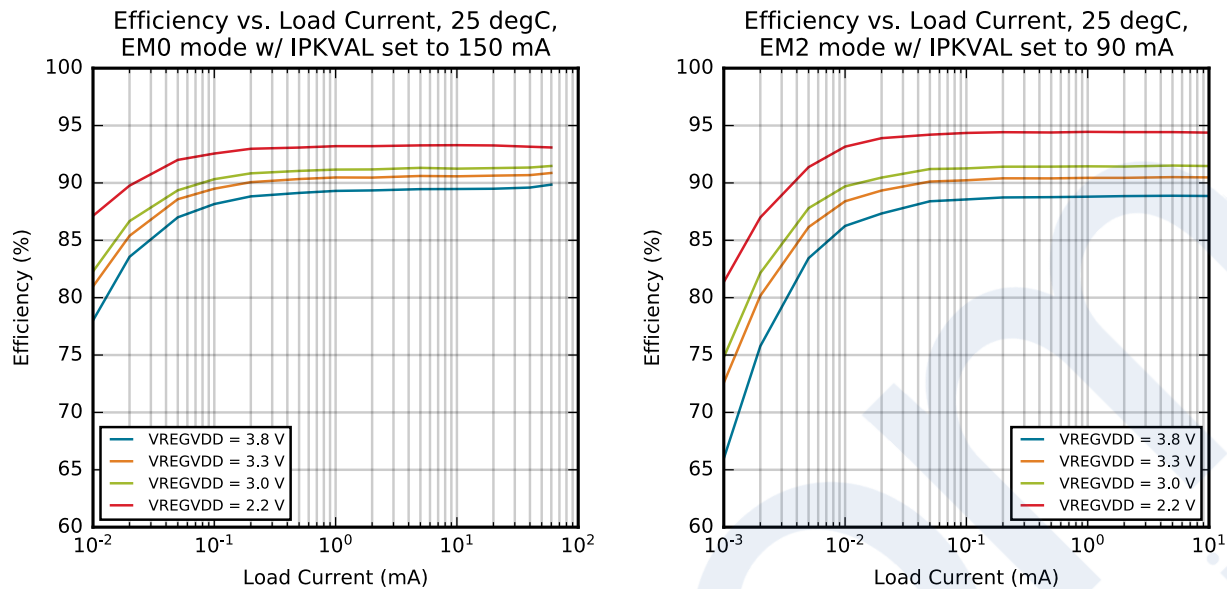


Figure 4.9. DC-DC Efficiency

4.26.3 IADC

Typical performance is shown across different oversampling ratio (OSR) settings with the maximum speed ADC clock. The ADC clock speed is 10 MHz for Normal mode, 20 MHz for High Speed mode, and 5 MHz for High Accuracy mode.

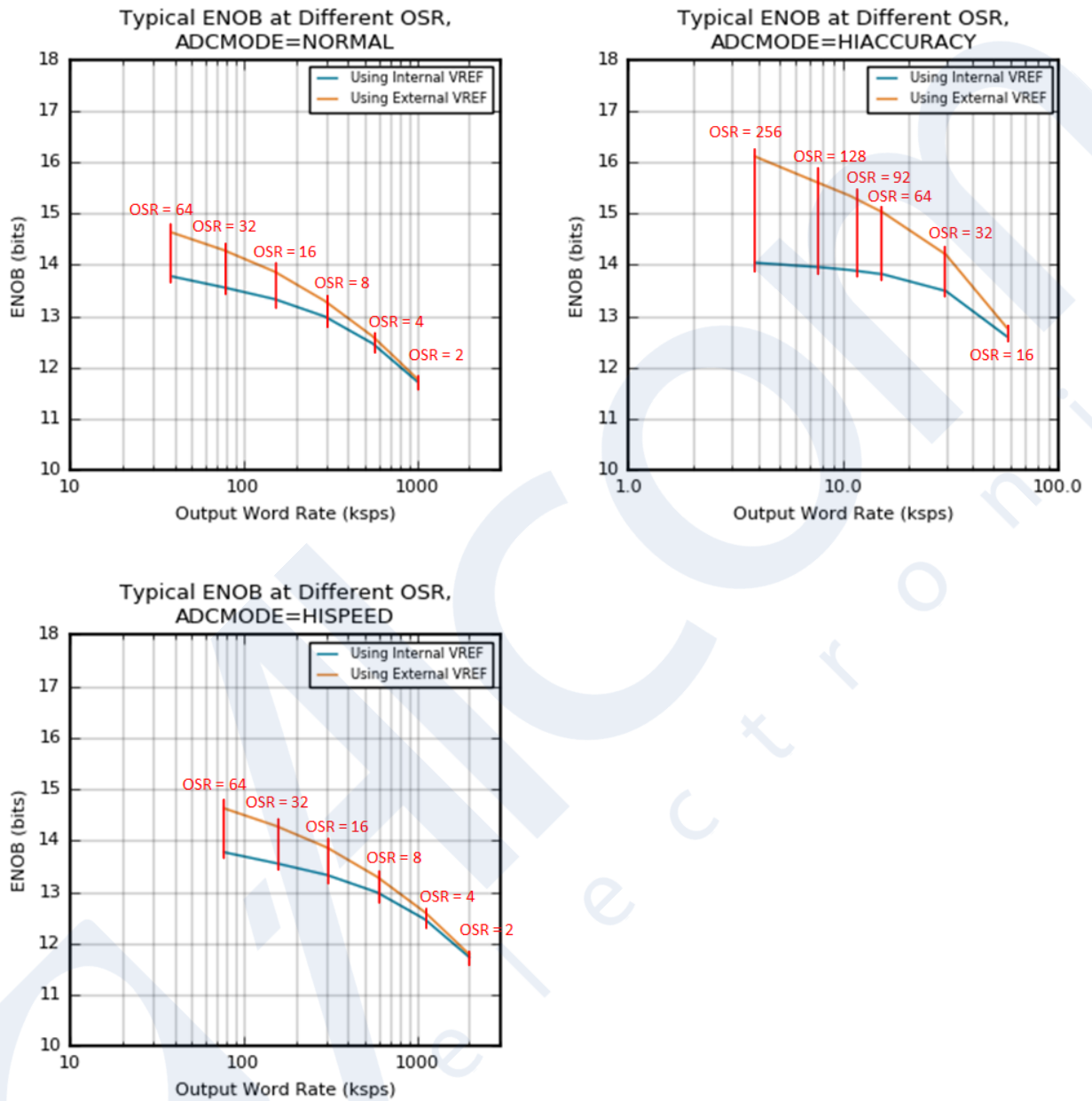


Figure 4.10. Typical ENOB vs. Oversampling Ratio

4.26.4 GPIO

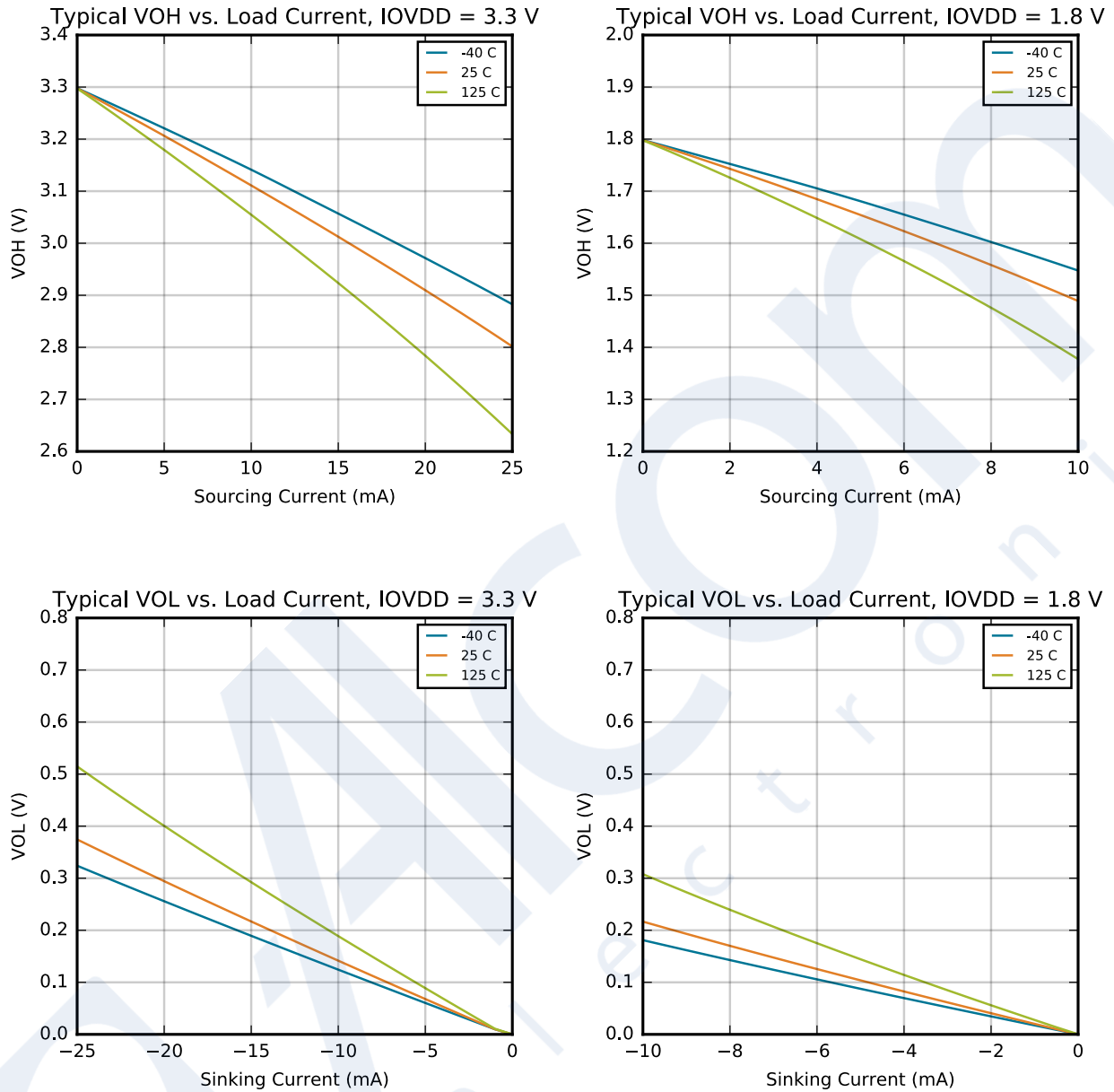


Figure 4.11. VOH and VOL vs. Load Current

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections are shown in the following figures.

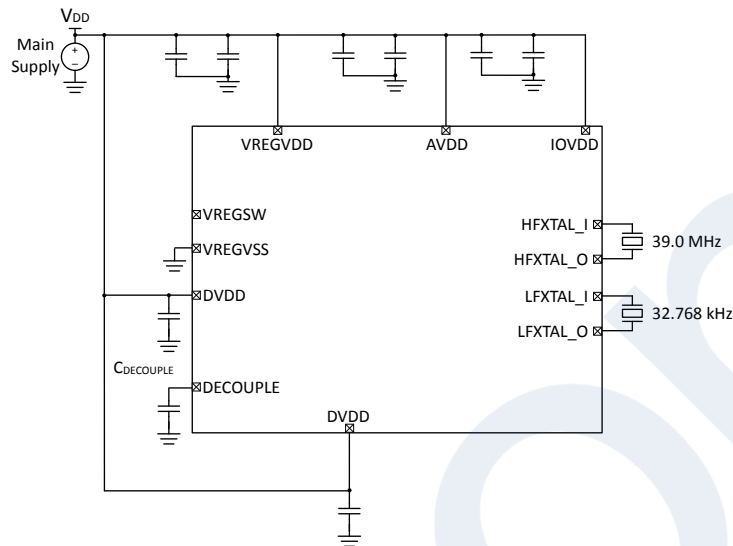


Figure 5.1. EFM32PG23 Typical Application Circuit: Direct Supply Configuration without DCDC

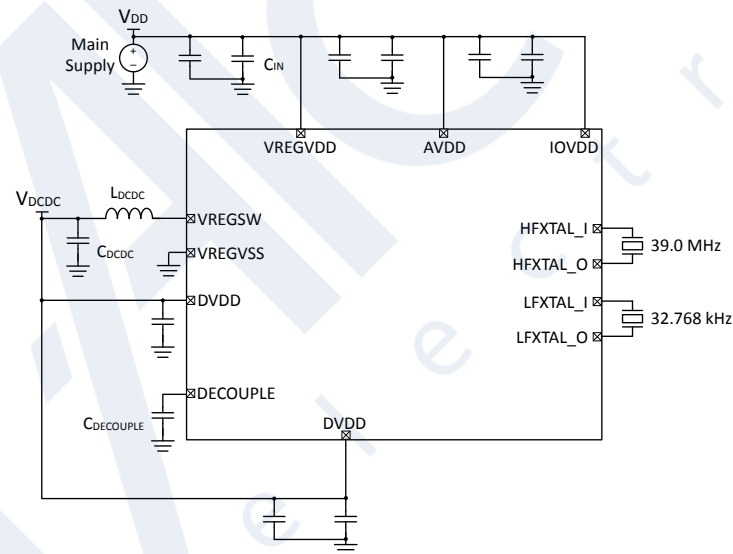


Figure 5.2. EFM32PG23 Typical Application Circuit: DCDC Configuration

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note [AN0002.2: "EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations"](#) contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN48 Device Pinout

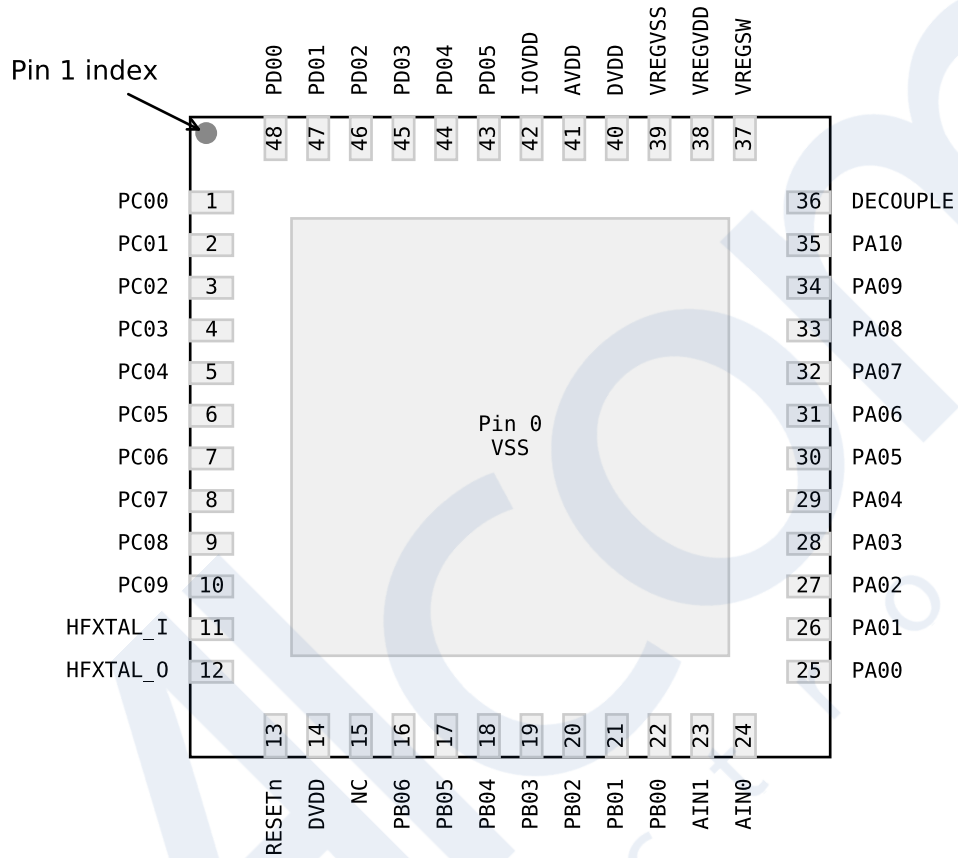


Figure 6.1. QFN48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.1. QFN48 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------|----------|--------|-------------|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | PC07 | 8 | GPIO |
| PC08 | 9 | GPIO | PC09 | 10 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---------------------|--------|-------------------------------|----------|--------|--------------------------------|
| HFXTAL_I | 11 | High Frequency XTAL input pin | HFXTAL_O | 12 | High Frequency XTAL output pin |
| RESETE _n | 13 | Reset pin (active low) | DVDD | 14 | Digital VDD supply pin |
| NC | 15 | No Connection | PB06 | 16 | GPIO |
| PB05 | 17 | GPIO | PB04 | 18 | GPIO |
| PB03 | 19 | GPIO | PB02 | 20 | GPIO |
| PB01 | 21 | GPIO | PB00 | 22 | GPIO |
| AIN1 | 23 | ADC input 1 | AIN0 | 24 | ADC input 0 |
| PA00 | 25 | GPIO | PA01 | 26 | GPIO |
| PA02 | 27 | GPIO | PA03 | 28 | GPIO |
| PA04 | 29 | GPIO | PA05 | 30 | GPIO |
| PA06 | 31 | GPIO | PA07 | 32 | GPIO |
| PA08 | 33 | GPIO | PA09 | 34 | GPIO |
| PA10 | 35 | GPIO | DECOUPLE | 36 | Decoupling Capacitor pin |
| VREGSW | 37 | DCDC output (Inductor) pin | VREGVDD | 38 | DCDC input supply pin |
| VREGVSS | 39 | DCDC ground pin | DVDD | 40 | Digital VDD supply pin |
| AVDD | 41 | Analog VDD supply pin | IOVDD | 42 | IO VDD supply pin |
| PD05 | 43 | GPIO | PD04 | 44 | GPIO |
| PD03 | 45 | GPIO | PD02 | 46 | GPIO |
| PD01 | 47 | GPIO | PD00 | 48 | GPIO |

6.2 QFN48 with VREF Inputs Device Pinout

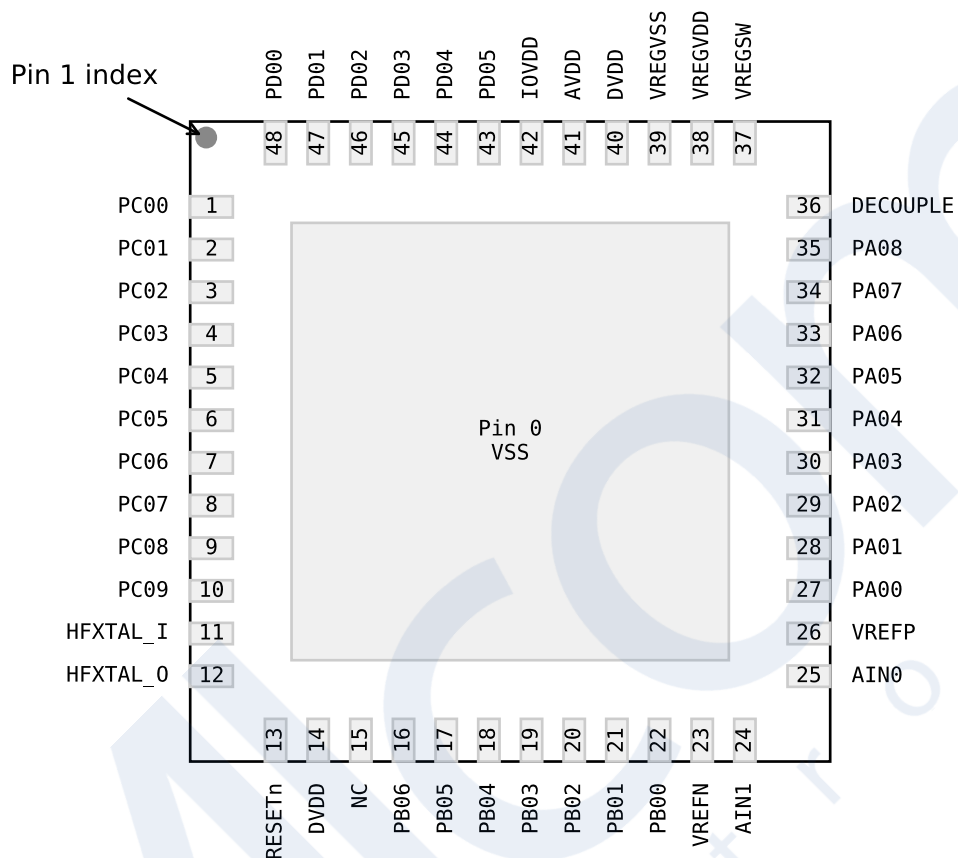


Figure 6.2. QFN48 with VREF Inputs Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.2. QFN48 with VREF Inputs Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|--------------------------------|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | PC07 | 8 | GPIO |
| PC08 | 9 | GPIO | PC09 | 10 | GPIO |
| HFXTAL_I | 11 | High Frequency XTAL input pin | HFXTAL_O | 12 | High Frequency XTAL output pin |
| RESETn | 13 | Reset pin (active low) | DVDD | 14 | Digital VDD supply pin |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|----------------------------|----------|--------|--------------------------|
| NC | 15 | | PB06 | 16 | GPIO |
| PB05 | 17 | GPIO | PB04 | 18 | GPIO |
| PB03 | 19 | GPIO | PB02 | 20 | GPIO |
| PB01 | 21 | GPIO | PB00 | 22 | GPIO |
| VREFN | 23 | VREF Negative input | AIN1 | 24 | ADC input 1 |
| AIN0 | 25 | ADC input 0 | VREFP | 26 | VREF Positive Input |
| PA00 | 27 | GPIO | PA01 | 28 | GPIO |
| PA02 | 29 | GPIO | PA03 | 30 | GPIO |
| PA04 | 31 | GPIO | PA05 | 32 | GPIO |
| PA06 | 33 | GPIO | PA07 | 34 | GPIO |
| PA08 | 35 | GPIO | DECOUPLE | 36 | Decoupling Capacitor pin |
| VREGSW | 37 | DCDC output (Inductor) pin | VREGVDD | 38 | DCDC input supply pin |
| VREGVSS | 39 | DCDC ground pin | DVDD | 40 | Digital VDD supply pin |
| AVDD | 41 | Analog VDD supply pin | IOVDD | 42 | IO VDD supply pin |
| PD05 | 43 | GPIO | PD04 | 44 | GPIO |
| PD03 | 45 | GPIO | PD02 | 46 | GPIO |
| PD01 | 47 | GPIO | PD00 | 48 | GPIO |

6.3 QFN40 Device Pinout

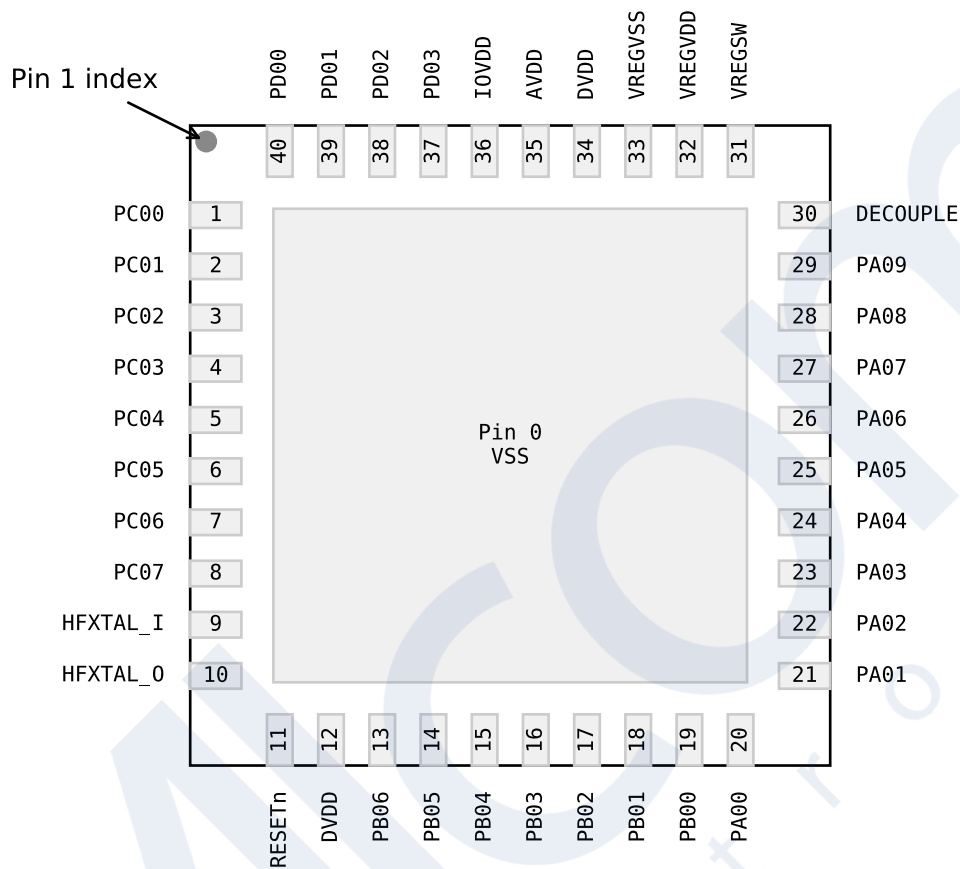


Figure 6.3. QFN40 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.3. QFN40 Device Pinout

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|-------------------------------|----------|--------|--------------------------------|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | PC07 | 8 | GPIO |
| HFXTAL_I | 9 | High Frequency XTAL input pin | HFXTAL_O | 10 | High Frequency XTAL output pin |
| RESETh | 11 | Reset pin (active low) | DVDD | 12 | Digital VDD supply pin |
| PB06 | 13 | GPIO | PB05 | 14 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|----------|--------|----------------------------|----------|--------|--------------------------|
| PB04 | 15 | GPIO | PB03 | 16 | GPIO |
| PB02 | 17 | GPIO | PB01 | 18 | GPIO |
| PB00 | 19 | GPIO | PA00 | 20 | GPIO |
| PA01 | 21 | GPIO | PA02 | 22 | GPIO |
| PA03 | 23 | GPIO | PA04 | 24 | GPIO |
| PA05 | 25 | GPIO | PA06 | 26 | GPIO |
| PA07 | 27 | GPIO | PA08 | 28 | GPIO |
| PA09 | 29 | GPIO | DECOUPLE | 30 | Decoupling Capacitor pin |
| VREGSW | 31 | DCDC output (Inductor) pin | VREGVDD | 32 | DCDC input supply pin |
| VREGVSS | 33 | DCDC ground pin | DVDD | 34 | Digital VDD supply pin |
| AVDD | 35 | Analog VDD supply pin | IOVDD | 36 | IO VDD supply pin |
| PD03 | 37 | GPIO | PD02 | 38 | GPIO |
| PD01 | 39 | GPIO | PD00 | 40 | GPIO |

6.4 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

Table 6.4. GPIO Alternate Function Table

| GPIO | Alternate Functions | QFN48 Package ¹ | QFN48 with VREF In-puts Package ² | QFN40 Package ³ |
|------|---------------------|----------------------------|--|----------------------------|
| PA00 | IADC0.VREFP | Yes | | Yes |
| | LCD.SEG8 | Yes | Yes | Yes |
| PA01 | GPIO.SWCLK | Yes | Yes | Yes |
| | LCD.SEG9 | Yes | Yes | Yes |
| PA02 | GPIO.SWDIO | Yes | Yes | Yes |
| PA03 | GPIO.SWV | Yes | Yes | Yes |
| | GPIO.TDO | Yes | Yes | Yes |
| | GPIO.TRACEDATA0 | Yes | Yes | Yes |
| | LESENSE.EN_0 | Yes | Yes | Yes |
| PA04 | GPIO.TDI | Yes | Yes | Yes |
| | GPIO.TRACECLK | Yes | Yes | Yes |
| | LCD.SEG10 | Yes | Yes | Yes |
| | LESENSE.EN_1 | Yes | Yes | Yes |
| PA05 | GPIO.TRACEDATA1 | Yes | Yes | Yes |
| | GPIO.EM4WU0 | Yes | Yes | Yes |
| | LCD.SEG11 | Yes | Yes | Yes |
| | LESENSE.EN_2 | Yes | Yes | Yes |
| PA06 | GPIO.TRACEDATA2 | Yes | Yes | Yes |
| | LCD.LCD_CP | Yes | Yes | Yes |
| PA07 | GPIO.TRACEDATA3 | Yes | Yes | Yes |
| | LCD.SEG12 | Yes | Yes | Yes |
| PA08 | LCD.SEG13 | Yes | Yes | Yes |
| PB00 | LCD.SEG14 | Yes | Yes | Yes |
| | VDAC0.CH0_MAIN_OUT | Yes | Yes | Yes |
| PB01 | GPIO.EM4WU3 | Yes | Yes | Yes |
| | LCD.SEG15 | Yes | Yes | Yes |
| | VDAC0.CH1_MAIN_OUT | Yes | Yes | Yes |
| PB02 | LCD.SEG16 | Yes | Yes | Yes |
| PB03 | GPIO.EM4WU4 | Yes | Yes | Yes |
| | LCD.SEG17 | Yes | Yes | Yes |
| PC00 | GPIO.EM4WU6 | Yes | Yes | Yes |
| | LCD.SEG0 | Yes | Yes | Yes |

| GPIO | Alternate Functions | QFN48 Package ¹ | QFN48 with VREF Inputs Package ² | QFN40 Package ³ |
|------|---------------------|----------------------------|---|----------------------------|
| PC01 | LCD.SEG1 | Yes | Yes | Yes |
| PC02 | LCD.SEG2 | Yes | Yes | Yes |
| PC03 | LCD.SEG3 | Yes | Yes | Yes |
| PC04 | LCD.SEG4 | Yes | Yes | Yes |
| PC05 | GPIO.EM4WU7 | Yes | Yes | Yes |
| | LCD.SEG5 | Yes | Yes | Yes |
| PC06 | LCD.SEG6 | Yes | Yes | Yes |
| PC07 | GPIO.EM4WU8 | Yes | Yes | Yes |
| | LCD.SEG7 | Yes | Yes | Yes |
| PC08 | LCD.SEG18 | Yes | Yes | |
| PC09 | LCD.SEG19 | Yes | Yes | |
| PD00 | LFXO.LFXTAL_O | Yes | Yes | Yes |
| PD01 | LFXO.LFXTAL_I | Yes | Yes | Yes |
| | LFXO.LF_EXTCLK | Yes | Yes | Yes |
| PD02 | GPIO.EM4WU9 | Yes | Yes | Yes |
| | LCD.COM0 | Yes | Yes | Yes |
| PD03 | LCD.COM1 | Yes | Yes | Yes |
| PD04 | LCD.COM2 | Yes | Yes | |
| PD05 | GPIO.EM4WU10 | Yes | Yes | |
| | LCD.COM3 | Yes | Yes | |

Note:

1. QFN48 Package includes OPNs EFM32PG23B210F128IM48-C, EFM32PG23B210F256IM48-C, EFM32PG23B210F512IM48-C, and EFM32PG23B210F64IM48-C
2. QFN48 with VREF Inputs Package includes OPNs EFM32PG23B310F128IM48-C, EFM32PG23B310F256IM48-C, EFM32PG23B310F512IM48-C, and EFM32PG23B310F64IM48-C
3. QFN40 Package includes OPNs EFM32PG23B200F128IM40-C, EFM32PG23B200F256IM40-C, EFM32PG23B200F512IM40-C, and EFM32PG23B200F64IM40-C

6.5 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.5. ABUS Routing Table

| Peripheral | Signal | PA | | PB | | PC | | PD | |
|------------|--------------|------|-----|------|-----|------|-----|------|-----|
| | | EVEN | ODD | EVEN | ODD | EVEN | ODD | EVEN | ODD |
| ACMP0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ACMP1 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| IADC0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| VDAC0 | CH0_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | CH1_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

6.6 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.6. DBUS Routing Table

| Peripheral.Resource | PORT | | | |
|---------------------------|-----------|-----------|-----------|-----------|
| | PA | PB | PC | PD |
| ACMP0.DIGOUT | Available | Available | Available | Available |
| ACMP1.DIGOUT | Available | Available | Available | Available |
| CMU.CLKIN0 | | | Available | Available |
| CMU.CLKOUT0 | | | Available | Available |
| CMU.CLKOUT1 | | | Available | Available |
| CMU.CLKOUT2 | Available | Available | | |
| EUSART0.CS | Available | Available | | |
| EUSART0.CTS | Available | Available | | |
| EUSART0.RTS | Available | Available | | |
| EUSART0.RX | Available | Available | | |
| EUSART0.SCLK | Available | Available | | |
| EUSART0.TX | Available | Available | | |
| EUSART1.CS | Available | Available | Available | Available |
| EUSART1.CTS | Available | Available | Available | Available |
| EUSART1.RTS | Available | Available | Available | Available |
| EUSART1.RX | Available | Available | Available | Available |
| EUSART1.SCLK | Available | Available | Available | Available |
| EUSART1.TX | Available | Available | Available | Available |
| EUSART2.CS | | | Available | Available |
| EUSART2.CTS | | | Available | Available |
| EUSART2.RTS | | | Available | Available |
| EUSART2.RX | | | Available | Available |
| EUSART2.SCLK | | | Available | Available |
| EUSART2.TX | | | Available | Available |
| HFX00.BUFOUT_REQ_IN_ASYNC | Available | Available | | |
| I2C0.SCL | Available | Available | Available | Available |
| I2C0.SDA | Available | Available | Available | Available |
| I2C1.SCL | | | Available | Available |
| I2C1.SDA | | | Available | Available |
| KEYSCAN.COL_OUT_0 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_1 | Available | Available | Available | Available |

| Peripheral.Resource | PORT | | | |
|---------------------|-----------|-----------|-----------|-----------|
| | PA | PB | PC | PD |
| KEYSCAN.COL_OUT_2 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_3 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_4 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_5 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_6 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_7 | Available | Available | Available | Available |
| KEYSCAN.ROW_SENSE_0 | Available | Available | | |
| KEYSCAN.ROW_SENSE_1 | Available | Available | | |
| KEYSCAN.ROW_SENSE_2 | Available | Available | | |
| KEYSCAN.ROW_SENSE_3 | Available | Available | | |
| KEYSCAN.ROW_SENSE_4 | Available | Available | | |
| KEYSCAN.ROW_SENSE_5 | Available | Available | | |
| LESENSE.CH0OUT | Available | Available | | |
| LESENSE.CH1OUT | Available | Available | | |
| LESENSE.CH2OUT | Available | Available | | |
| LESENSE.CH3OUT | Available | Available | | |
| LESENSE.CH4OUT | Available | Available | | |
| LESENSE.CH5OUT | Available | Available | | |
| LESENSE.CH6OUT | Available | Available | | |
| LESENSE.CH7OUT | Available | Available | | |
| LESENSE.CH8OUT | Available | Available | | |
| LESENSE.CH9OUT | Available | Available | | |
| LESENSE.CH10OUT | Available | Available | | |
| LESENSE.CH11OUT | Available | Available | | |
| LESENSE.CH12OUT | Available | Available | | |
| LESENSE.CH13OUT | Available | Available | | |
| LESENSE.CH14OUT | Available | Available | | |
| LESENSE.CH15OUT | Available | Available | | |
| LETIMER0.OUT0 | Available | Available | | |
| LETIMER0.OUT1 | Available | Available | | |
| PCNT0.S0IN | Available | Available | | |
| PCNT0.S1IN | Available | Available | | |
| PRS.ASYNCH0 | Available | Available | | |
| PRS.ASYNCH1 | Available | Available | | |
| PRS.ASYNCH2 | Available | Available | | |
| PRS.ASYNCH3 | Available | Available | | |

| Peripheral.Resource | PORT | | | |
|---------------------|-----------|-----------|-----------|-----------|
| | PA | PB | PC | PD |
| PRS.ASYNCH4 | Available | Available | | |
| PRS.ASYNCH5 | Available | Available | | |
| PRS.ASYNCH6 | | | Available | Available |
| PRS.ASYNCH7 | | | Available | Available |
| PRS.ASYNCH8 | | | Available | Available |
| PRS.ASYNCH9 | | | Available | Available |
| PRS.ASYNCH10 | | | Available | Available |
| PRS.ASYNCH11 | | | Available | Available |
| PRS.SYNCH0 | Available | Available | Available | Available |
| PRS.SYNCH1 | Available | Available | Available | Available |
| PRS.SYNCH2 | Available | Available | Available | Available |
| PRS.SYNCH3 | Available | Available | Available | Available |
| TIMER0.CC0 | Available | Available | Available | Available |
| TIMER0.CC1 | Available | Available | Available | Available |
| TIMER0.CC2 | Available | Available | Available | Available |
| TIMER0.CDTI0 | Available | Available | Available | Available |
| TIMER0.CDTI1 | Available | Available | Available | Available |
| TIMER0.CDTI2 | Available | Available | Available | Available |
| TIMER1.CC0 | Available | Available | Available | Available |
| TIMER1.CC1 | Available | Available | Available | Available |
| TIMER1.CC2 | Available | Available | Available | Available |
| TIMER1.CDTI0 | Available | Available | Available | Available |
| TIMER1.CDTI1 | Available | Available | Available | Available |
| TIMER1.CDTI2 | Available | Available | Available | Available |
| TIMER2.CC0 | Available | Available | | |
| TIMER2.CC1 | Available | Available | | |
| TIMER2.CC2 | Available | Available | | |
| TIMER2.CDTI0 | Available | Available | | |
| TIMER2.CDTI1 | Available | Available | | |
| TIMER2.CDTI2 | Available | Available | | |
| TIMER3.CC0 | | | Available | Available |
| TIMER3.CC1 | | | Available | Available |
| TIMER3.CC2 | | | Available | Available |
| TIMER3.CDTI0 | | | Available | Available |
| TIMER3.CDTI1 | | | Available | Available |
| TIMER3.CDTI2 | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---------------------|-----------|-----------|-----------|-----------|
| | PA | PB | PC | PD |
| TIMER4.CC0 | Available | Available | | |
| TIMER4.CC1 | Available | Available | | |
| TIMER4.CC2 | Available | Available | | |
| TIMER4.CDTI0 | Available | Available | | |
| TIMER4.CDTI1 | Available | Available | | |
| TIMER4.CDTI2 | Available | Available | | |
| USART0.CLK | Available | Available | Available | Available |
| USART0.CS | Available | Available | Available | Available |
| USART0.CTS | Available | Available | Available | Available |
| USART0.RTS | Available | Available | Available | Available |
| USART0.RX | Available | Available | Available | Available |
| USART0.TX | Available | Available | Available | Available |

7. QFN40 Package Specifications

7.1 QFN40 Package Dimensions

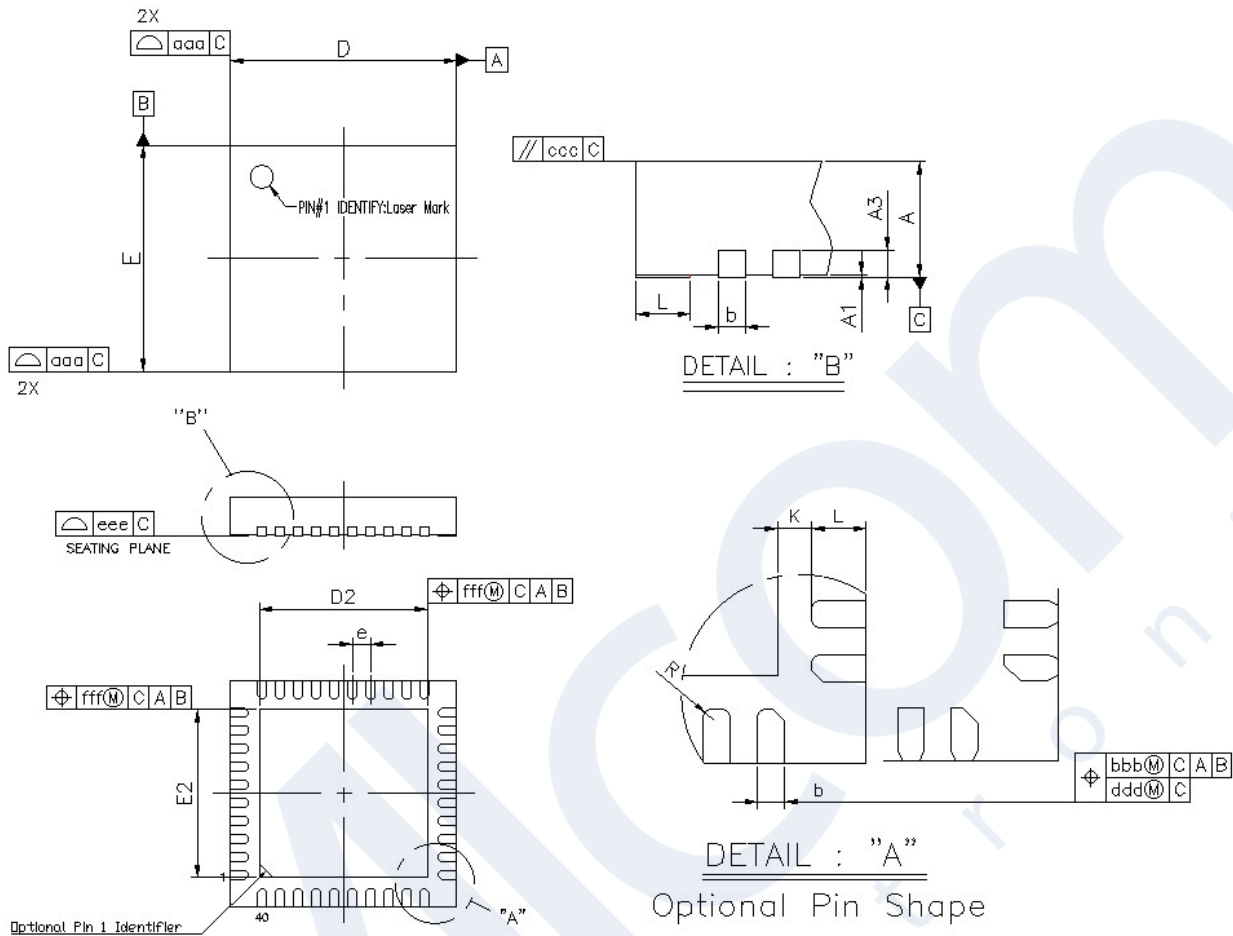


Figure 7.1. QFN40 Package Drawing

Table 7.1. QFN40 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.55 | 3.70 | 3.85 |
| E2 | 3.55 | 3.70 | 3.85 |
| e | 0.40 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.075 | — | — |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

7.2 QFN40 PCB Land Pattern

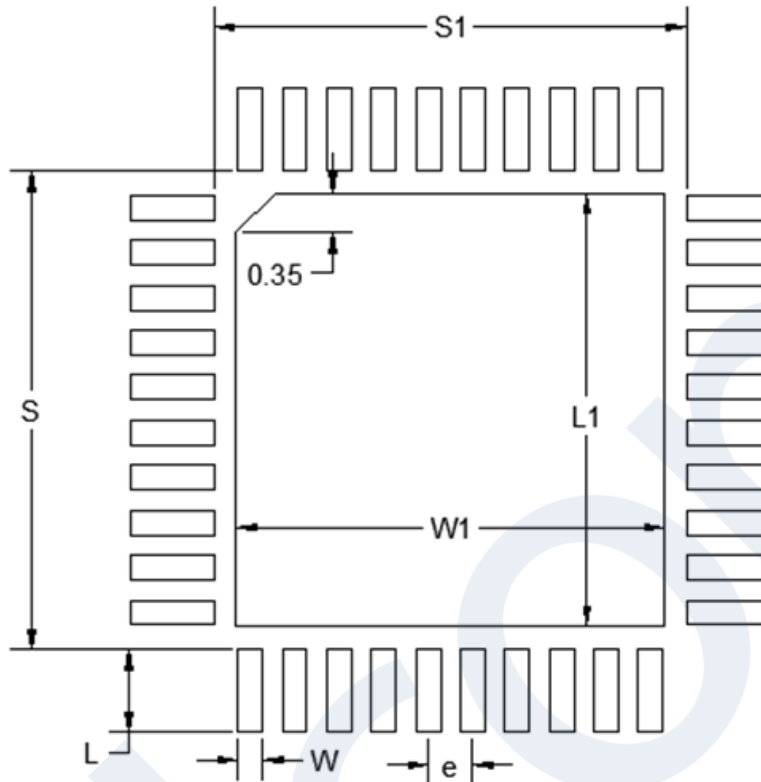


Figure 7.2. QFN40 PCB Land Pattern Drawing

Table 7.2. QFN40 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| S1 | 4.25 |
| S | 4.25 |
| L1 | 3.85 |
| W1 | 3.85 |
| e | 0.40 |
| W | 0.22 |
| L | 0.74 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. **Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.**

7.3 QFN40 Package Marking



Figure 7.3. QFN40 Package Marking

The package marking consists of:

- P P P P P P P P P P – The product option codes.
 - 1-9. The part number designation
 - 9. Flash (H = 512k | G = 256k | F = 128k | E = 64k)
 - 10. Temperature grade (I = -40 to 125 °C)
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # - The device revision.

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

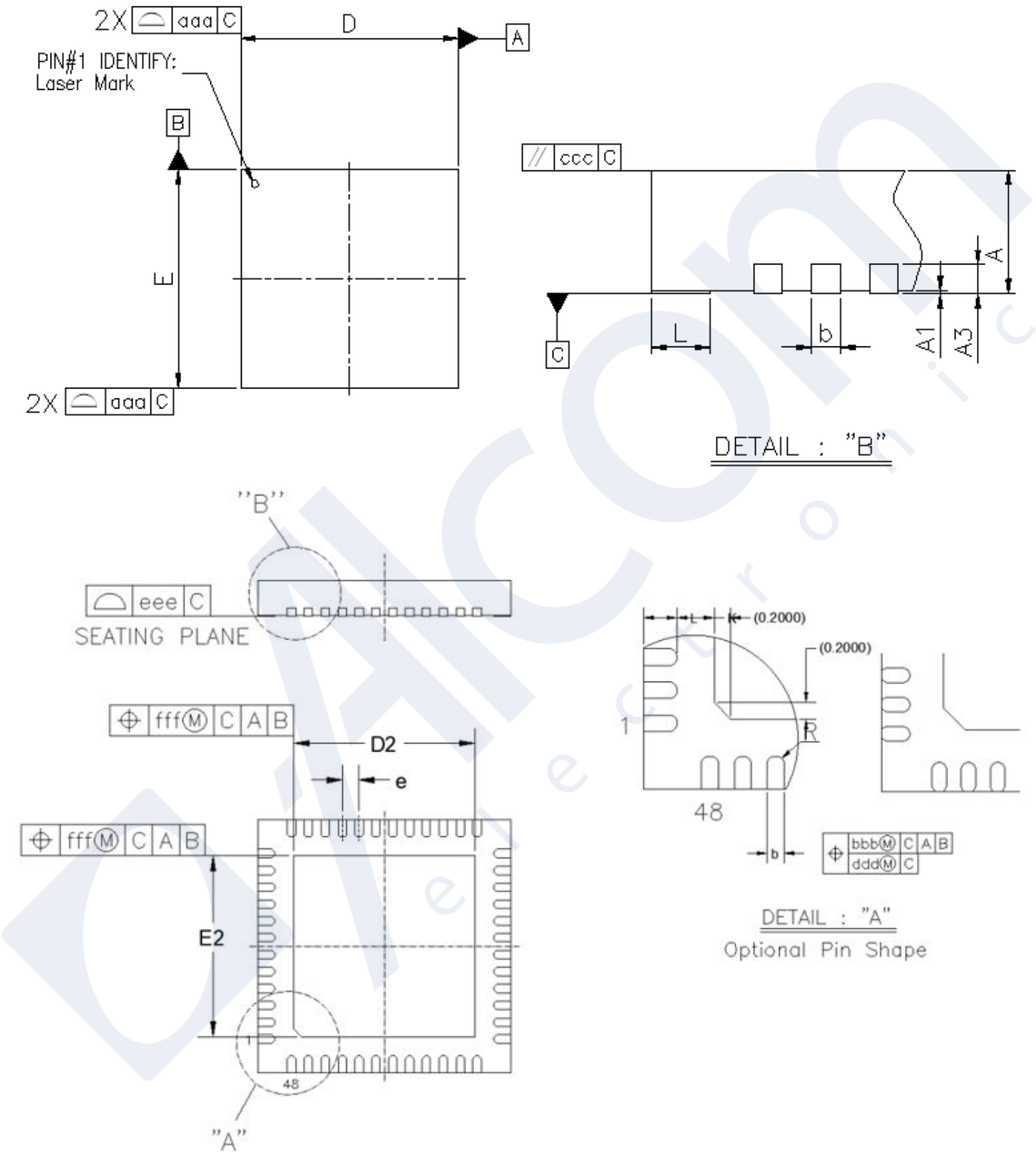


Figure 8.1. QFN48 Package Drawing

Table 8.1. QFN48 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.15 | 0.2 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 |
| e | 0.40 BSC | | |
| D2 | 4.15 | 4.30 | 4.45 |
| E2 | 4.15 | 4.30 | 4.45 |
| L | 0.30 | 0.4 | 0.50 |
| K | 0.20 | — | — |
| R | 0.075 | — | — |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8.2 QFN48 PCB Land Pattern

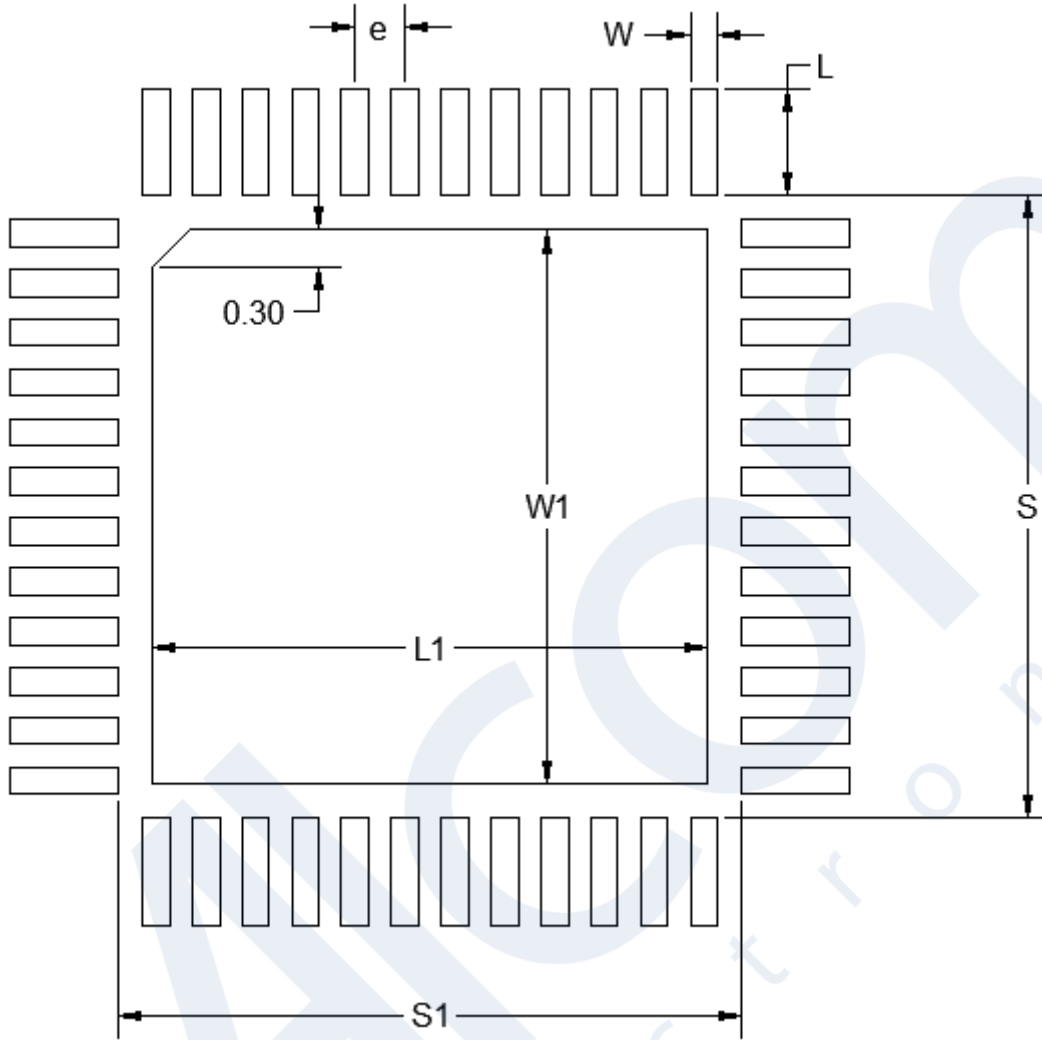


Figure 8.2. QFN48 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| L | 0.86 |
| W | 0.22 |
| e | 0.40 |
| S | 5.01 |
| S1 | 5.01 |
| L1 | 4.45 |
| W1 | 4.45 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 1.10mm x 1.10mm openings on 1.30mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

8.3 QFN48 Package Marking



Figure 8.3. QFN48 Package Marking

The package marking consists of:

- P P P P P P P P P P – The product option codes.
 - 1-9. The part number designation
 - 9. Flash (H = 512k | G = 256k | F = 128k | E = 64k)
 - 10. Temperature grade (I = -40 to 125 °C)
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # - The device revision.

9. Revision History

Revision 0.5

April, 2022

- Added [Figure 2.1 Ordering Code Key on page 4](#)
- [3.9.4 Power Domains](#): Extended description of available power domains.
- [4.1 Electrical Characteristics](#):
 - Populated electrical specification tables with latest characterization results.
 - Added Boot Timing and Crypto Operation Timing / Current tables.
- [6.4 Alternate Function Table](#): Changed formatting of section to show signals available on each package option and include footnote to detail OPNs.

Revision 0.2

July, 2021

Initial release.

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