

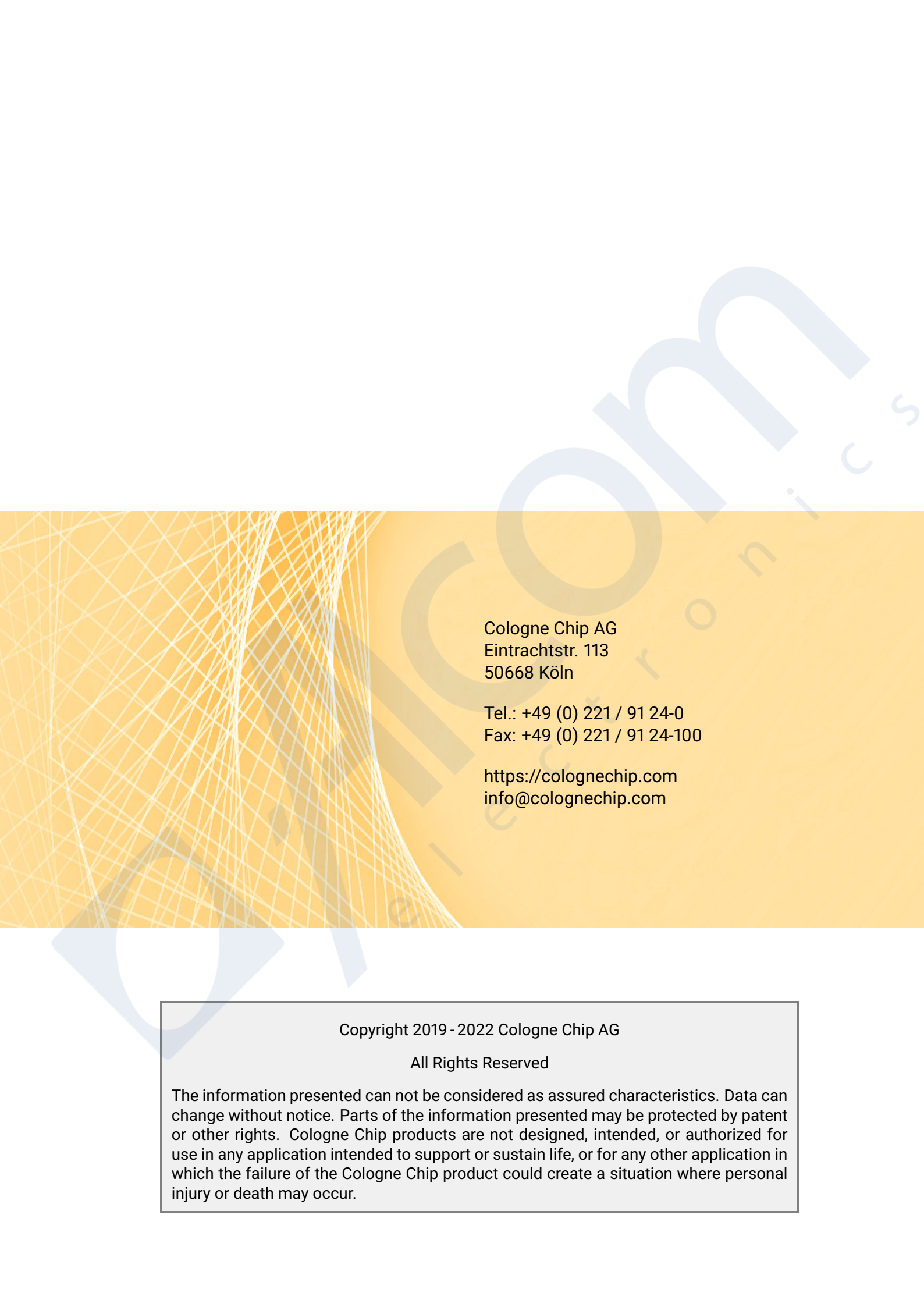


# GateMate™ FPGA Evaluation Board Datasheet

## Evaluation Board Version 3.1







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# About this Document

This datasheet covers all features of the Cologne Chip GateMate™ FPGA evaluation board and is part of the GateMate™ documentation collection.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA [↗](#)
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet [↗](#)
- **DS1002** – GateMate™ FPGA Programmer Board Ver. 1.3 Datasheet [↗](#)
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide [↗](#)

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

## Revision History

This Datasheet is constantly updated. The latest version of the document can be found following the link below:

**DS1003 – GateMate™ FPGA Evaluation Board Ver. 3.1 Datasheet** [↗](#)

A brief description and download links can be found here:

**GateMate™ FPGA Evaluation Board** [↗](#)

Date	Remarks
April 2022	Pmod signal assignment added (Table 3.8 on page 34).
March 2022	Initial release.



# Chapter 1

## Introduction

The GateMate™ FPGA Evaluation Board is a feature-rich, ready-to-use development platform for the CCGM1A1.

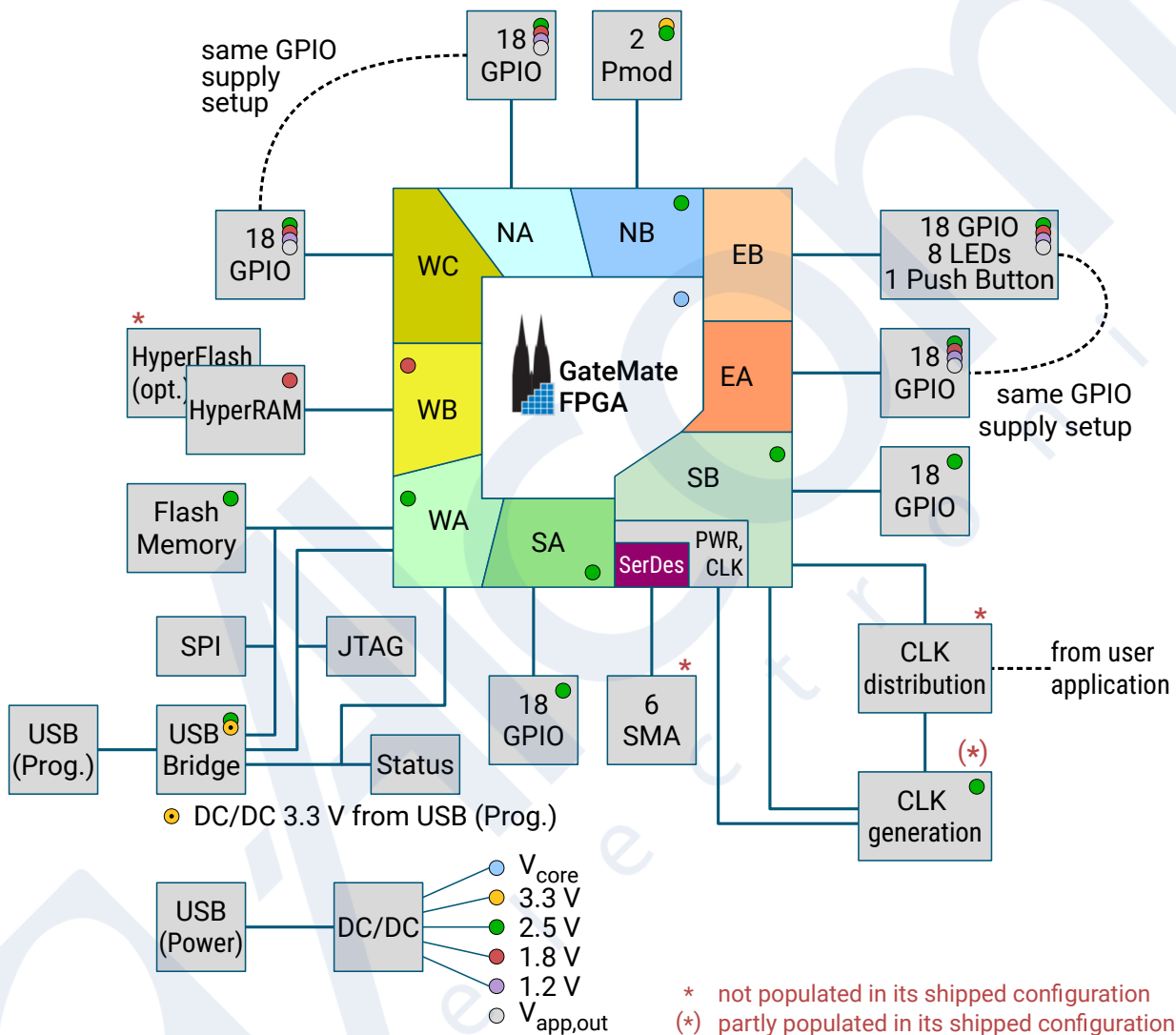
It serves as a reference design and for a direct entry into application development. It is the perfect starting point for all embedded designers as it features

- USB host access,
- JTAG interface,
- SPI interface,
- on-board flash memory,
- Serializer / Deserializer (SerDes) interface,
- Pmod-compatible interface,
- on-board HyperRAM module,
- 108 accessible general purpose input / outputs (GPIOs),
- 7 status LEDs.

The evaluation kit is available from Cologne Chip. Please visit our website for more information.

Figure 1.1 gives a brief overview of the evaluation board features. Some GPIO banks have fixed power level according to their function. Others can be configured to different voltages due to the user application requirements.

The printed circuit board (PCB) top view is shown in Figure 1.2. Please note, that some components are prepared for extended features and must be populated by the user, if needed.



**Figure 1.1:** Feature overview of the GateMate™ FPGA evaluation board version 3.1

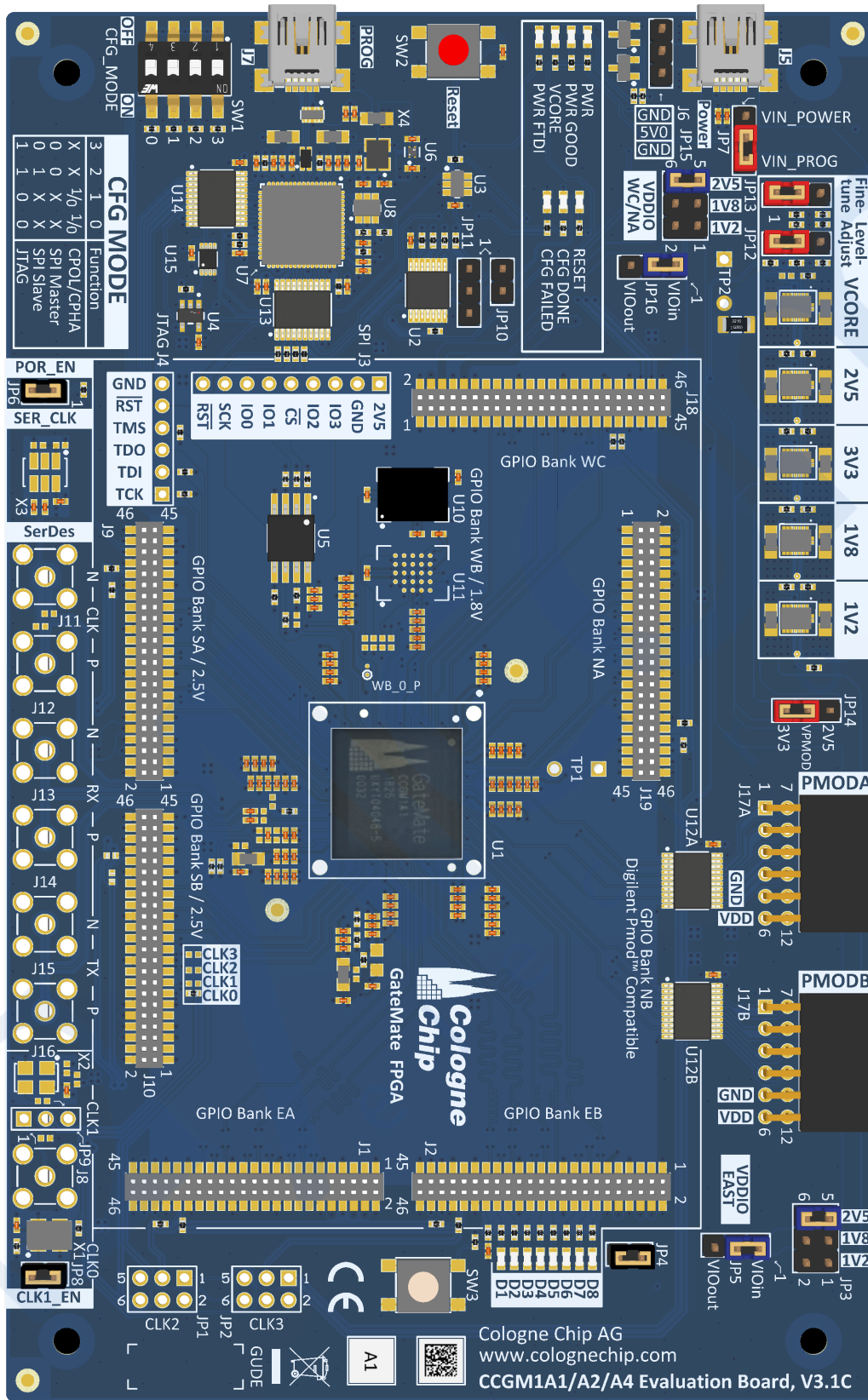


Figure 1.2: GateMate™ FPGA evaluation board version 3.1





# Chapter 2

## Startup

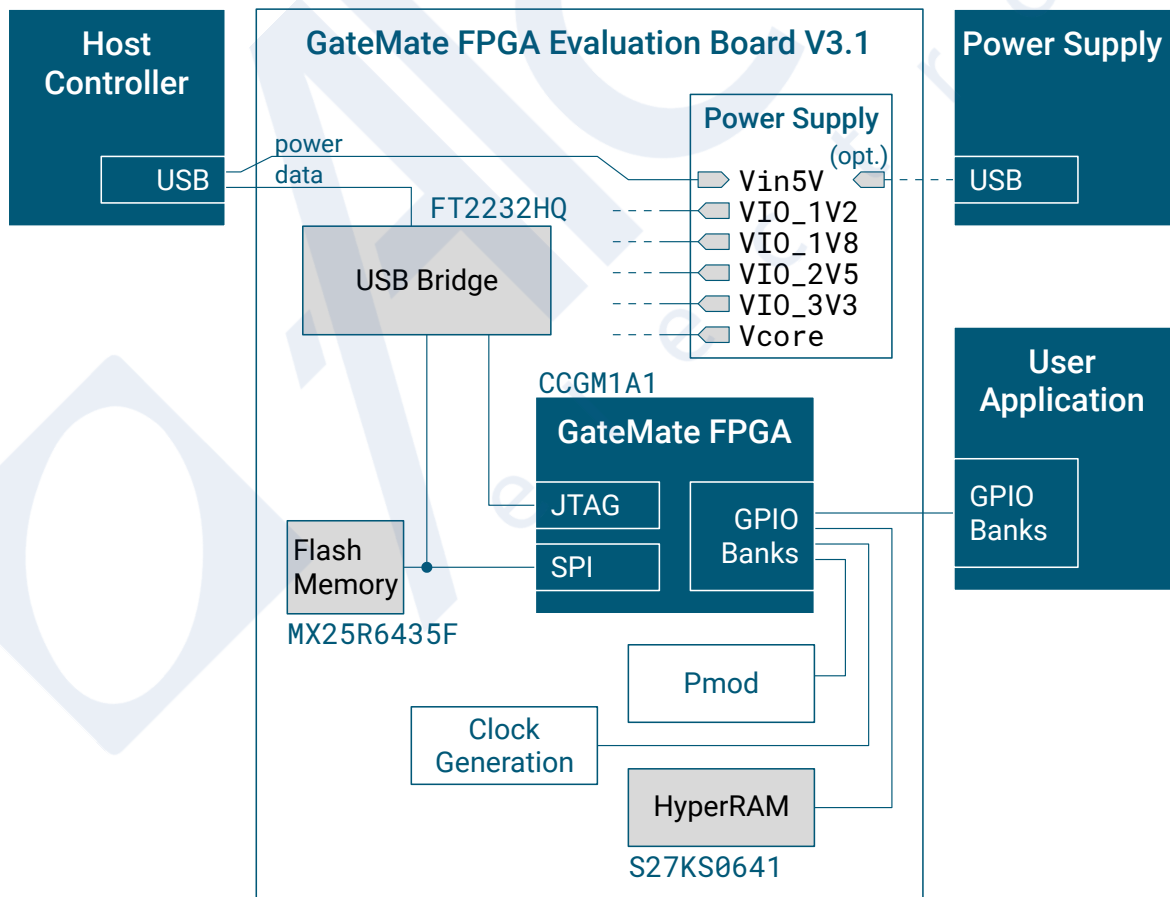


Figure 2.1: Block diagram of the GateMate™ FPGA evaluation board

## 2.1 Block Diagram

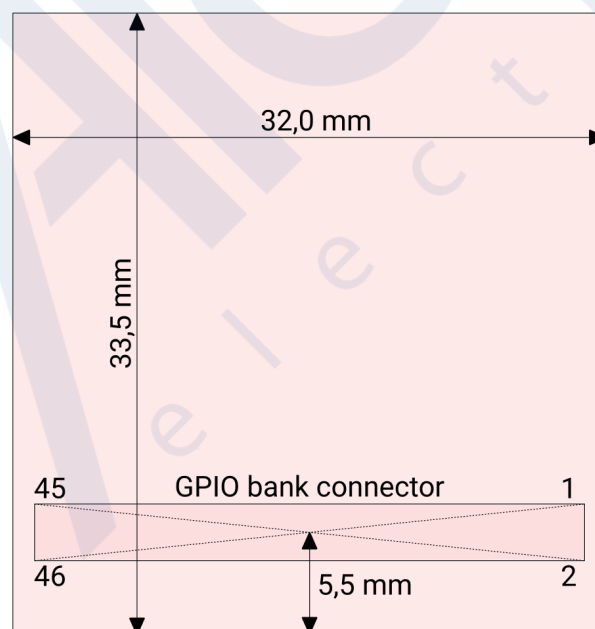
The GateMate™ FPGA evaluation board offers a quick access to the CCGM1A1 functions. Figure 2.1 gives a simplified overview of the printed circuit board (PCB) block diagram. A single supply voltage from any USB supply is typically used for powering the PCB and the user application.

The FPGA configuration can be loaded in two different ways. The on-board flash memory can automatically set up the FPGA configuration after reset. Alternatively, a host controller can be used to load the FPGA configuration. These functions and additional features on the SPI und JTAG interface are described in Chapter 3.3 from page 26.

The user application connects the general purpose input/output (GPIO) banks of the GateMate™ FPGA and some additional signals like reset and clock to fulfill further application requirements.

## 2.2 Connection to the User Application

The interface to the GPIO banks is implemented with 2-row 46-pin through-hole connectors with pin pitch 1.27 mm. The user application can use standard male pin header 2×23 to connect the GPIO banks and some further signals.



**Figure 2.2:** Recommended maximum dimensions of a user application PCB for a single GPIO bank and horizontal assembly (top view)

Due to through-hole technology, the user application can either be connected at the top side of the evaluation board, or it can be mounted below. It is usually advisable to assemble the user application on the top side for an easy access to the user circuitry. Then,

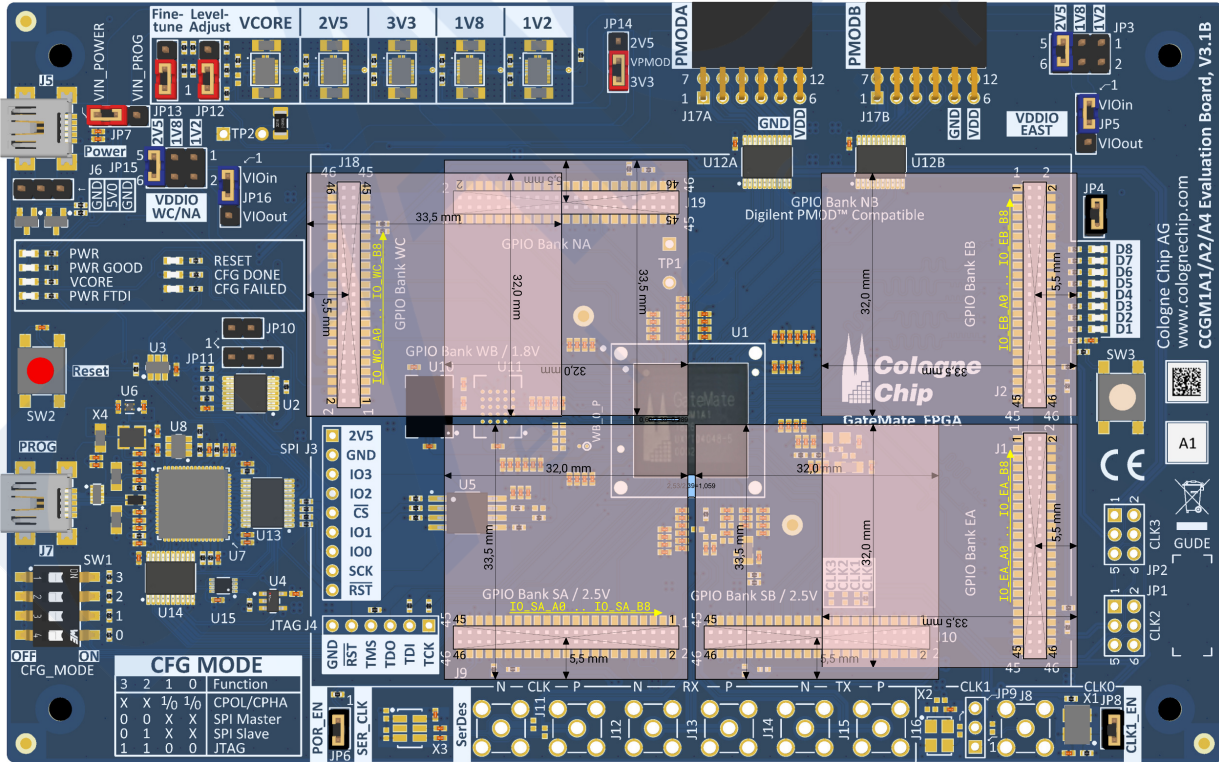
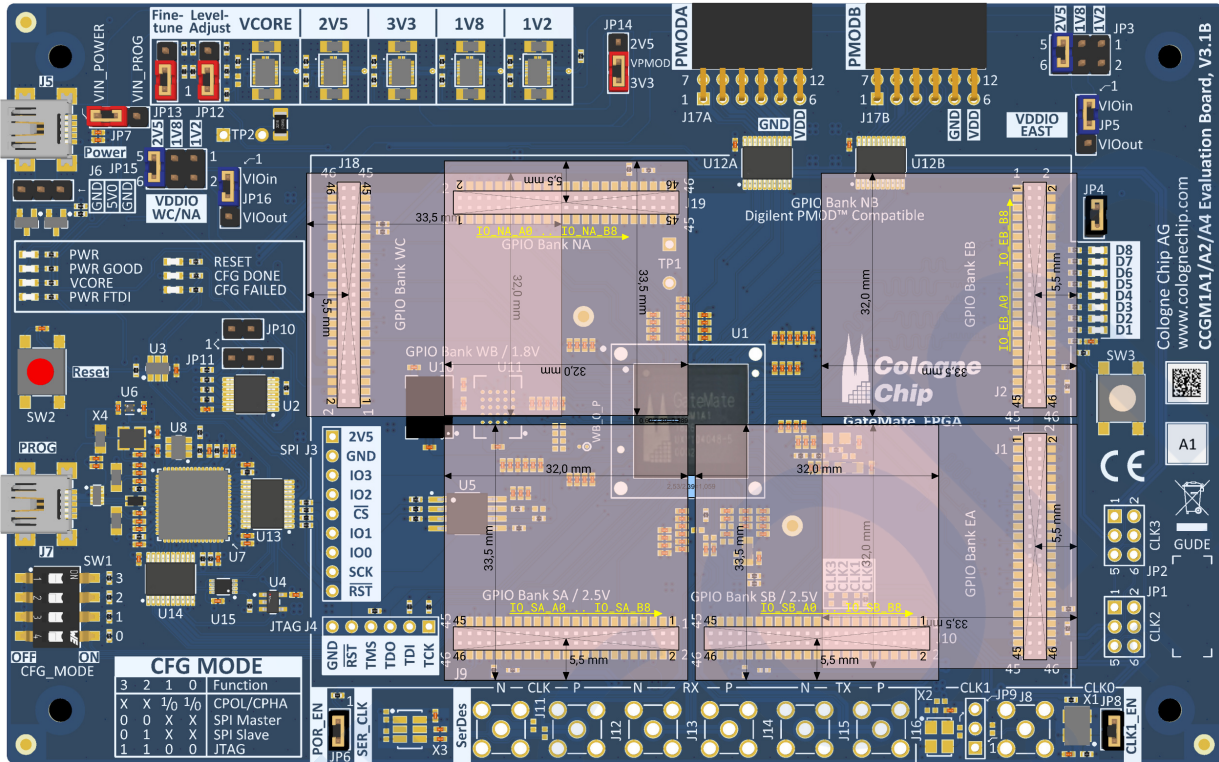


Figure 2.3: Examples of assembling several 1-bank user applications at the same time



it should be noted that all tall components are outside the rectangular area of the GPIO bank connectors.

For a user application with access to a single GPIO bank, e.g., the maximum PCB dimensions should not exceed 32.0×33.5 mm for horizontal assembly. Furthermore, the location of the GPIO pin header should be as shown in Figure 2.2. With this arrangement,

- a) the user PCB can be plugged onto every GPIO bank and
- b) several user PCBs can be used at the same time as shown in Figure 2.3.

When assembling the user PCB below the evaluation board there are no restrictions due to tall components.

When assembling the user PCB upright, there are no restrictions concerning the user PCB length. However, the specified width of 32.0 mm should not be exceeded.


For the design of user applications with more than one GPIO bank please see the evaluation board dimensions in Figure 5.1 on page 40.

## 2.3 Connection to the Host Controller

The GateMate™ FPGA Evaluation Board requires a computer with Linux or Windows operating system as follows:

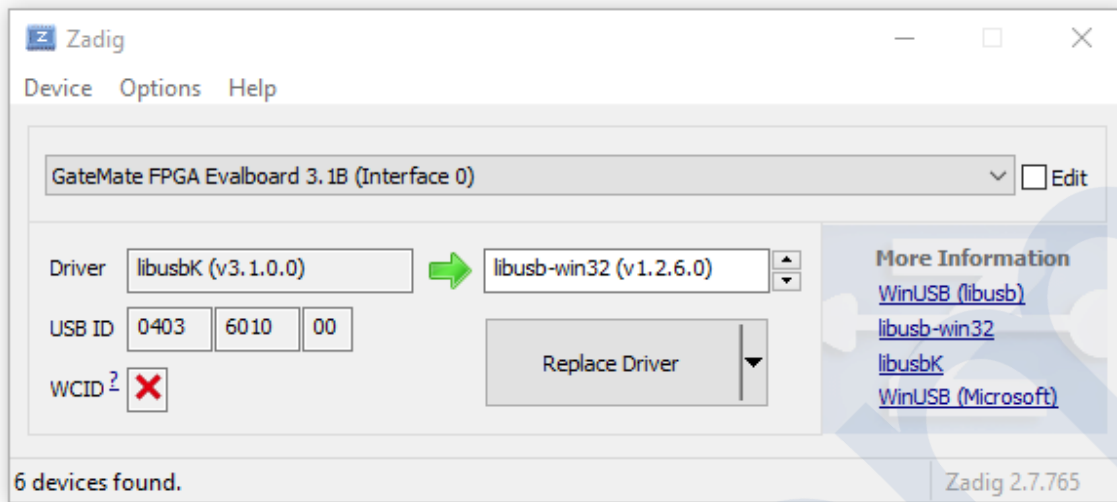
- Supported Linux environments:
  - Debian-based Linux (Debian, Ubuntu, ...) with apt package manager
  - Arch-based Linux (Arch, Manjaro, ...) with pacman package manager
  - Red Hat-based Linux (Fedora, ...) with dnf or yum package manager
- Windows environments:
  - Windows 7 or later, 64 bit
  - Zadig USB driver installer (<https://zadig.akeo.ie/>)

When first plugged into the computer's USB port, drivers should load by default.

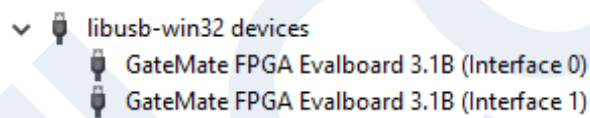
In Windows environments, it is necessary to install USB drivers using Zadig . Download the software and connect the GateMate™ Evaluation Board to your USB port. In the Zadig Window, select **Options > List All Devices** to refresh the device list. From the drop-down list, select **GateMate FPGA Evalboard 3.1B (Interface0)**. Now select **libusb-win32 (any version)** from the driver list and replace the drivers (see Figure 2.4).

Replacing drivers might take a moment. Repeat this procedure for interface 1. Your GateMate™ Evaluation Board should then be listed as **libusb-win32 devices** in the Device Manager as shown in Figure 2.5.

In Linux environments, drivers are automatically loaded correctly.



**Figure 2.4:** Zadig Window with selected GateMate™ FPGA Evaluation Board



**Figure 2.5:** GateMate™ FPGA Evaluation Board in Device Manager

The tool setup for the Cologne Chip GateMate™ series is described in the user guide **UG1002 – GateMate™ FPGA Toolchain Installation User Guide** [↗](#)



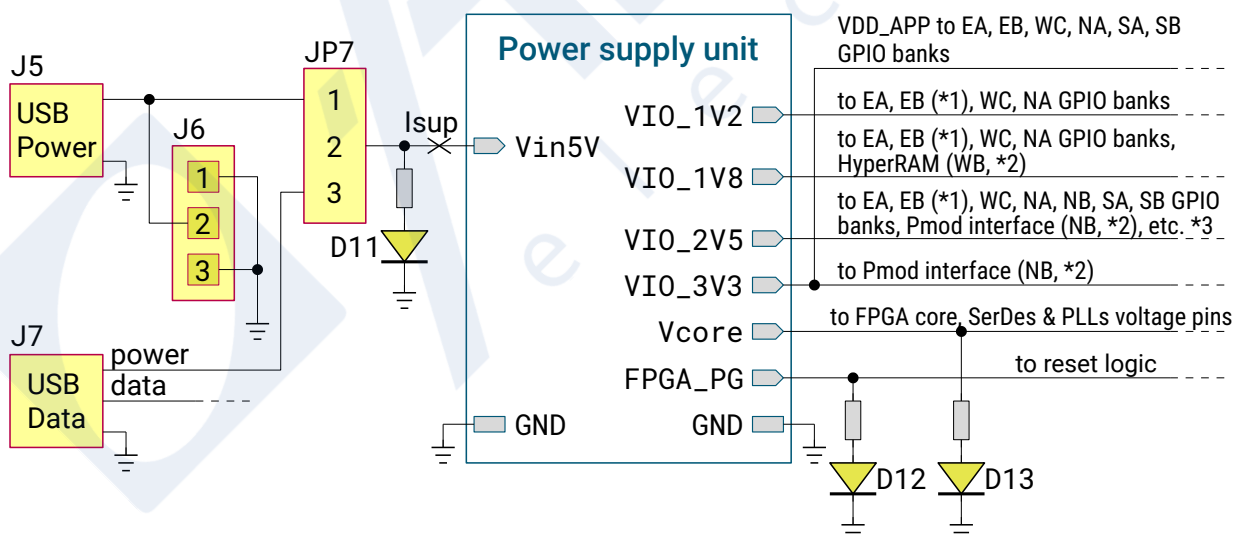


# Chapter 3

## GateMate™ FPGA Evaluation Board Functions

### 3.1 PCB Power Supply

The power supply unit consists of five DC-DC converters which offer all voltages to fulfill the requirements of a wide range of user applications. All converters are feed from a single source. Typically an USB supply can be used.

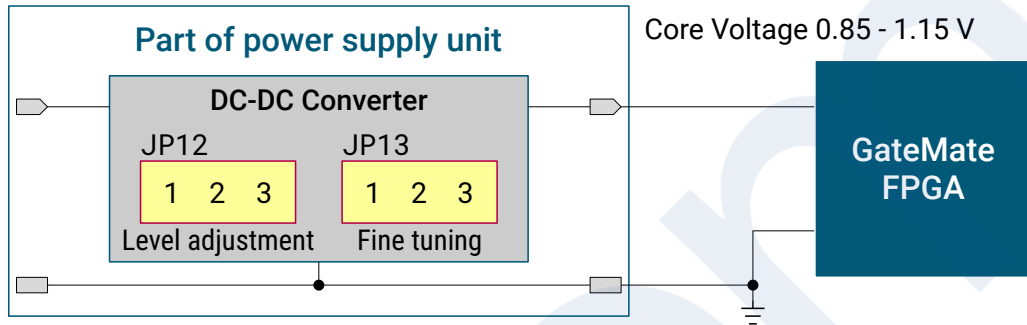


- \*1 including alternative use of 8 LEDs and 1 push button
- \*2 GPIO pins not available
- \*3 configuration bank (WA, \*2), clock generation, reset module

Figure 3.1: PCB power supply

Figure 3.1 shows that power supply can either be feed in from the USB connector J5 or it can be taken from the USB data connector J7 instead. Please ensure, that enough power can be delivered from the USB host.

Alternatively, power supply can be feed from any other source via connector J6. The required input voltage is 4.0 .. 6.0 V.



**Figure 3.2:** GateMate™ FPGA core voltage

The DC-DC converters have a fixed output voltage. Only the DC-DC converter for the FPGA core voltage can be adjusted as shown in the block diagram in Figure 3.2.

The FPGA core voltage can be set up to different levels for low power mode, economy mode or speed mode. Furthermore, typical voltage can be chosen as well as minimum and maximum levels. Jumper settings are described in Table 3.1.

**Table 3.1:** JP12 and JP13 jumper settings for FPGA core voltage

JP12	JP13	Core Voltage	Function
open	open	0.85 V	low power mode, min
open	1 - 2	0.90 V	low power mode, typical
open	2 - 3	0.95 V	low power mode, max
1 - 2	open	0.95 V	economy mode, min
1 - 2	1 - 2	1.00 V	economy mode, typical
1 - 2	2 - 3	1.05 V	economy mode, max
2 - 3	open	1.05 V	speed mode, min
2 - 3	1 - 2	1.10 V	speed mode, typical
2 - 3	2 - 3	1.15 V	speed mode, max



**Important note:**

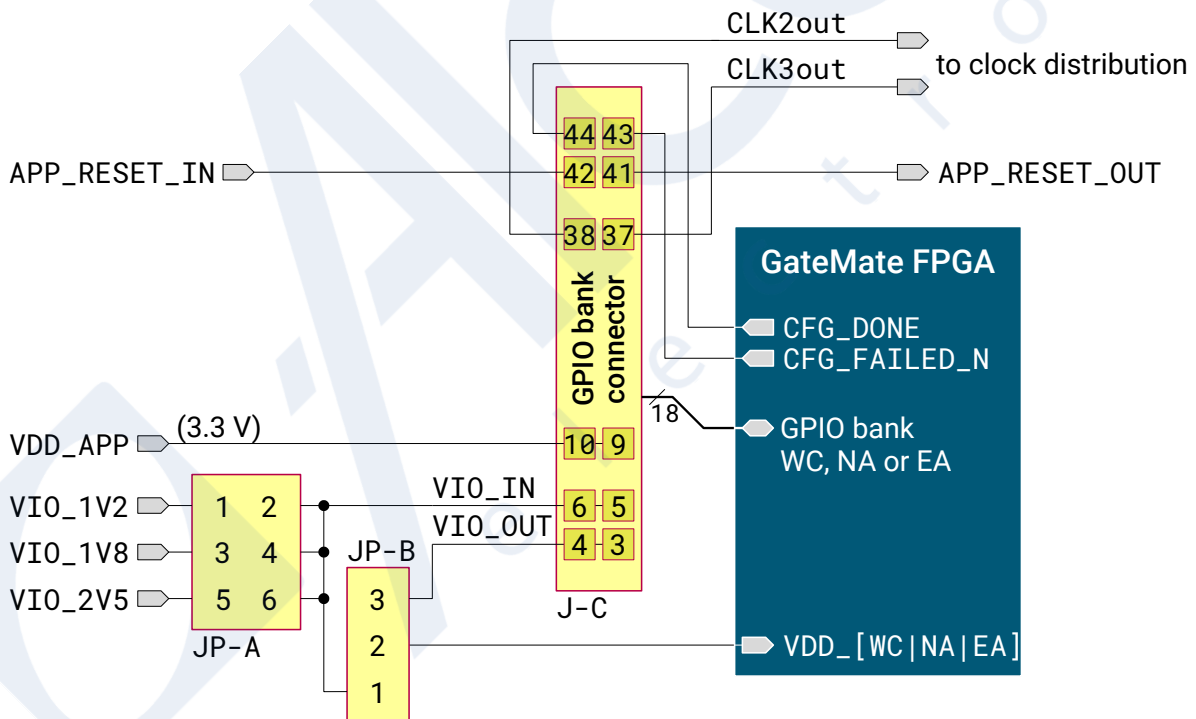
Please ensure to disconnect the power supply before changing the jumper settings to avoid damage of the devices.

### 3.2 GPIO Power Supply

The CCGM1A1 FPGA offers nine general purpose input / output (GPIO) banks. Their GPIO supply voltage is set up in different ways on the evaluation board as shown in Table 3.2.

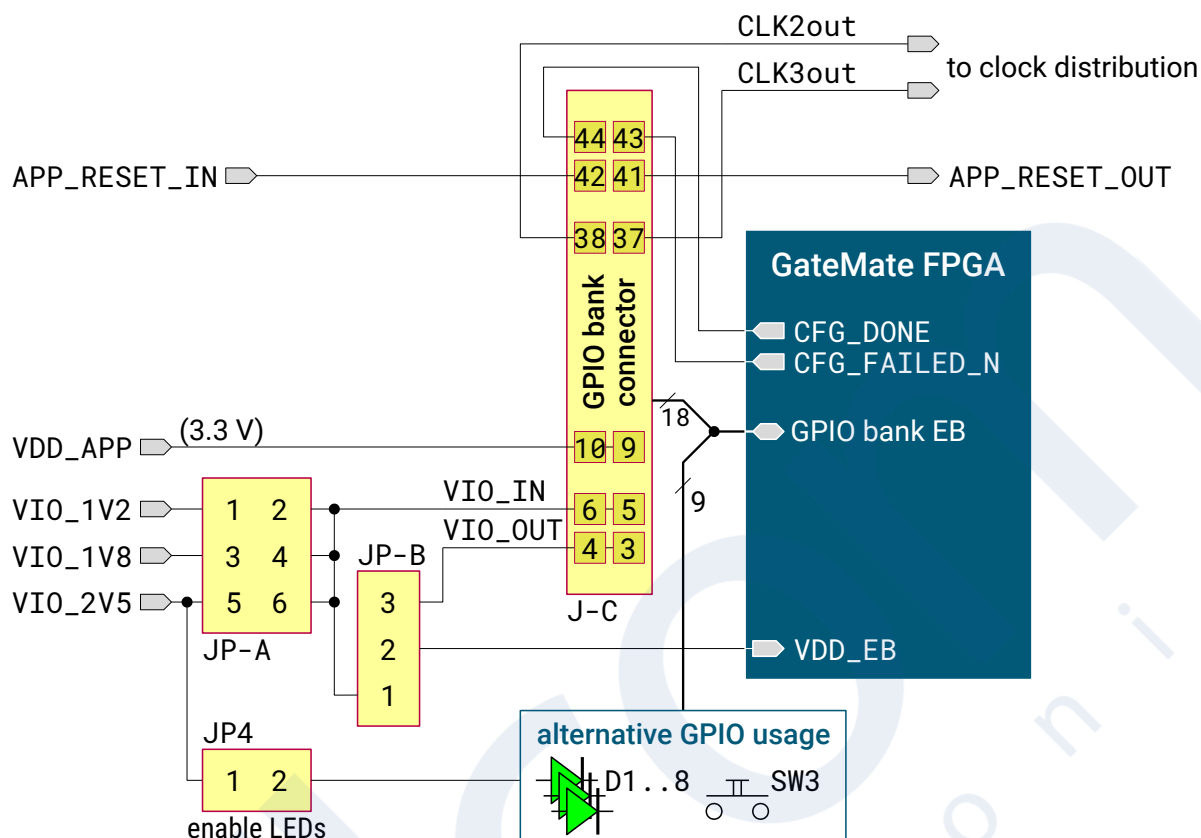
**Table 3.2:** Assignment of GPIO power supply scheme to GPIO banks

Figure	Page	GPIO banks	Scheme characteristics
3.3	23	WC, NA, EA	GPIO voltage selected from three on-board sources or the application voltage
3.4	24	EB	GPIO voltage selected from three on-board sources or the application voltage, additional functions (LEDs and user button)
3.5	25	SA, SB	Single 2.5 V voltage supply
–	–	WA	Configuration bank, 2.5 V supply
3.16	35	WB	HyperBus memory, 1.8 V supply
3.15	34	NB	Pmod interface, 2.5 V supply



**Figure 3.3:** GPIO supply with voltage selection

Figure 3.3 shows the configurable GPIO supply setup for GPIO banks WC, NA and EA. These banks can select one of three on-board voltages as well as VIO\_OUT feed from the user application. The selected on-board voltage is also feed to the user application (VIO\_IN) and can be used to supplement the separat VDD\_APP voltage.



**Figure 3.4:** GPIO supply with voltage selection and alternative LEDs and push button

The same GPIO supply scheme is available for GPIO bank EB but additional functionality is implemented for some GPIO signals as shown in Figure 3.4 and Table 3.3. Eight LEDs can be enabled with Jumper JP4 set. With open jumper, the normal GPIO function is available at connector J-C (J2). Switch SW3 has an on-board pull-up resistor, which should be

**Table 3.3:** Additional functions on GPIO bank EB

Component	GPIO	Funktion
D1	IO_EB_B1	<u>low</u> : on (green), <u>high</u> : off
D2	IO_EB_B2	ditto
D3	IO_EB_B3	ditto
D4	IO_EB_B4	ditto
D5	IO_EB_B5	ditto
D6	IO_EB_B6	ditto
D7	IO_EB_B7	ditto
D8	IO_EB_B8	ditto
SW3	IO_EB_B0	<u>pressed</u> : low, <u>unpressed</u> : high



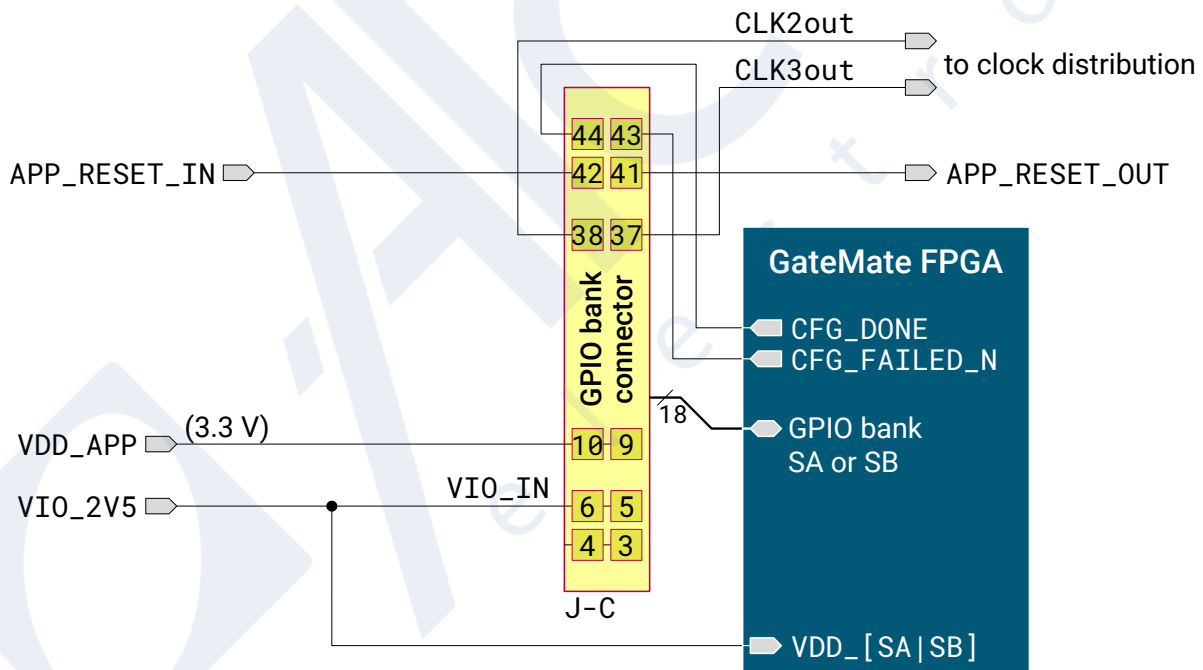
**Table 3.4:** Jumper JP-A, JP-B and connector J-C designators

Figure	JP-A	JP-B	J-C	GPIO bank
3.3 (page 23)	JP15	JP16	J18	WC
	JP15	JP16	J19	NA
	JP3	JP5	J1	EA
3.4 (page 24)	JP3	JP5	J2	EB
3.5 (page 25)	–	–	J9	SA
	–	–	J10	SB

taken into account when using the normal GPIO function instead. Table 3.3 shows the additional EB GPIO functions in detail.

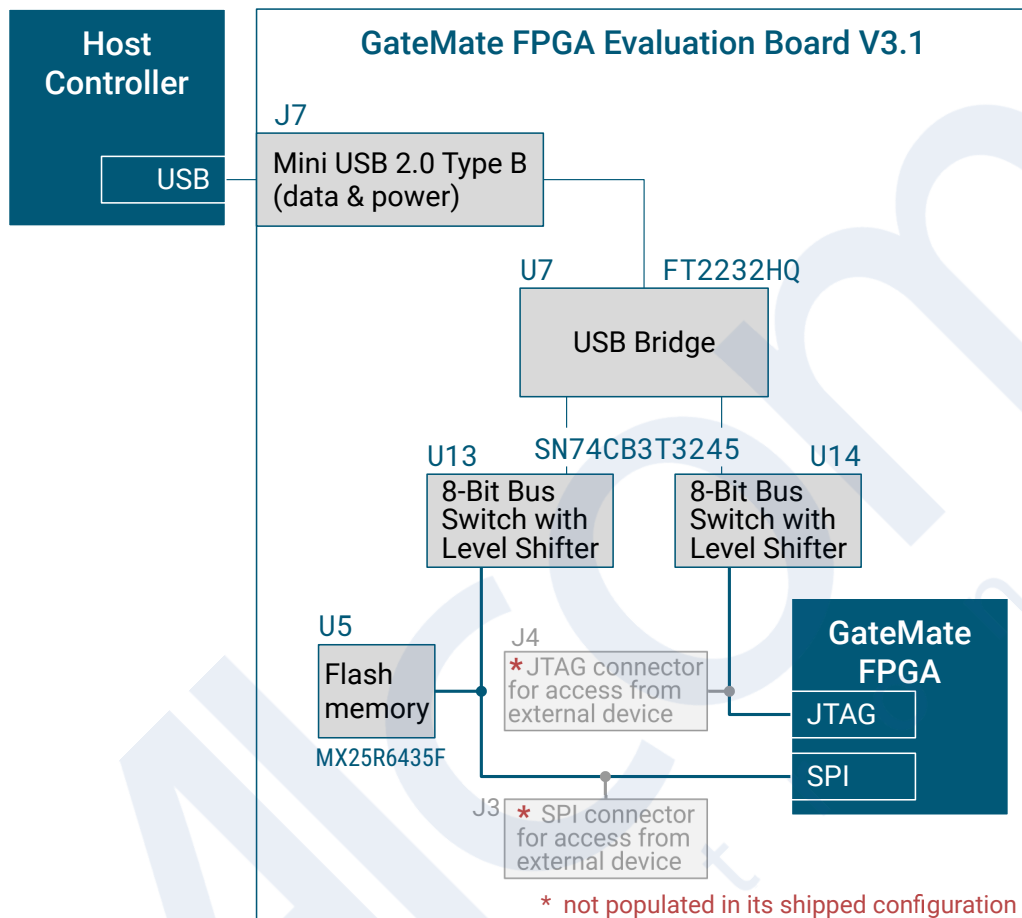
Table 3.4 gives an overview of jumpers JP-A and JP-B and connector J-C availability for the individual GPIO banks.

Finally, GPIO banks SA and SB have a fixed supply voltage 2.5 V (see Figure 3.5). Again, the user application supply is both, VDD\_APP and the GPIO voltage VIO\_2V5.



**Figure 3.5:** GPIO supply with single voltage

### 3.3 SPI and JTAG Data Busses



**Figure 3.6:** Block diagram with details of SPI and JTAG interfaces

The SPI bus can be accessed from any user device. For this, connector J3 (2.54 mm pin pitch, 9 pins) has to be populated. Figure 3.7 shows the pin assignment of the SPI connector.

The JTAG interface can be accessed from any user device. For this, connector J4 (2.54 mm pin pitch, 6 pins) has to be populated. Figure 3.8 shows the pin assignment of the JTAG connector.

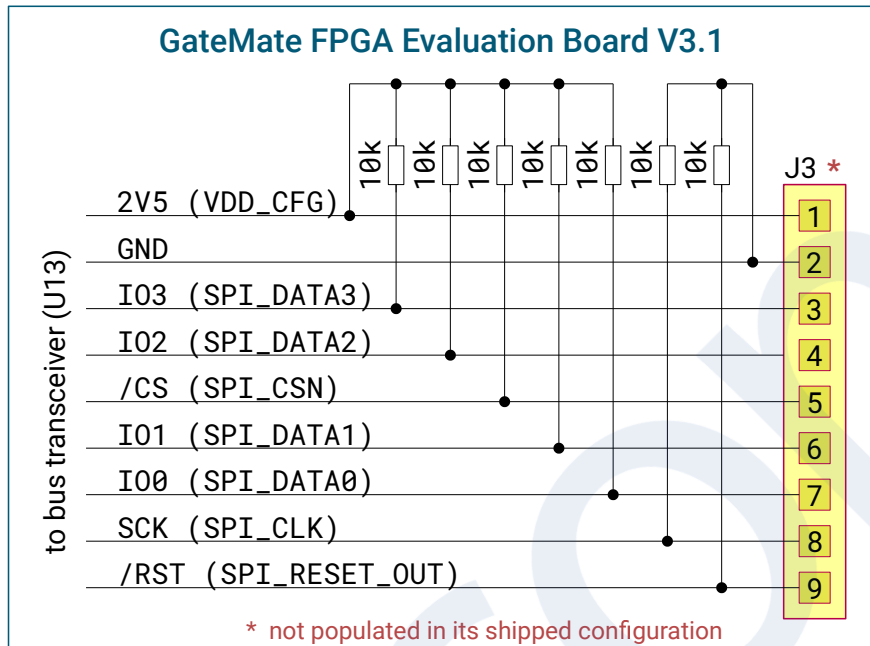


Figure 3.7: Optional SPI interface connector J3

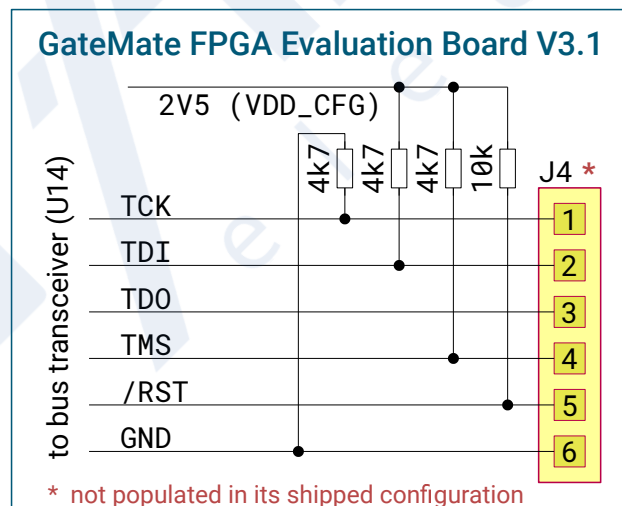


Figure 3.8: Optional JTAG interface connector J4

### 3.4 Configuration Mode and Reset

There are several ways to load the FPGA configuration. The configuration mode is chosen with switch SW1 setup as shown in Table 3.5.

**Table 3.5:** GateMate™ FPGA configuration modes

CFG_MD[3:0] *	Configuration mode
0x0 0b0000	SPI Master Mode CPOL = 0, CPHA = 0
0x1 0b0001	SPI Master Mode CPOL = 0, CPHA = 1
0x2 0b0010	SPI Master Mode CPOL = 1, CPHA = 0
0x3 0b0011	SPI Master Mode CPOL = 1, CPHA = 1
0x4 0b0100	SPI Slave Mode CPOL = 0, CPHA = 0
0x5 0b0101	SPI Slave Mode CPOL = 0, CPHA = 1
0x6 0b0110	SPI Slave Mode CPOL = 1, CPHA = 0
0x7 0b0111	SPI Slave Mode CPOL = 1, CPHA = 1
0xC 0b1100	JTAG

\* Modes not mentioned in the list may not be selected and lead to a malfunction of the device.

FPGA reset depends on different conditions:

- The user can press button SW2 to trigger FPGA reset.
- After power-on, all DC-DC converters must notify 'power good' to finish reset state.
- The host controller can trigger reset via SPI or JTAG interface. In this case either level shifter U13 or U14 will feed the host's reset signal to the GateMate™ FPGA.
- An external SPI device can feed a reset signal to the FPGA via the SPI connector J3 pin 9 (see Figure 3.7).
- An external JTAG device can feed a reset signal to the FPGA via the JTAG connector J4 pin 5 (see Figure 3.8).
- The user application can trigger FPGA reset via GPIO bank connector J-C pin 41 (APP\_RESET\_OUT). This signal can be disabled via Jumper JP10.

The GPIO bank connector feeds a reset signal APP\_RESET\_IN to the user application. This is either the reset button SW2 or any reset condition mentioned above (see Figure 3.9).

Every GPIO bank connector has a APP\_RESET\_OUT signal. These are all connected together and are called 'User application reset out' in Figure 3.9.

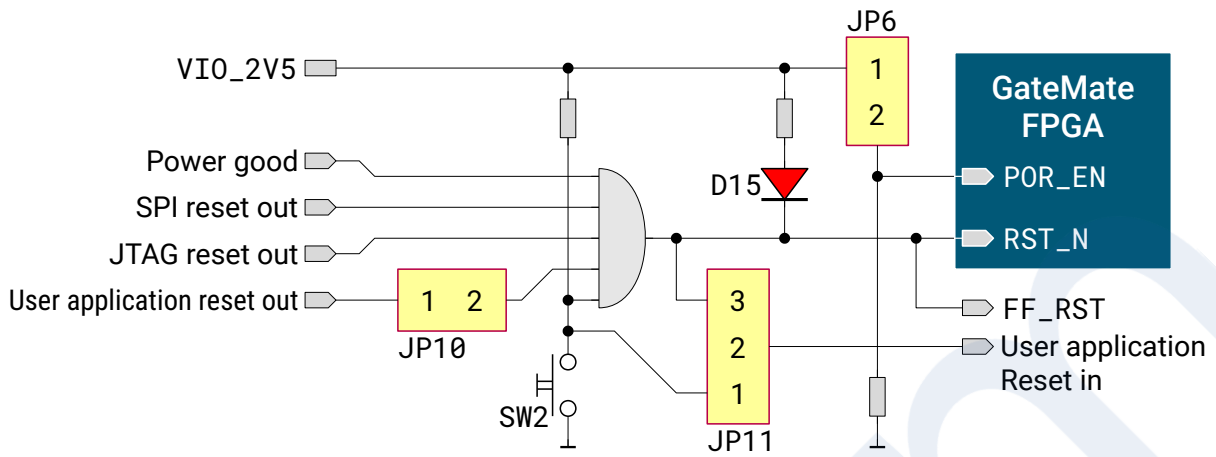


Figure 3.9: Reset module

After configuration, the GateMate™ FPGA reports whether the data stream was successfully loaded or not.

- LED D10 (green) is switched on when the data stream has completely been transferred.
- LED D9 (red) is switched on when an error occurred.

Both signals are also passed to the host controller as shown in Figure 3.10. In case of an failed loading, a reset should be triggered in order to load the data stream again.

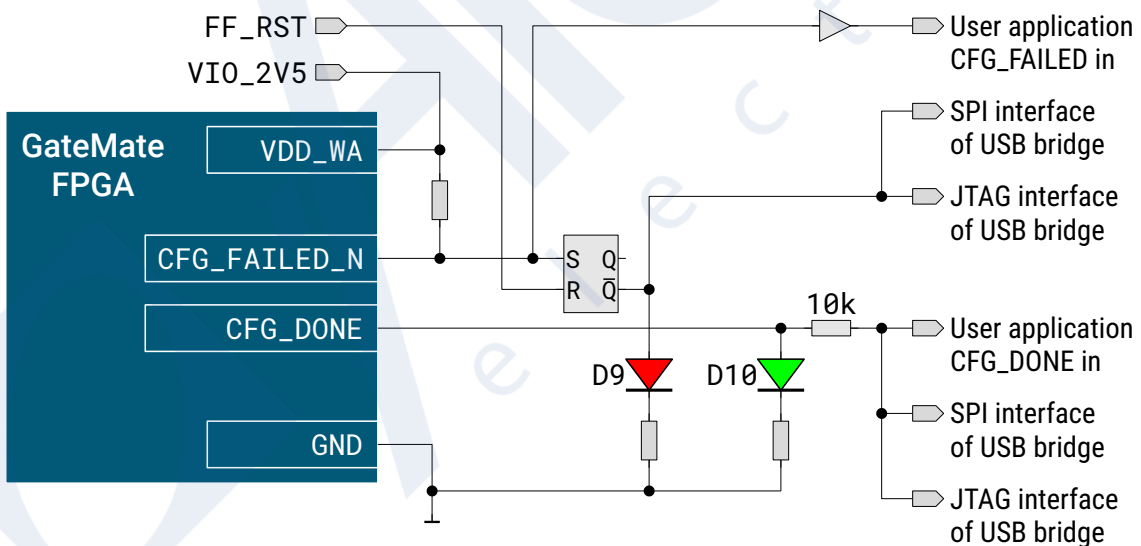


Figure 3.10: Configuration status signals



### 3.5 Clock Generation and Distribution

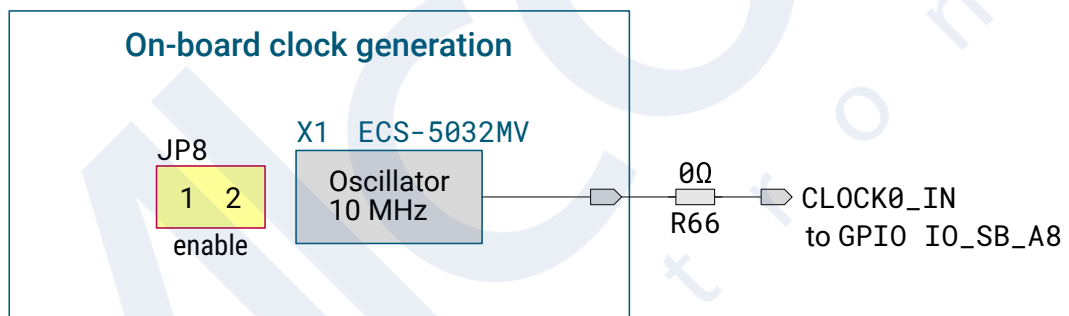
The evaluation board has an on-board oscillator X1 with 10.000 MHz frequency. This signal is connected to GPIO IO\_SB\_A8 which is the input for clock 0 (see Figure 3.11). The oscillator can be disabled with jumper JP8.

The GateMate™ FPGA has three more clock inputs connected to the GPIO WA bank. The evaluation board has these clocks prepared for usage, but some components have to be populated by the user as shown in Figure 3.13.

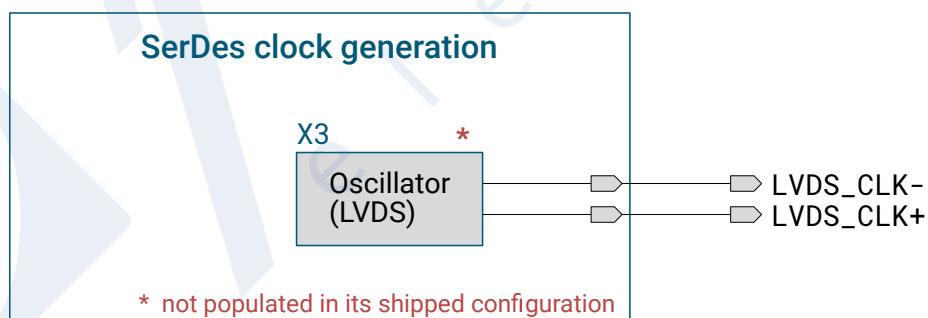
**Clock 1:** Another oscillator can be populated or an external clock source can be used via SMA jack J8.

**Clock 2 and 3:** The user application can feed two clock signals to the FPGA inputs. Jumpers JP1 and JP2 must be populated to select the clock source.

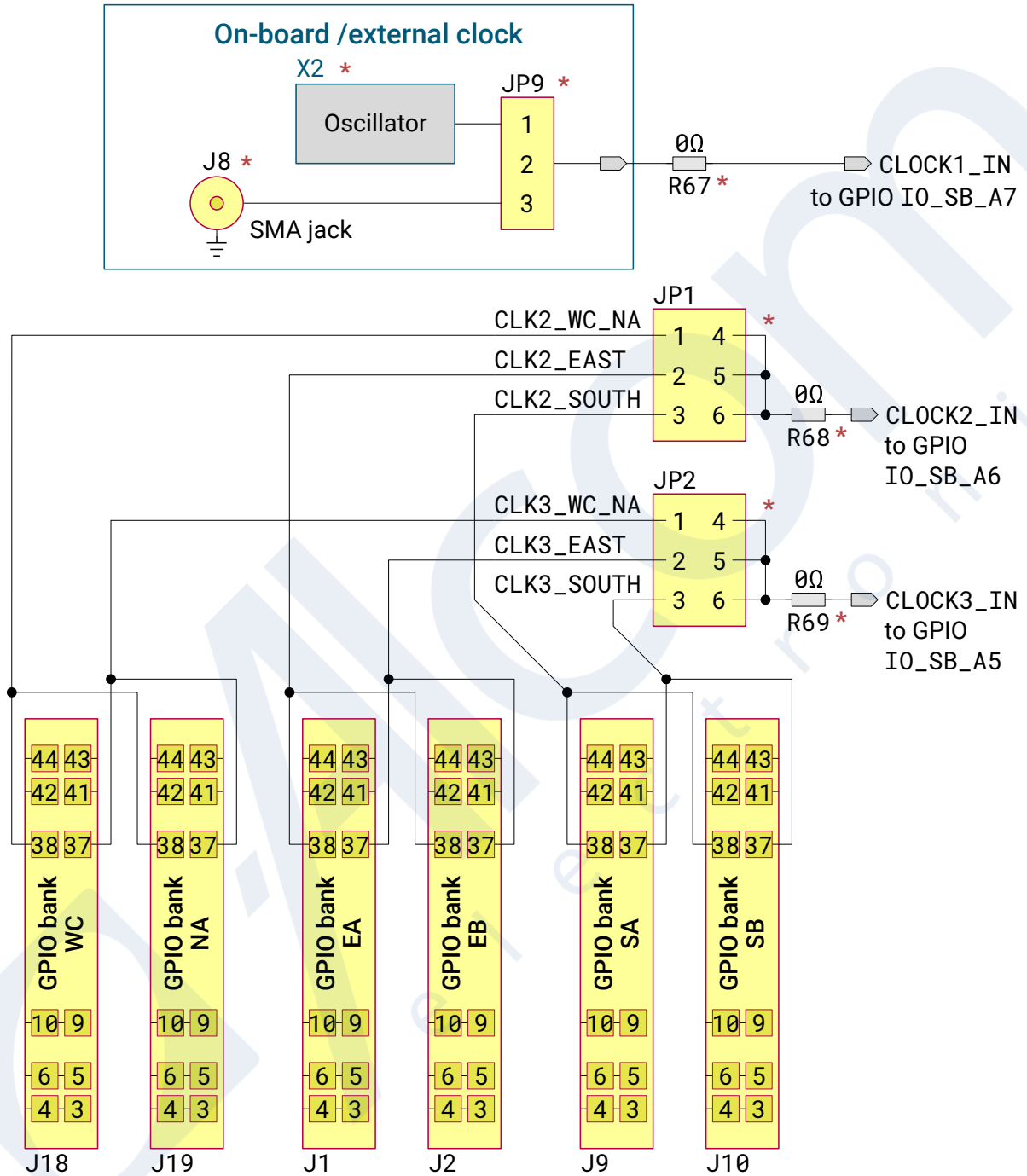
Finally, a low-voltage differential signaling (LVDS) clock oscillator can be populated to generate a Serializer / Deserializer (SerDes) input clock as shown in Figure 3.12. Please note, that also series resistors R73 and R74 have to be populated (see Figure 3.17 on page 36).



**Figure 3.11:** 10 MHz on-board clock oscillator



**Figure 3.12:** Optional SerDes clock (LVDS clock oscillator)



\* not populated in its shipped configuration

Figure 3.13: Optional clock signals

### 3.6 GPIO Connection to the User Application

The user application can be connected to one or more GPIO banks. Up to 6 banks are available. The other GPIO banks are assigned elsewhere.

All GPIO bank connectors have the same pinout as shown in Figure 3.14. Please note, that the GPIOs are arranged in two different ways with overturned signal vector. This is done to allow free choice of a GPIO bank for 1-bank user applications as shown in Figure 2.3 on page 17 and differential signal routing on the evaluation board at the same time. The PCB routing of all GPIO signals of banks EA and EB are inter-pair as well as intra-pair length matched.

The user application can get its power supply from the 3.3 V on-board DC-DC converter. In addition, GPIO voltage can be feed from the evaluation board to the user application or vice versa. Table 3.7 explains these VI0in and VI0out supply lines. The overall list of the GPIO bank connectors J-C is given in Table 3.6.

GPIO bank connector					
GND	46	45	GND		
CFGD	44	43	CFGF		
RSTin	42	41	RSTout		
GND	40	39	GND		
CLK2out	38	37	CLK3out		
GND	36	35	GND		
S / E: B[0]	W / N: B[8]	34	33	W / N: A[8]	S / E: A[0]
B[1]	B[7]	32	31	A[7]	A[1]
B[2]	B[6]	30	29	A[6]	A[2]
GND	28	27	GND		
S / E: B[3]	W / N: B[5]	26	25	W / N: A[5]	S / E: A[3]
B[4]	B[4]	24	23	A[4]	A[4]
B[5]	B[3]	22	21	A[3]	A[5]
GND	20	19	GND		
S / E: B[6]	W / N: B[2]	18	17	W / N: A[2]	S / E: A[6]
B[7]	B[1]	16	15	A[1]	A[7]
B[8]	B[0]	14	13	A[0]	A[8]
GND	12	11	GND		
Vapp	10	9	Vapp		
GND	8	7	GND		
VI0in	6	5	VI0in		
VI0out	4	3	VI0out		
GND	2	1	GND		

J-C

W / N: GPIO banks WC and NA

S / E: GPIO banks SA, SB, EA and EB

Reset, clock, configuration status

GPIO bank

Power supply

Figure 3.14: GPIO bank connector J-C

**Table 3.6:** Pin assignment of GPIO connector J-C

J-C pin	J-C signal	Schematic signal	Funktion
3 , 4	VI0out		see Table 3.7
5 , 6	VI0in		see Table 3.7
9 , 10	Vapp	VDD_APP	VI0_3V3 from power module
13 .. 33 <sup>1</sup>	A[8:0] or vice versa		to / from FPGA GPIO bank
14 .. 34 <sup>2</sup>	B[8:0] or vice versa		dto.
37	CLK3out		<ul style="list-style-type: none"> <li>• 3 different signal pairs WC &amp; NA, SA &amp; SB and EA &amp; EB from J-C connectors</li> <li>• to clock distribution jumper block JP2</li> </ul>
38	CLK2out		<ul style="list-style-type: none"> <li>• dto.</li> <li>• to clock distribution jumper block JP1</li> </ul>
41	RSTout	APP_RESET_OUT	<ul style="list-style-type: none"> <li>• from 6 GPIO connectors J-C</li> <li>• to reset circuitry via JP10</li> </ul>
42	RSTin	APP_RESET_IN	<ul style="list-style-type: none"> <li>• from JP11 of reset circuitry</li> <li>• to 6 GPIO connectors J-C</li> </ul>
43	CFGF	CFG_FAILED_APP	<ul style="list-style-type: none"> <li>• from FPGA pin CFG_FAILED_N</li> <li>• to 6 GPIO connectors J-C and FTDI chip (latched with flip-flop) via bus transceiver</li> </ul>
44	CFGD	CFG_DONE_APP	<ul style="list-style-type: none"> <li>• from FPGA pin CFG_DONE</li> <li>• to 6 GPIO connectors J-C and FTDI chip via bus transceiver</li> </ul>

<sup>1</sup> odd only, pins 19 and 27 are GND

<sup>2</sup> even only, pins 20 and 28 are GND

**Table 3.7:** Power input and output of GPIO connector J-C in Figures 3.3, 3.4 and 3.5 (pages 23 to 25)

J-C	GPIO bank	VI0in	VI0out
J1	EA	from JP3 (selection)	to JP5, supply option for FPGA GPIO banks
J2	EB	dto.	dto.
J9	SA	VI0_2V5 from power module	not connected
J10	SB	dto.	dto.
J18	WC	from JP15 (selection)	to JP16, supply option for FPGA GPIO banks
J19	NA	dto.	dto.

### 3.7 Pmod Interface

GPIO bank NB constitutes a Pmod interface with two standard 12-pin connectors J17A and J17B.

Supply voltage 3.3 V should be selected via jumper JP14 to fulfill Pmod specification. If desired for certain applications, 2.5 V supply can be chosen exceptionally. Please note, that many Pmod devices will not work properly in this case.

Table 3.8 shows the GPIO signals connected to the Pmod interface connectors J17A and J17B.

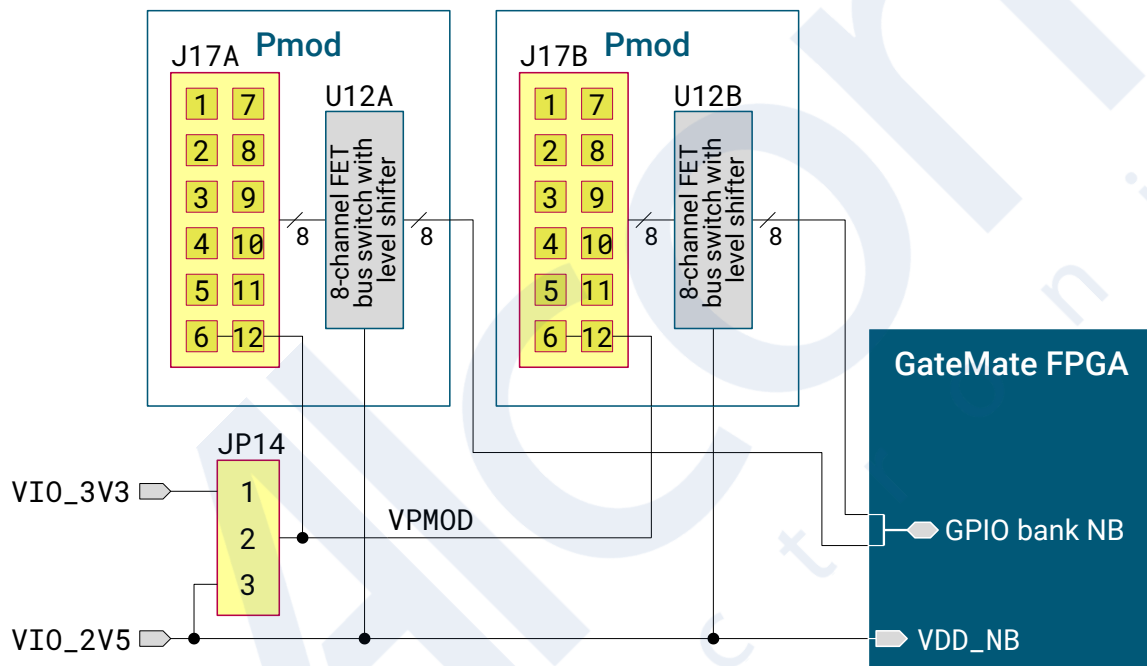


Figure 3.15: GPIO bank NB with Pmod interface

Table 3.8: Pmod signal assignment of J17A and J17B connectors

J17 pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B	J17 pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B
1	IO1	IO_NB_A0	IO_NB_A4	7	IO2	IO_NB_B0	IO_NB_B4
2	IO3	IO_NB_A1	IO_NB_A5	8	IO4	IO_NB_B1	IO_NB_B5
3	IO5	IO_NB_A2	IO_NB_A6	9	IO6	IO_NB_B2	IO_NB_B6
4	IO7	IO_NB_A3	IO_NB_A7	10	IO8	IO_NB_B3	IO_NB_B7
5	GND			11	GND		
6	VPMOD			12	VPMOD		



### 3.8 HyperRAM Device

GPIO bank WB is used to provide an on-board HyperRAM memory (see Figure 3.16). U10 is a 64 Mb device which is connected to the GPIO bank as shown in Table 3.9.

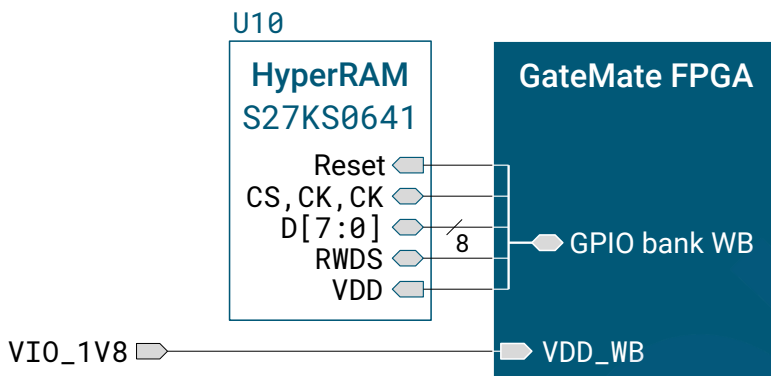


Figure 3.16: GPIO bank WB with HyperRAM device

Table 3.9: GPIO assignment to the on-board HyperRAM device

GPIO	HyperRAM signal	GPIO	HyperRAM signal
IO_WB_A0	–	IO_WB_B0	$\overline{CS}$
IO_WB_A1	–	IO_WB_B1	–
IO_WB_A2	$\overline{RESET}$	IO_WB_B2	–
IO_WB_A3	CK	IO_WB_B3	$\overline{CK}$
IO_WB_A4	–	IO_WB_B4	RWDS
IO_WB_A5	DQ0	IO_WB_B5	DQ1
IO_WB_A6	DQ2	IO_WB_B6	DQ3
IO_WB_A7	DQ4	IO_WB_B7	DQ5
IO_WB_A8	DQ6	IO_WB_B8	DQ7

### 3.9 SerDes Interface

The evaluation board is prepared to offer a SerDes interface. Figure 3.17 shows, that the SMA jacks J13 .. J16 must be populated from the user to get access to the CCGM1A1 SerDes interface.

There are two ways to feed in the SerDes clock signal:

1. SMA jacks J11 and J12 are populated to feed in an external LVDS clock.
2. An on-board LVDS oscillator and the series resistors R73 and R74 are populated (see also Figure 3.12 on page 30).

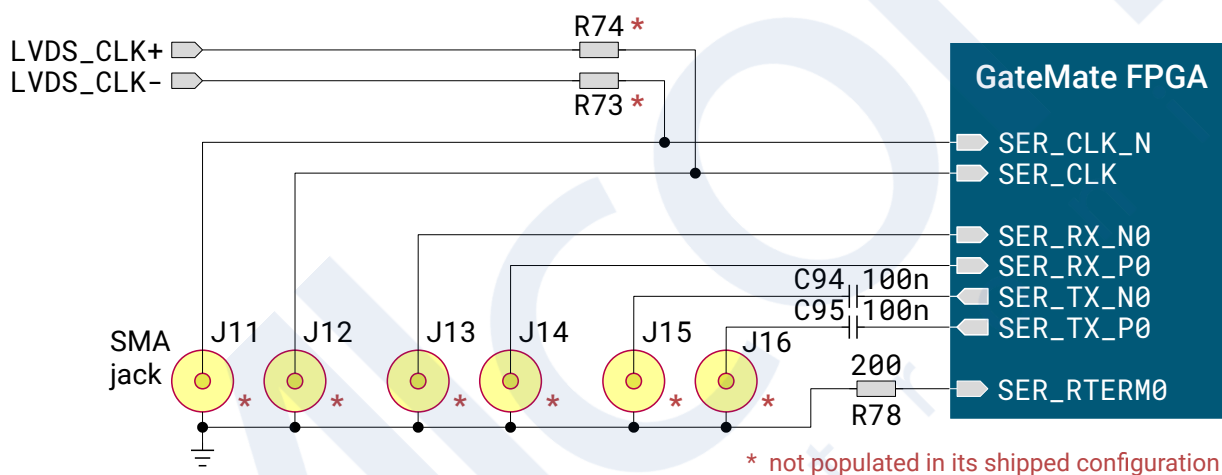


Figure 3.17: Optional SerDes interface

# Chapter 4

## Electrical Characteristics

**Table 4.1:** Absolute maximum characteristics of the GateMate™ FPGA evaluation board

Symbol	Min	Typ	Max	Unit	Description
	-40		125	°C	Junction temperature
$V_{in}$	-0.3		6.5	V	Power supply from J5 or J6
$V_{in}$	-0.3		6.0	V	Power supply from J7
$T_{stg}$	-55		150	°C	Storage temperature

**Table 4.2:** Operating characteristics of the GateMate™ FPGA evaluation board

Symbol	Min	Typ	Max	Unit	Description
	-40		85	°C	Operating temperature
$V_{in}$	4.0		6.0	V	Power supply from J5 or J6
$V_{in}$	4.75		5.75	V	Power supply from J7
$I_{in}$		140		mA	Power consumption during reset

**Table 4.3:** GPIO characteristics in single-ended mode

Symbol	Min	Typ	Max	Unit	Description
VDD <sub>IO</sub>	1.1		2.7	V	I/O supply voltage (GPIO banks and VDD_CLK)
V <sub>IN</sub>	-0.4		VDD <sub>IO</sub> + 0.4	V	Input voltage range
Schmitt-trigger function disabled:					
V <sub>IH</sub>	0.43		0.51	VDD <sub>IO</sub>	Input high threshold voltage
V <sub>IL</sub>	0.45		0.51	VDD <sub>IO</sub>	Input low threshold voltage
V <sub>HYST</sub>		0		V	Hysteresis
Schmitt-trigger function enabled:					
V <sub>IH</sub>	0.61		0.67	VDD <sub>IO</sub>	Input high threshold voltage
V <sub>IL</sub>	0.31		0.39	VDD <sub>IO</sub>	Input low threshold voltage
V <sub>HYST</sub>	0.26		0.33	VDD <sub>IO</sub>	Hysteresis
Output driver disabled:					
I <sub>IL</sub>			1	μA	Input pin current when driven active low
I <sub>IH</sub>			1	μA	Input pin current when driven active high
R <sub>PU</sub>		50		kΩ	Pull-up resistance
R <sub>PD</sub>		50		kΩ	Pull-down resistance
I <sub>DD,max</sub>			158	μA	Maximum supply current at GPIO input at transition point

**Table 4.4:** GPIO characteristics in LVDS mode

Symbol	Min	Typ	Max	Unit	Description
VDD <sub>IO</sub>	1.62		2.75	V	I/O supply voltage
I <sub>out</sub>		3.2		mA	Output current when LVDS output current boost is set to nominal current
I <sub>out</sub>		6.4		mA	Output current when LVDS output current boost is set to increased output current
VCM <sub>TX</sub>		VDD <sub>IO</sub> /2		V	Common-mode voltage
R <sub>term</sub>	90	100	130	Ω	

# Chapter 5

## Mechanical Dimensions



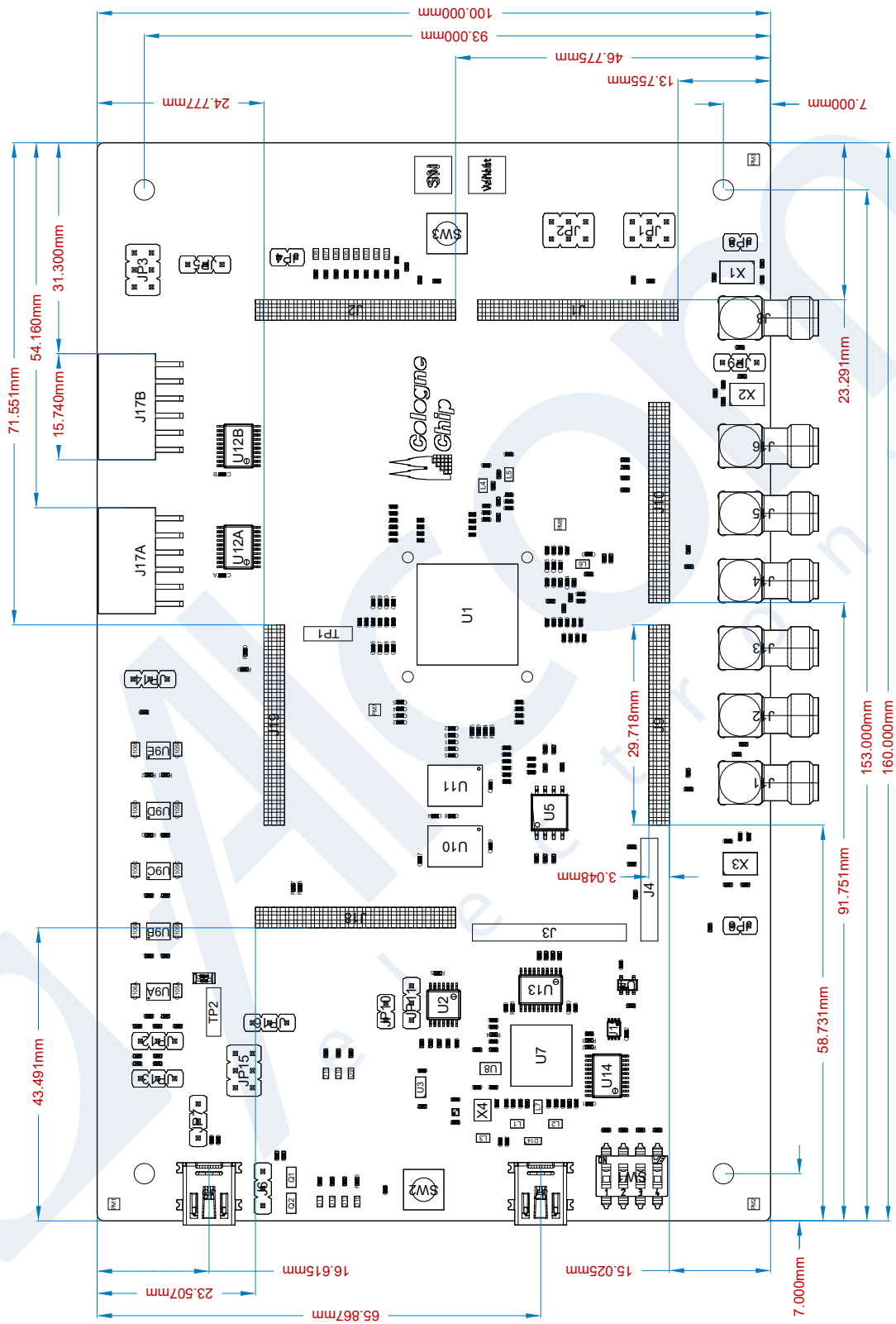


Figure 5.1: Board dimensions and position of connectors



# Appendix A

## Summary Overviews



## A.1 PCB components

Figure A.1 points out partial circuits that have been described in the previous chapters. The corresponding Table A.1 lists all associated Figures and where they can be found in this document.

**Table A.1:** Component locations on the GateMate™ FPGA evaluation board (numbering in counter clockwise order)

Marking	Function	Shown in Fig.	on Page
①	FPGA core voltage	3.2	22
②	PCB power supply	3.1	21
③	GPIO supply voltage selection (banks WC and NA)	3.3	23
④	Configuration status (LEDs for CFG_DONE and CFG_FAILED_N)	3.10	29
⑤	Reset	3.9	29
⑥	HyperRam device	3.16	35
⑦	USB bridge	3.6	26
⑧	Flash memory	3.6	26
⑨	SPI interface	3.6, 3.7	26, 27
⑩	JTAG interface	3.6, 3.8	26, 27
⑪	Configuration mode setup	Tab. 3.5	28
⑫	Power-on reset (POR) enable	3.9	29
⑬	SerDes LVDS clock	3.12	30
⑭	SerDes interface	3.17	36
⑮	GateMate™ FPGA CCGM1A1	1.1	12
⑯	On-board oscillator CLOCK0_IN	3.11	30
⑰	Optional clock signals CLOCK1_IN .. CLOCK3_IN	3.13	31
⑱	GPIO supply voltage selection (banks EA and EB) with alternative LEDs and push button on bank EB	3.3	23
⑲	Pmod interface	3.15	34

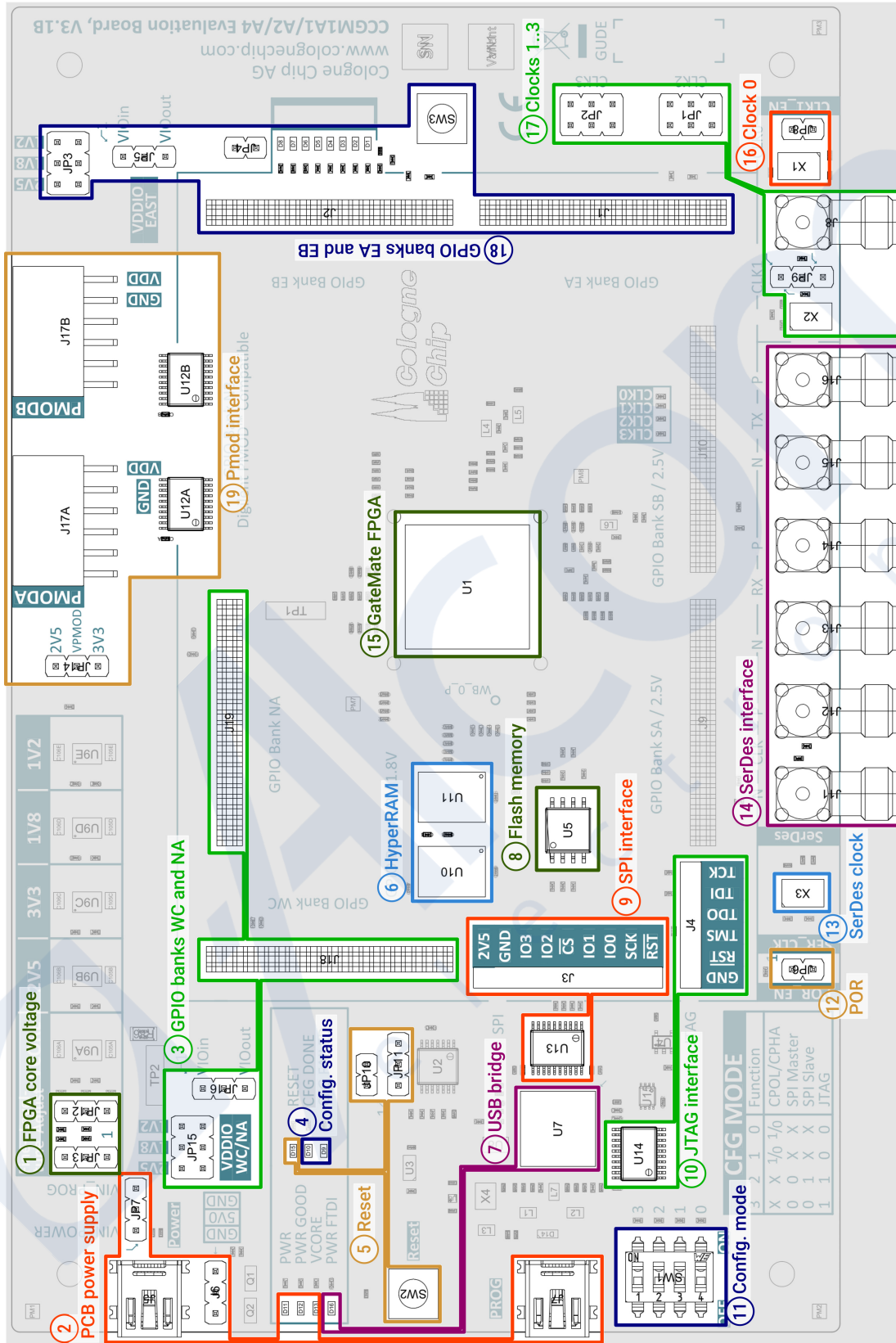


Figure A.1: Component locations on the GateMate™ FPGA evaluation board

## A.2 Default Jumper Settings

**Table A.2:** Default jumper settings

Designator	Color	Function	Default	Shown in Fig.	on Page
JP1 *	black	Clock distribution from user application to FPGA CLOCK2 signal.	–	3.13	31
JP2 *	black	Clock distribution from user application to FPGA CLOCK3 signal.	–	3.13	31
JP3	blue	Select supply voltage for GPIO banks EA and EB and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.4	24
JP4	black	Enable LEDs on GPIO bank EB.	closed	3.4	24
JP5	blue	Select supply voltage for GPIO banks EA and EB (from JP3 or user application supply output VIOout).	1-2: JP3	3.4	24
JP6	black	Enable power-on reset (POR) module.	closed	3.9	29
JP7	red	Power source selection from J5 or J7.	2-3: J7	3.1	21
JP8	black	Oscillator enable for CLOCK0 signal.	closed	3.11	30
JP9 *	black	CLOCK1 source selection from on-board oscillator * or external source via SMA jack J8. *	–	3.13	31
JP10	black	Enable reset signal from user application.	opened	3.9	29
JP11	black	Select reset signal input of user application (reset button only or any board reset).	opened	3.9	29
JP12	red	Core voltage level adjustment (low power, economy or speed mode).	1-2: econ.	3.2	22
JP13	red	Core voltage fine tuning (min, typ, max).	1-2: typ	3.2	22
JP14	red	Select Pmod supply voltage 3.3 V or 2.5 V.	1-2: 3.3 V	3.15	34
JP15	blue	Select supply voltage for GPIO banks NA and WC and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.3	23
JP16	blue	Select supply voltage for GPIO banks NA and WC (from JP15 or user application supply output VIOout).	1-2: JP15	3.3	23

\* Not populated in its shipped configuration.

### A.3 LEDs and Push Buttons

**Table A.3:** LEDs and push buttons

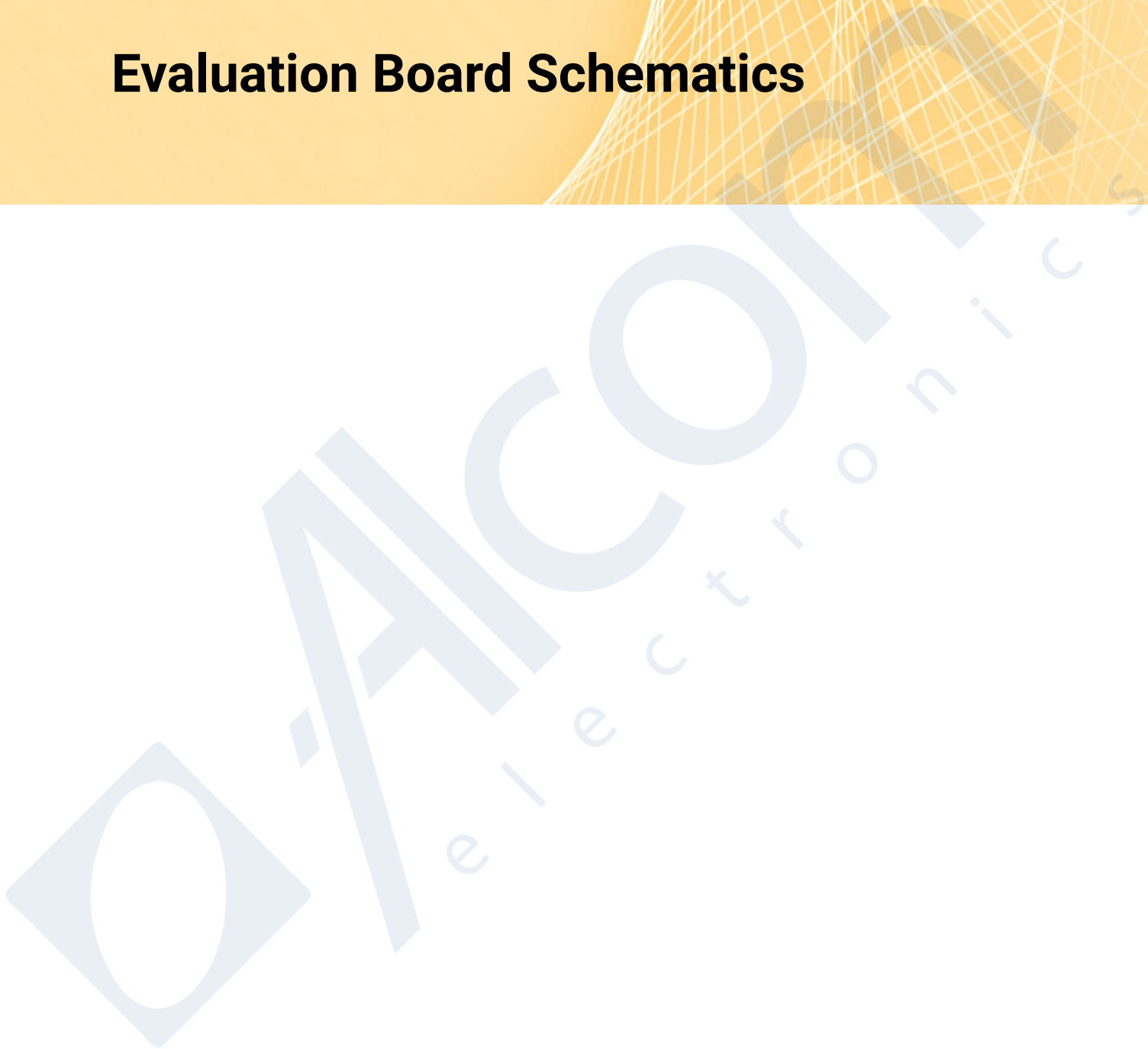
Designator	Color	Function	Shown in Fig.	on Page
D1 .. D8	green	User LEDs assigned to GPIO bank EB	3.4	24
D9	red	Configuration state CFG_FAILED_N	3.10	29
D10	green	Configuration state CFG_DONE	3.10	29
D11	yellow	PCB power supply	3.1	21
D12	yellow	Power good notification from on-board DC-DC converters	3.1	21
D13	yellow	FPGA core power	3.1	21
D15	red	FPGA reset	3.9	29
D16	yellow	Power supply from USB data jack J7 (supply for U7, FT2232HQ-Tray)	2.1, 3.6	15, 26
SW2	red	PCB reset	3.9	29
SW3	black	User button assigned to GPIO bank EB	3.4	24

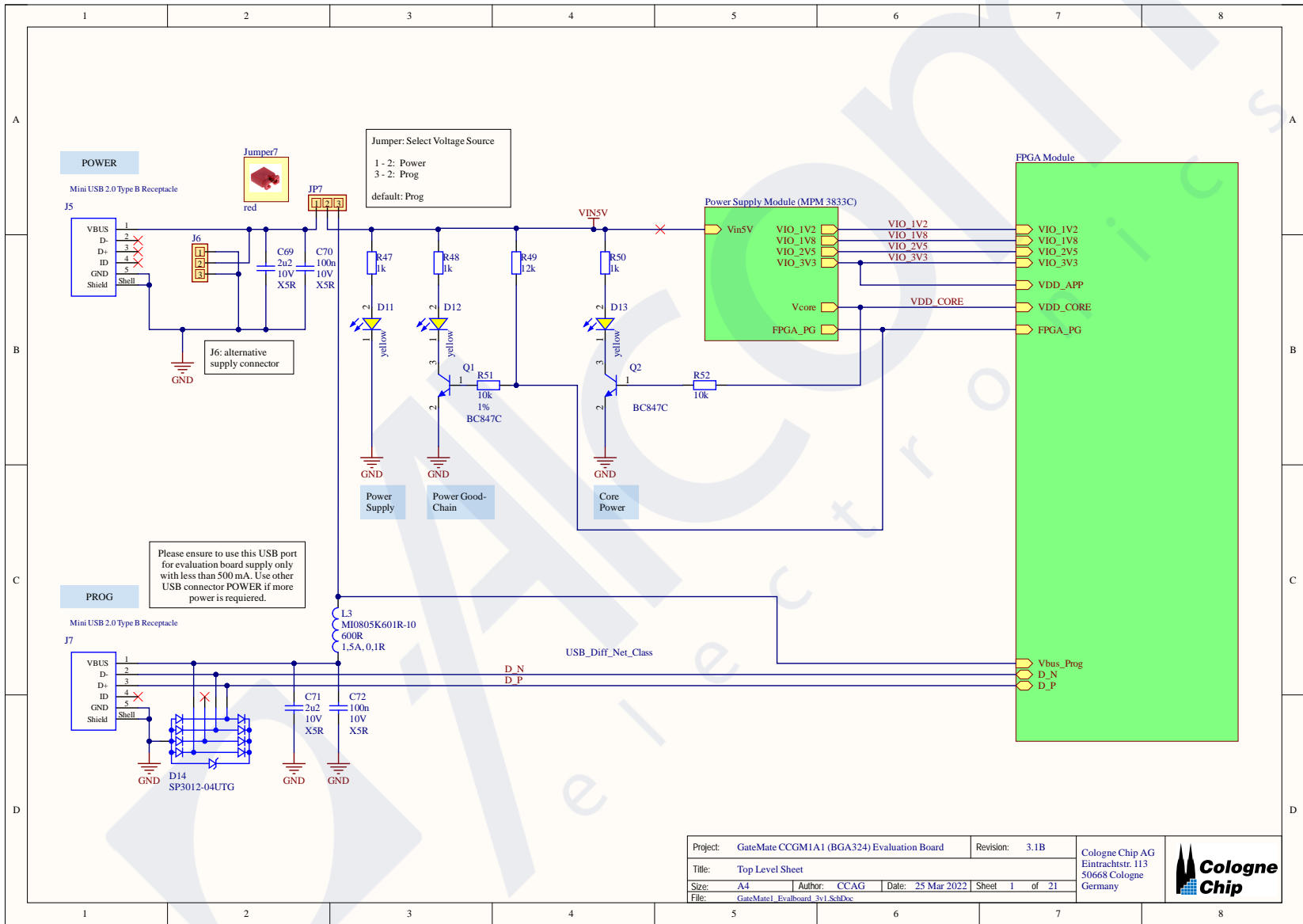





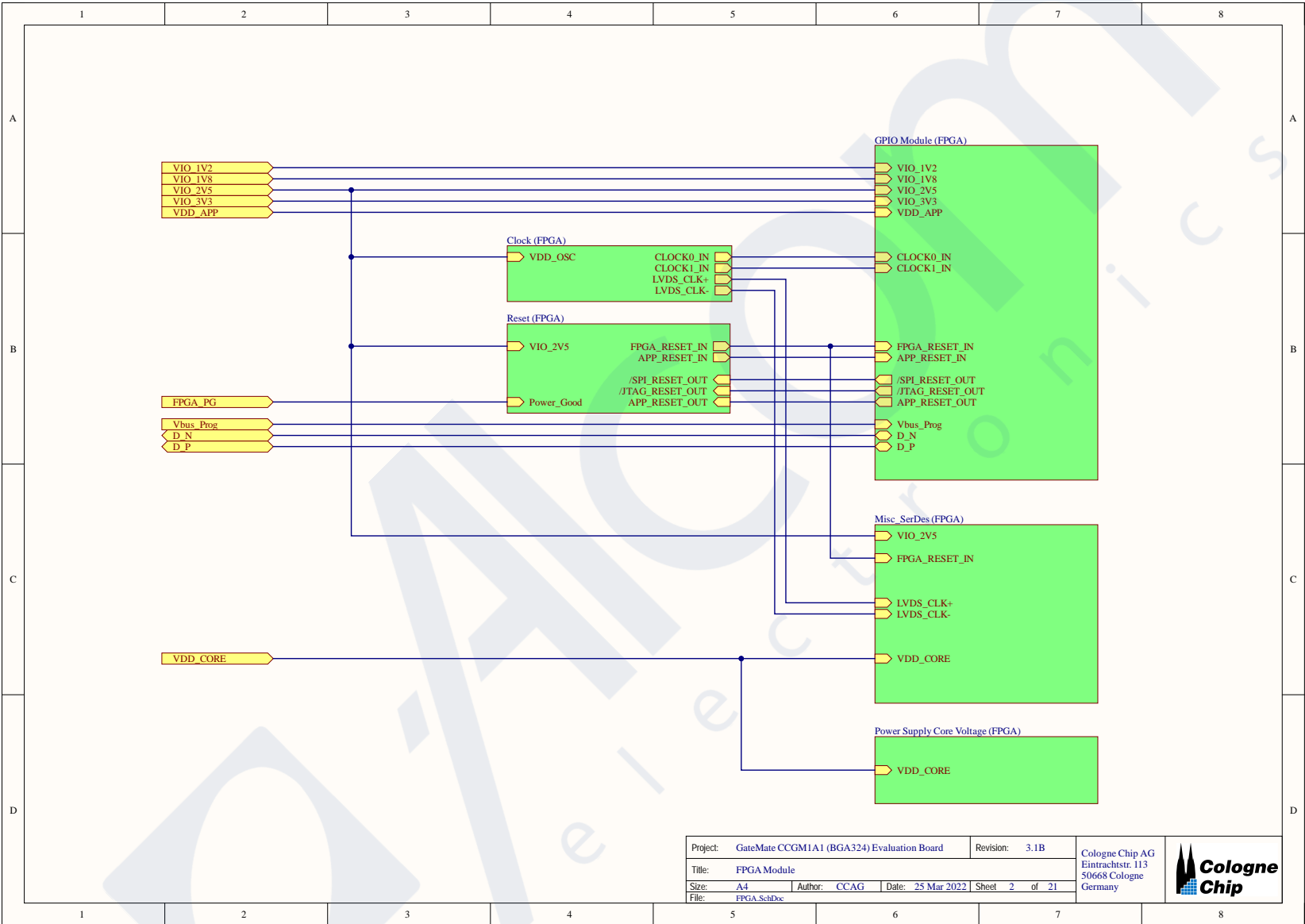
# Appendix B


## Evaluation Board Schematics

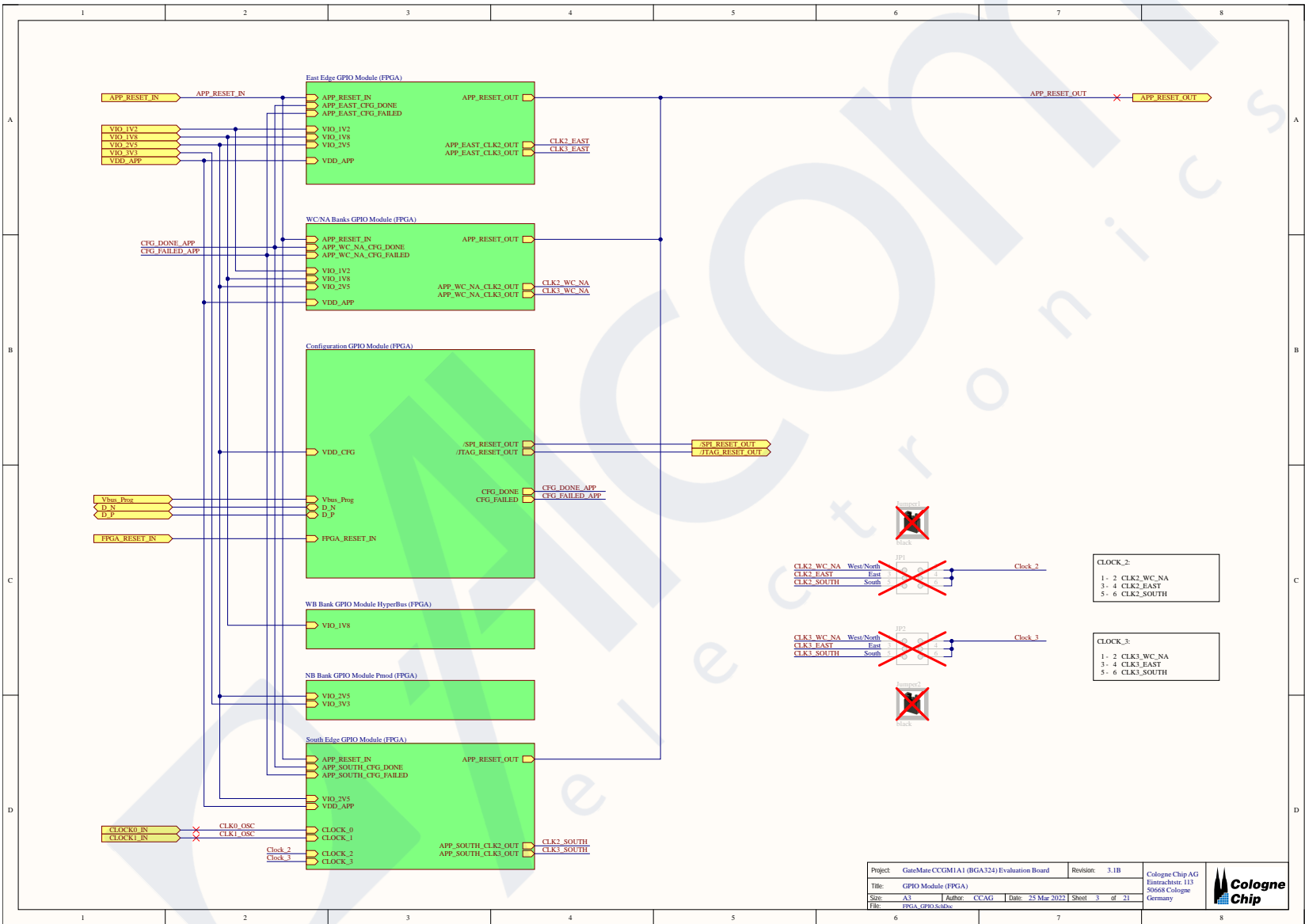




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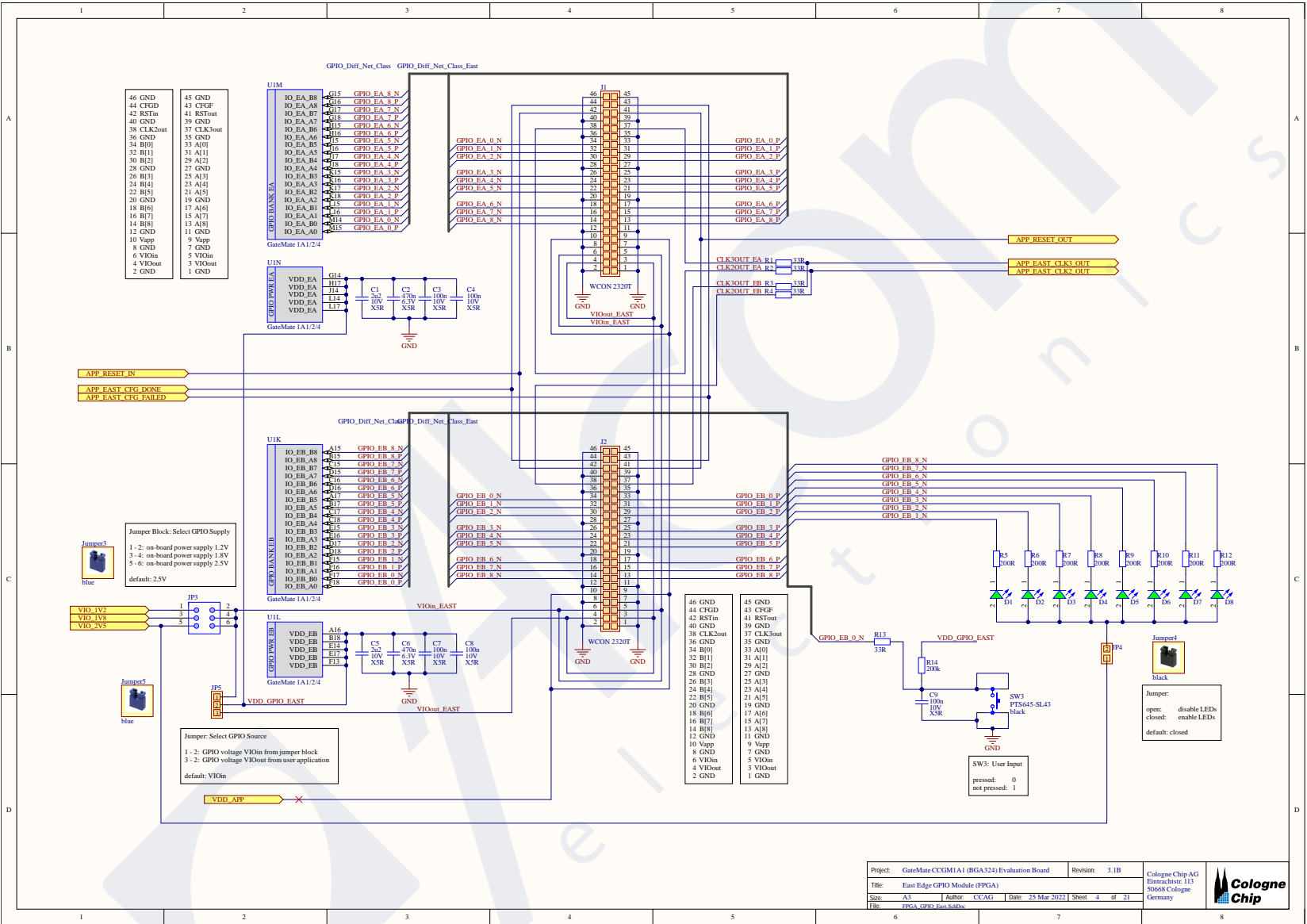


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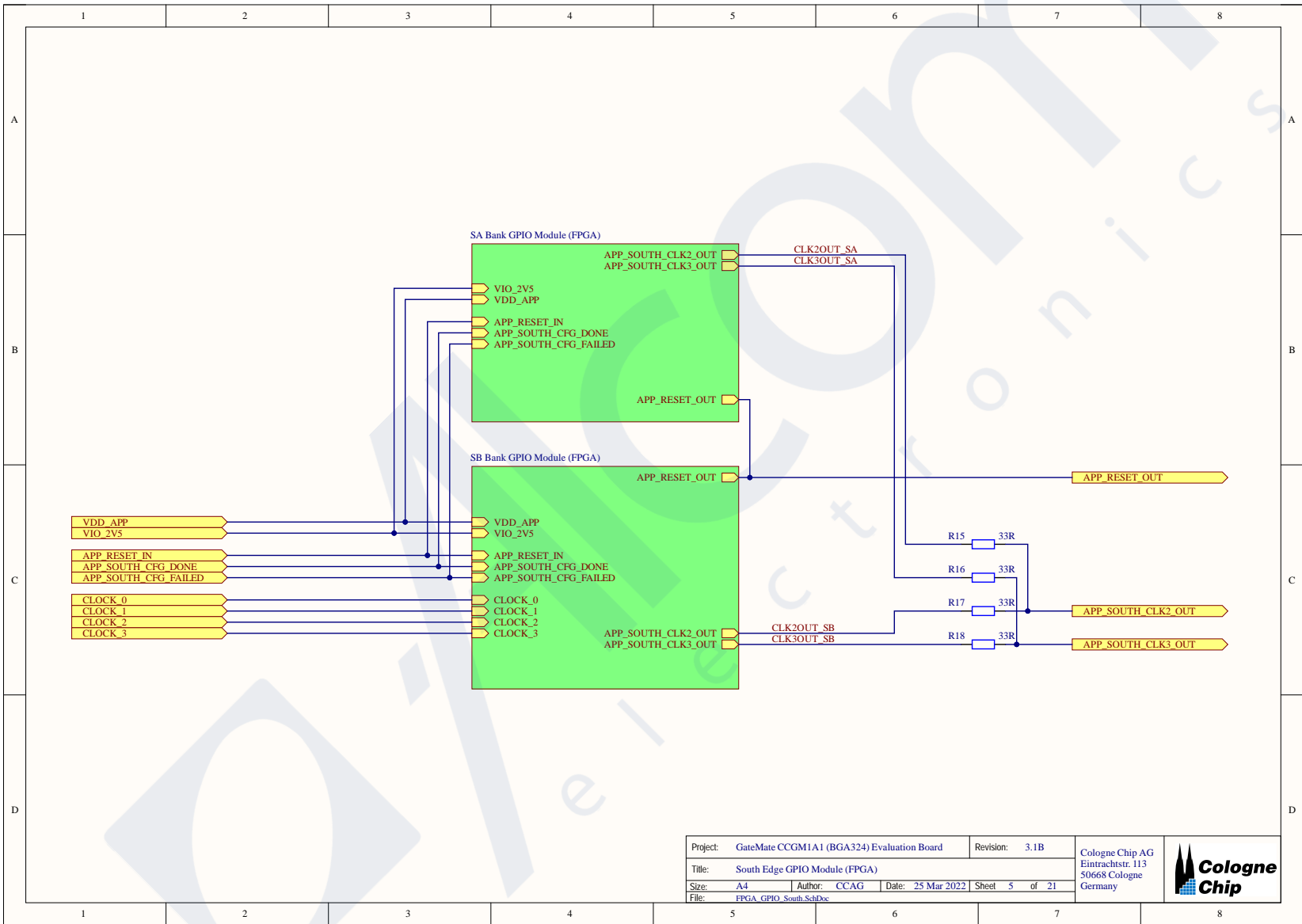


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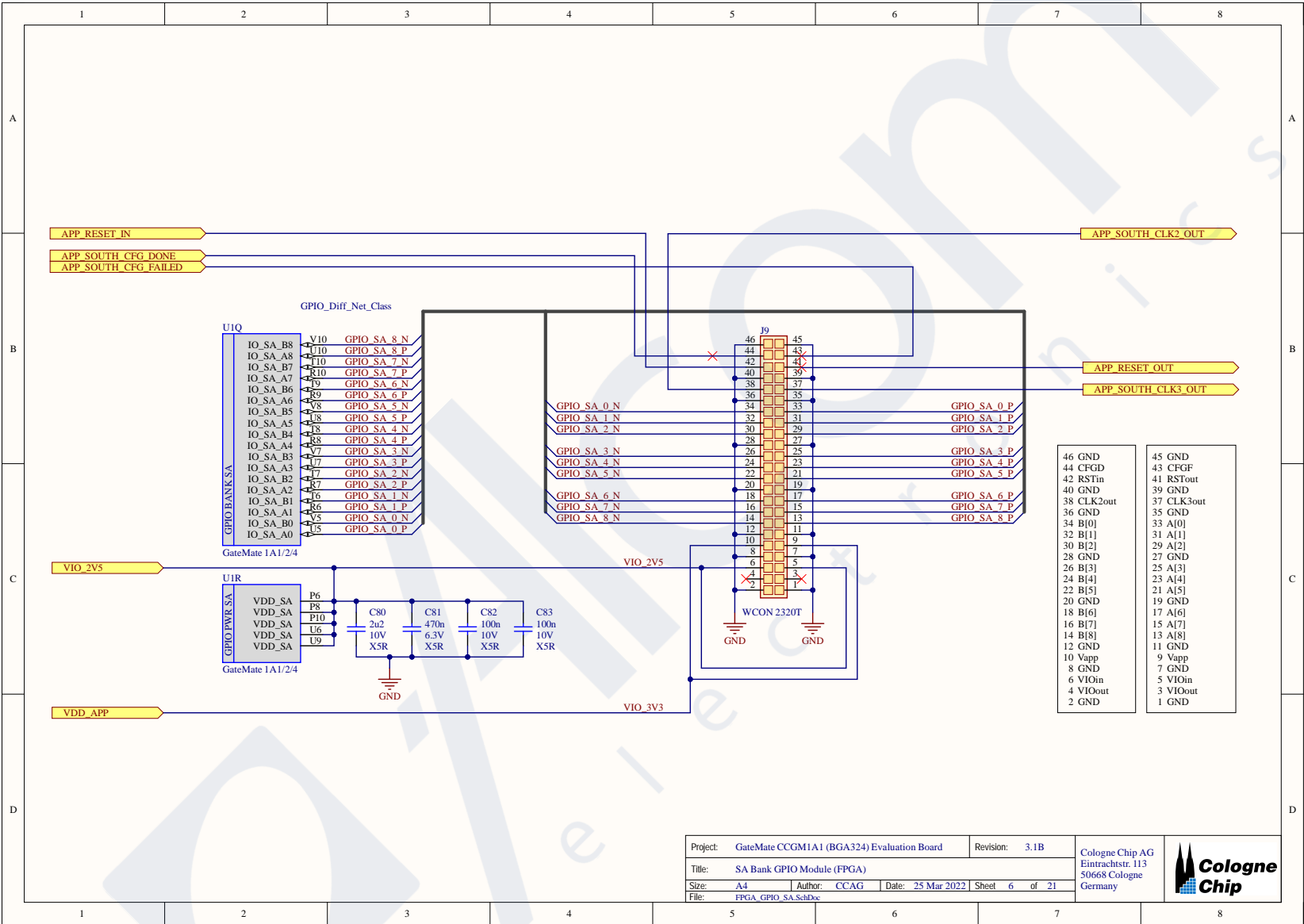




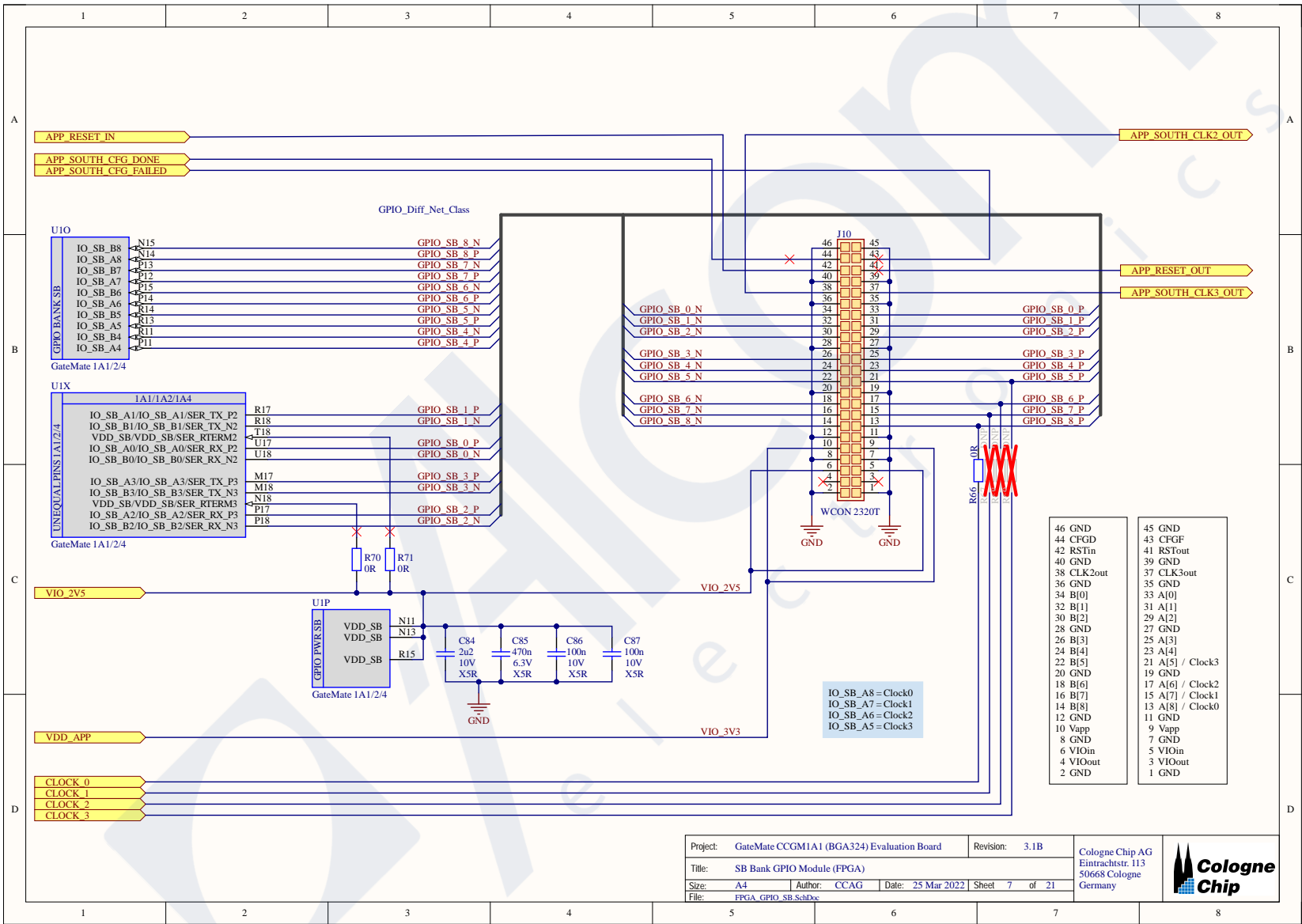
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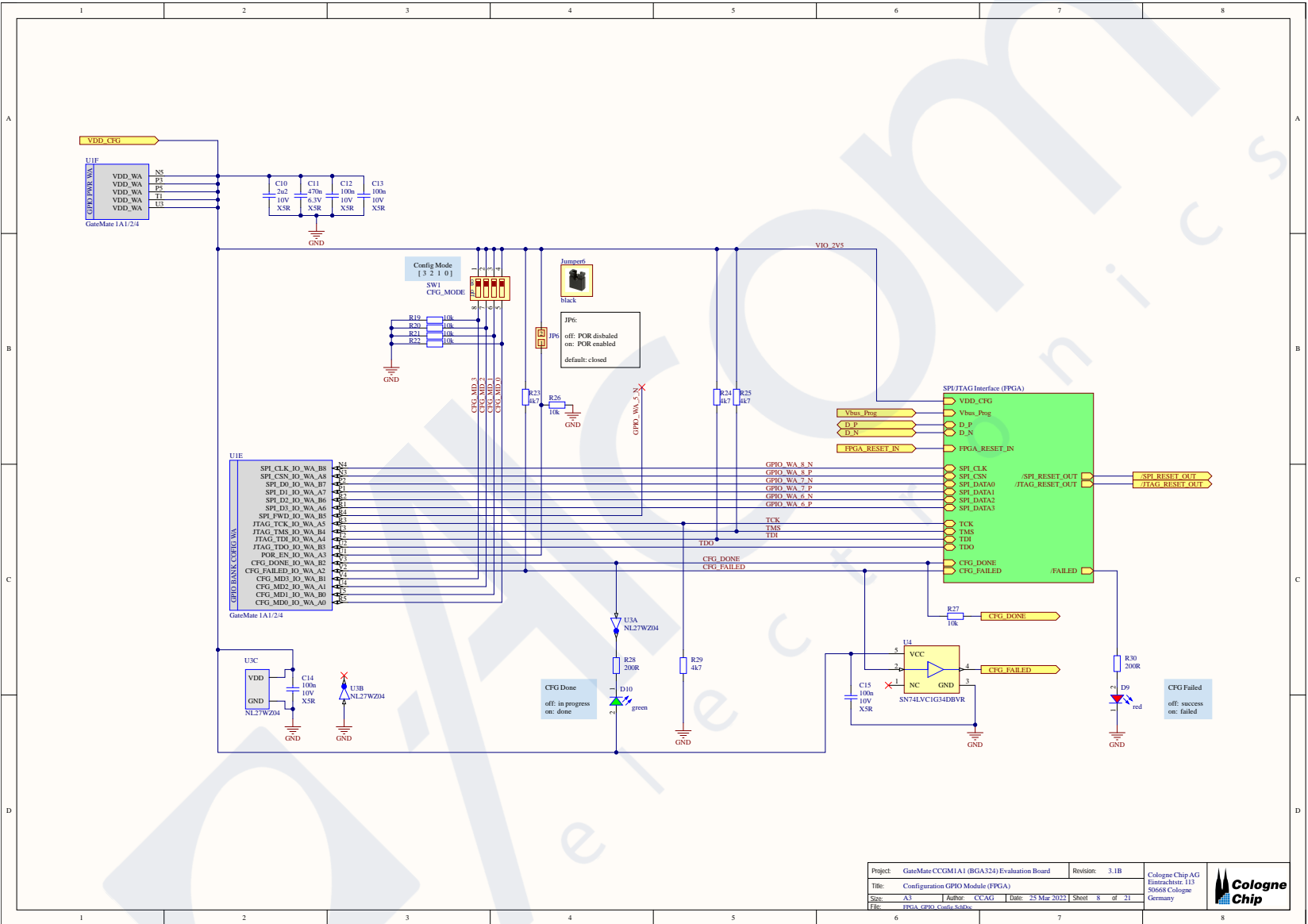




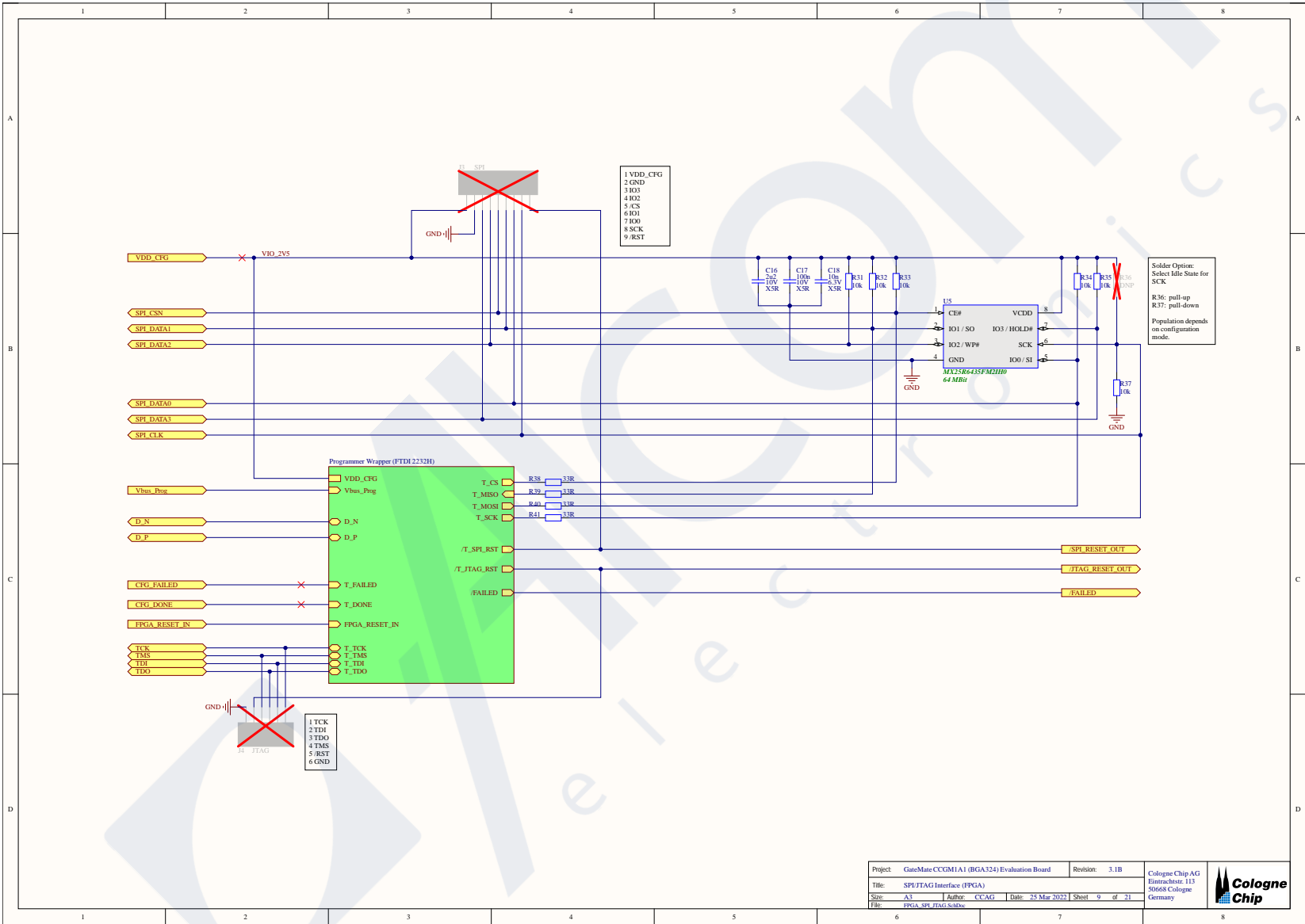


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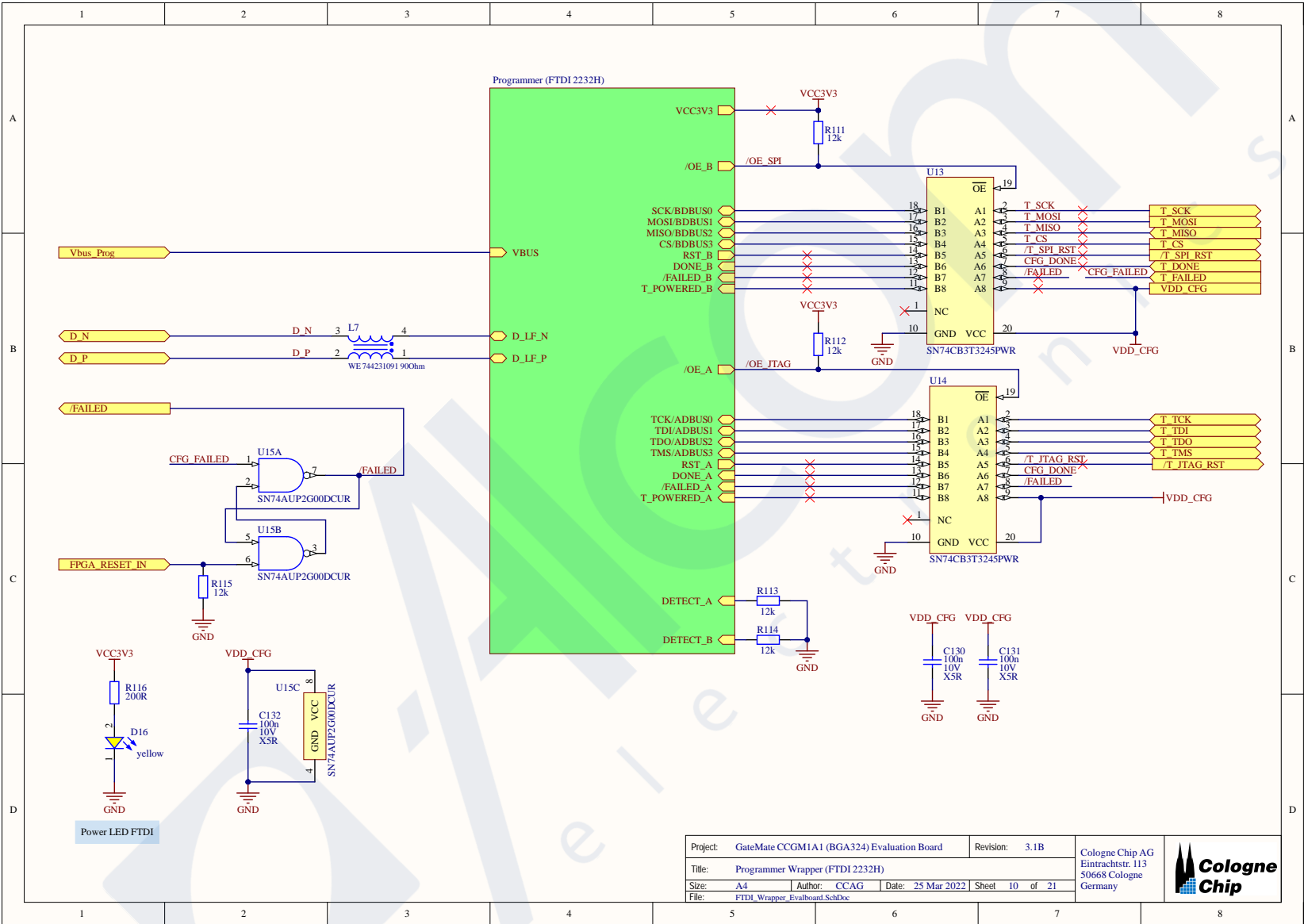


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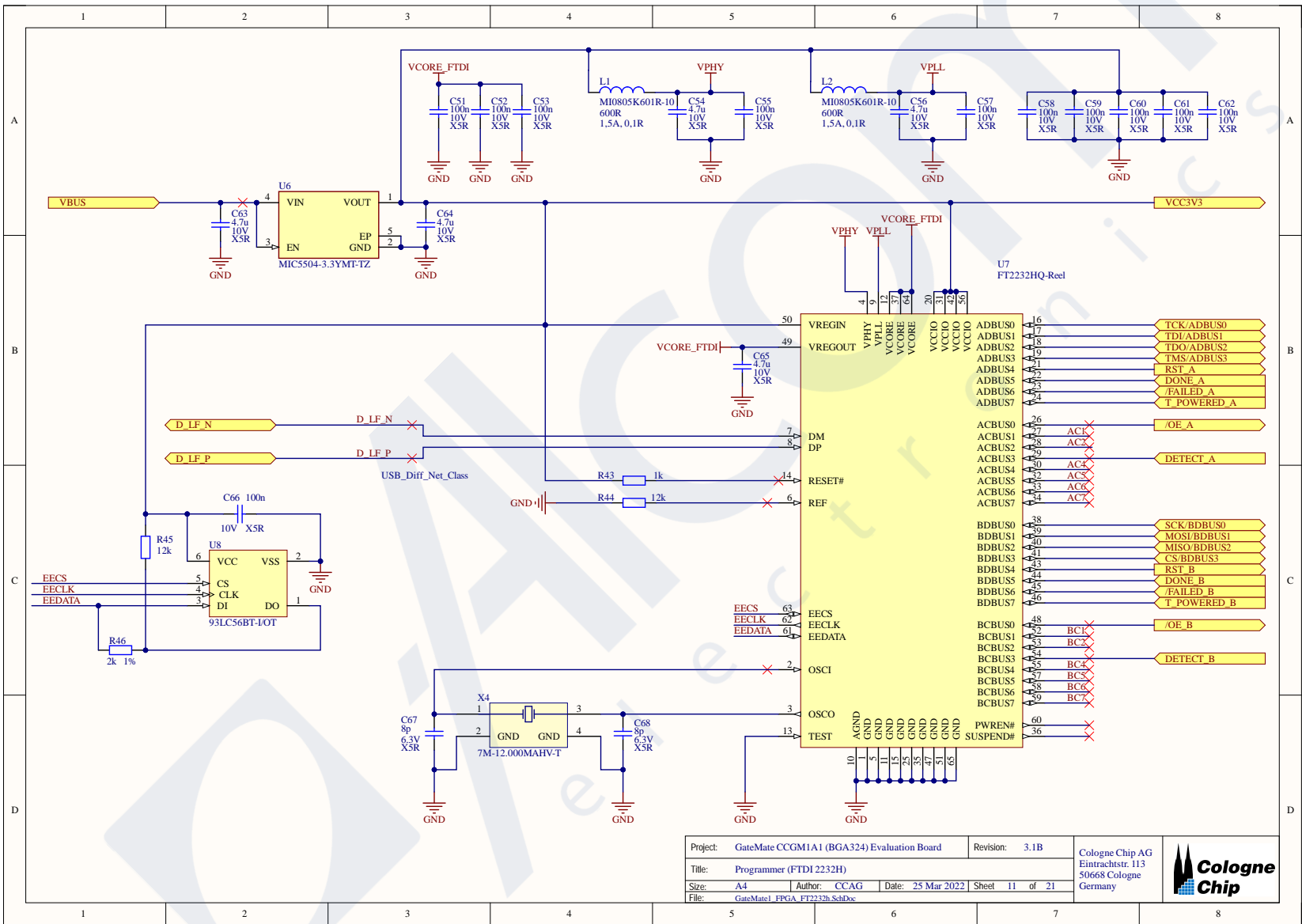


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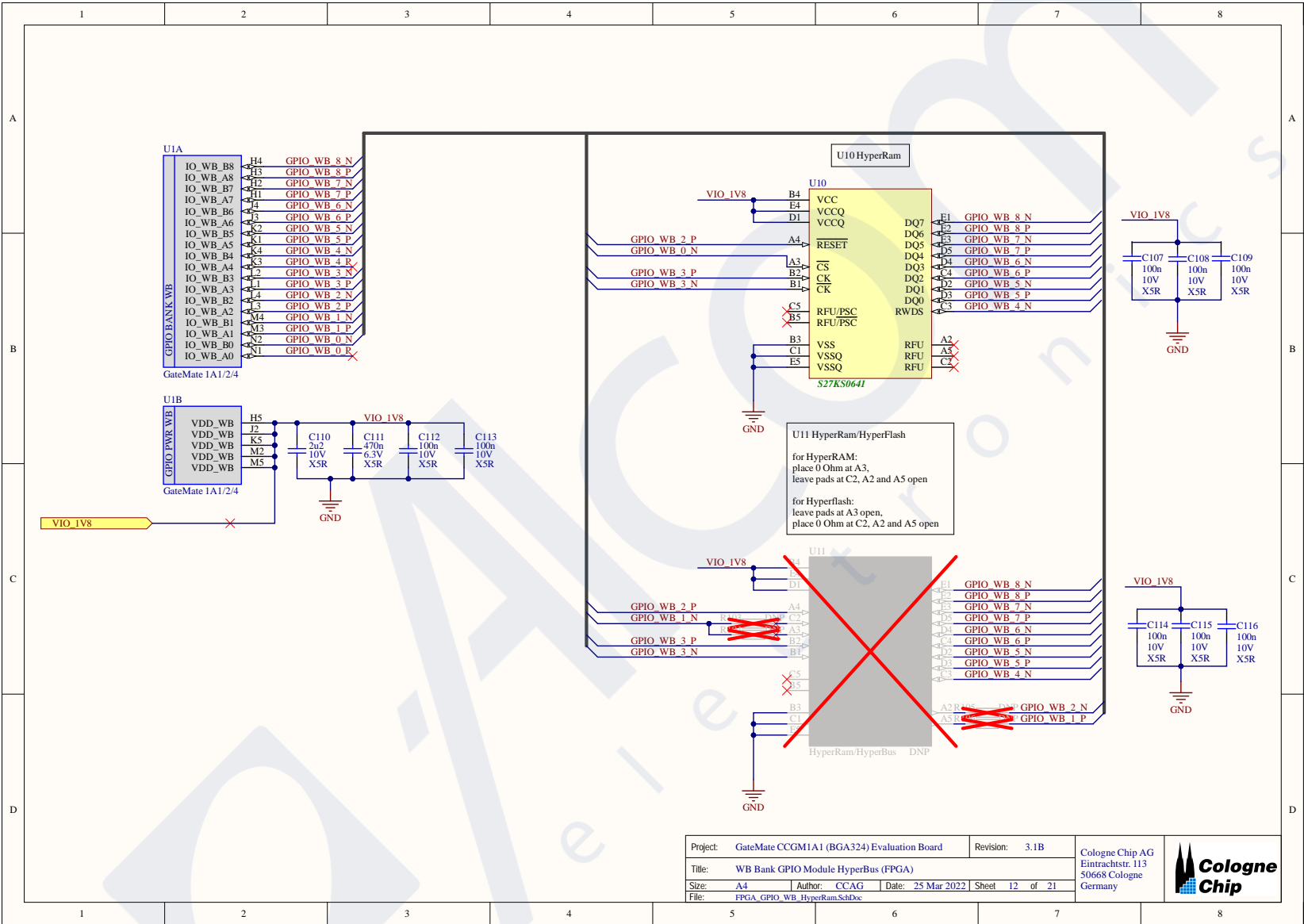
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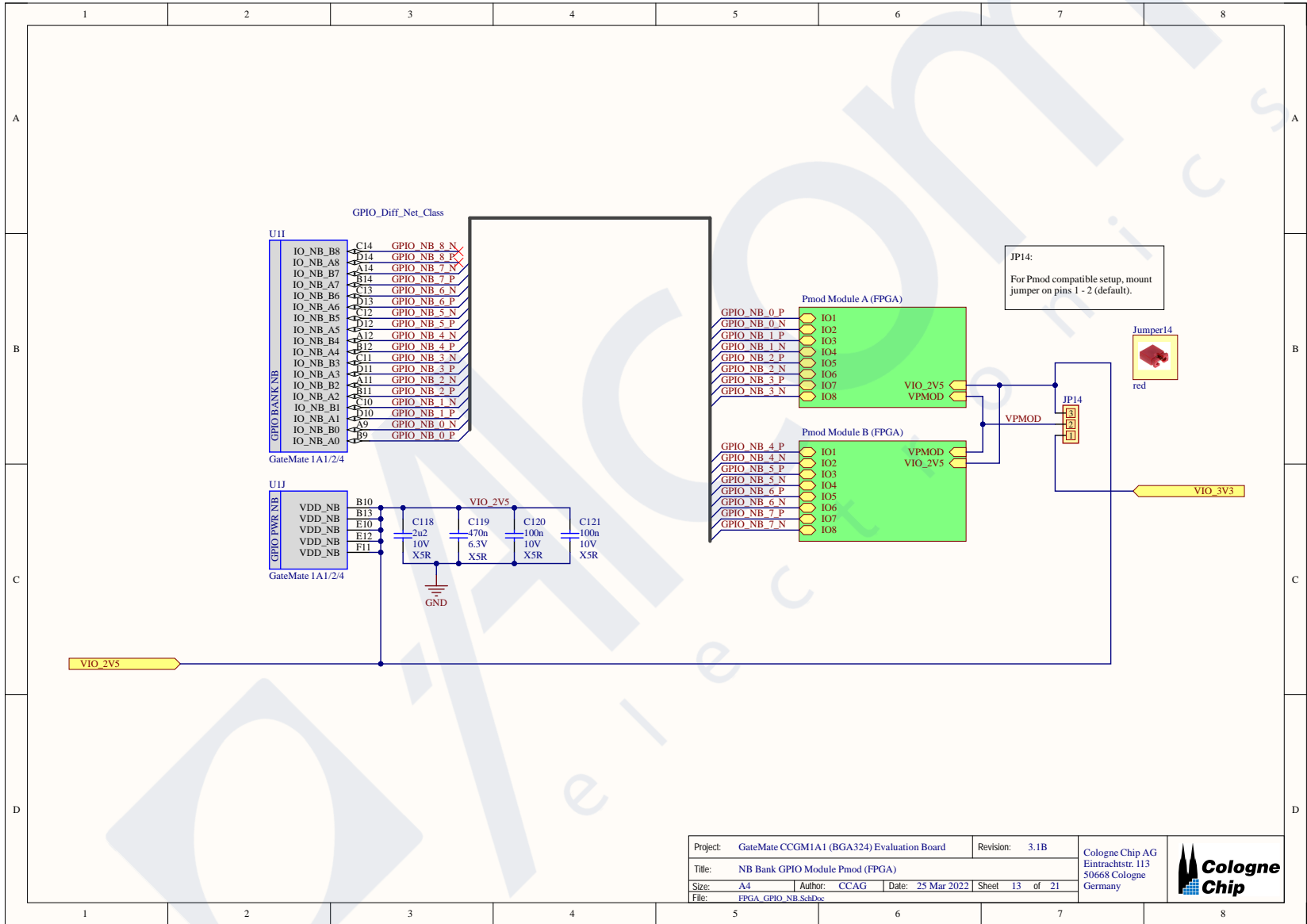


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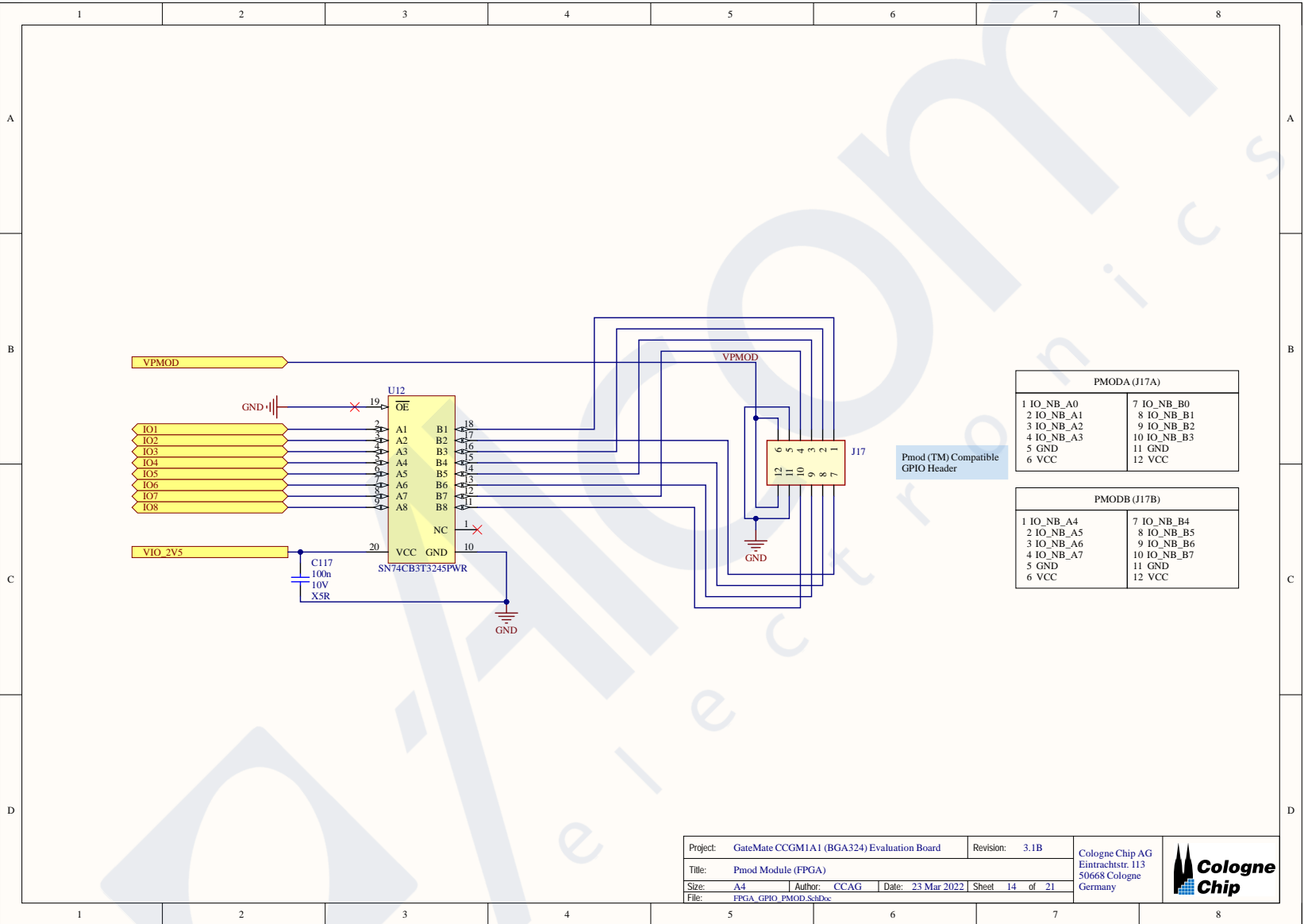
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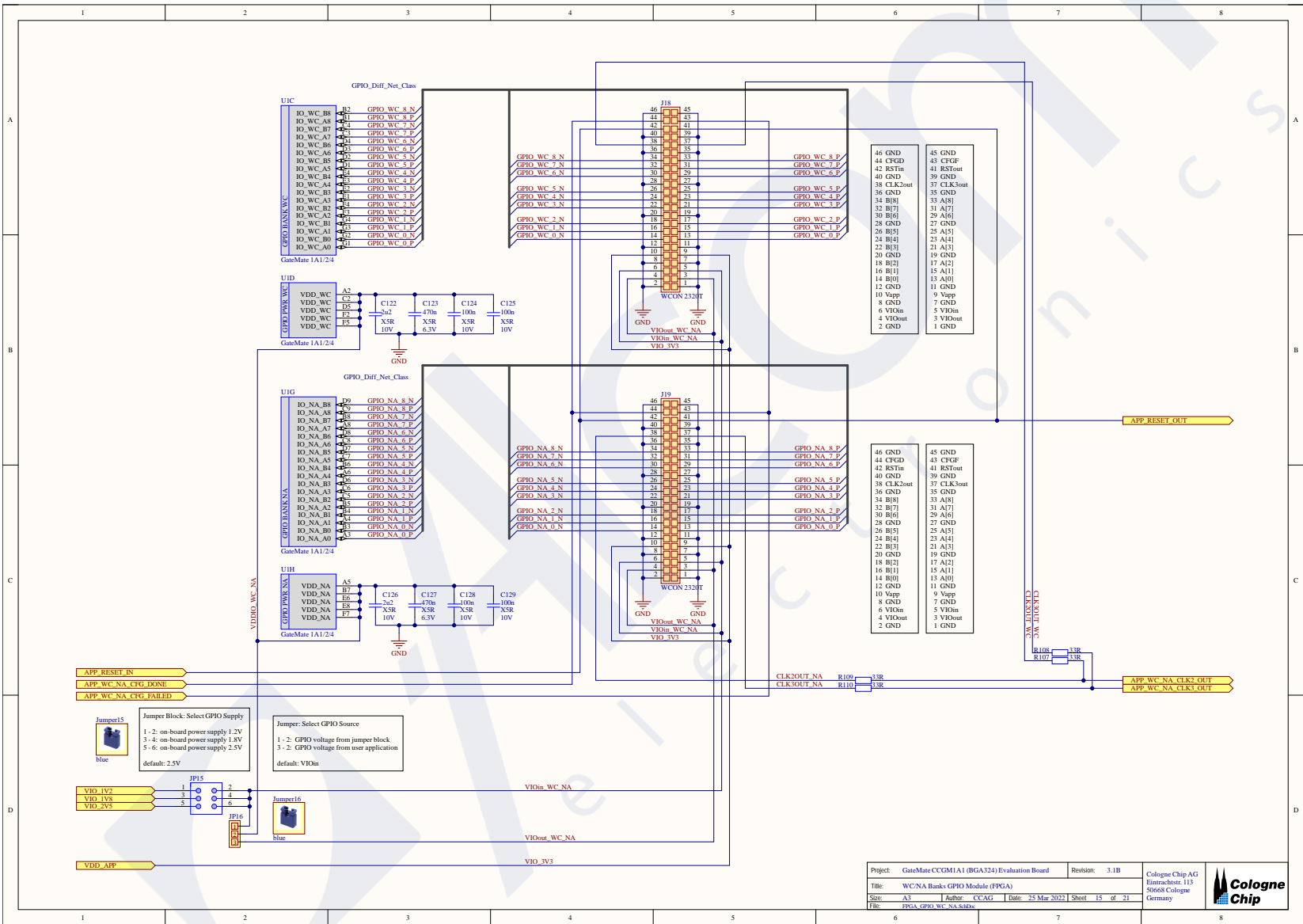


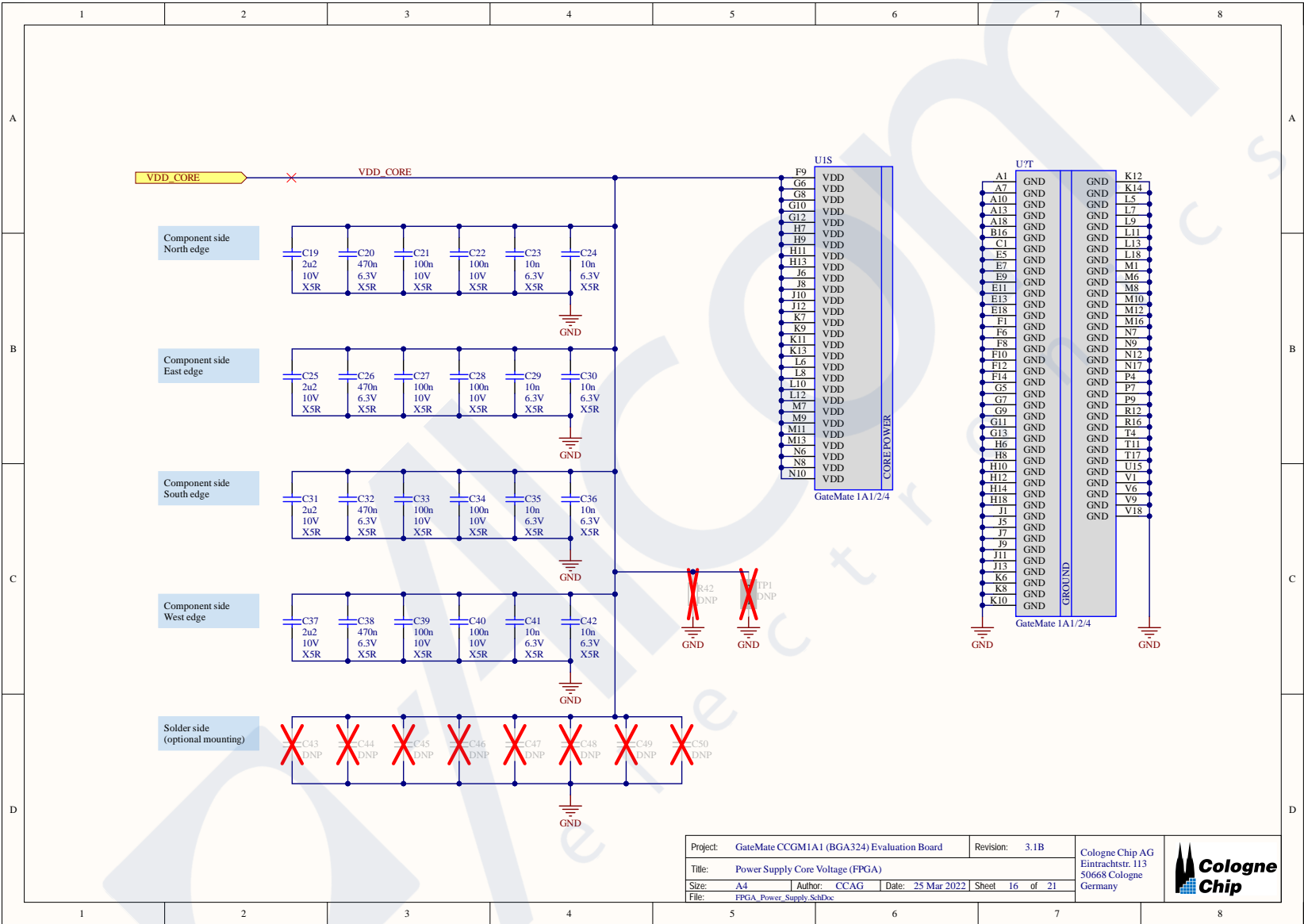


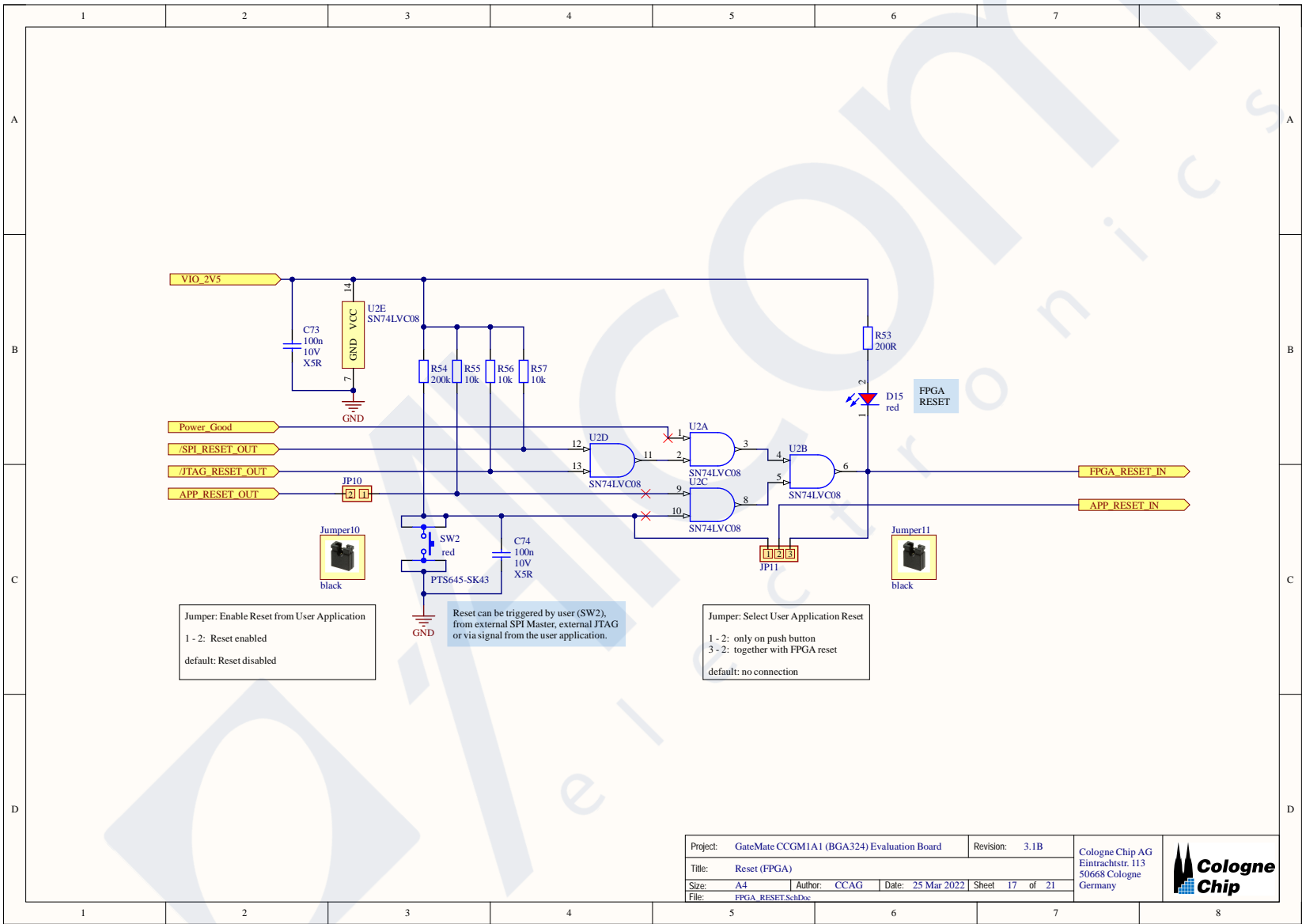
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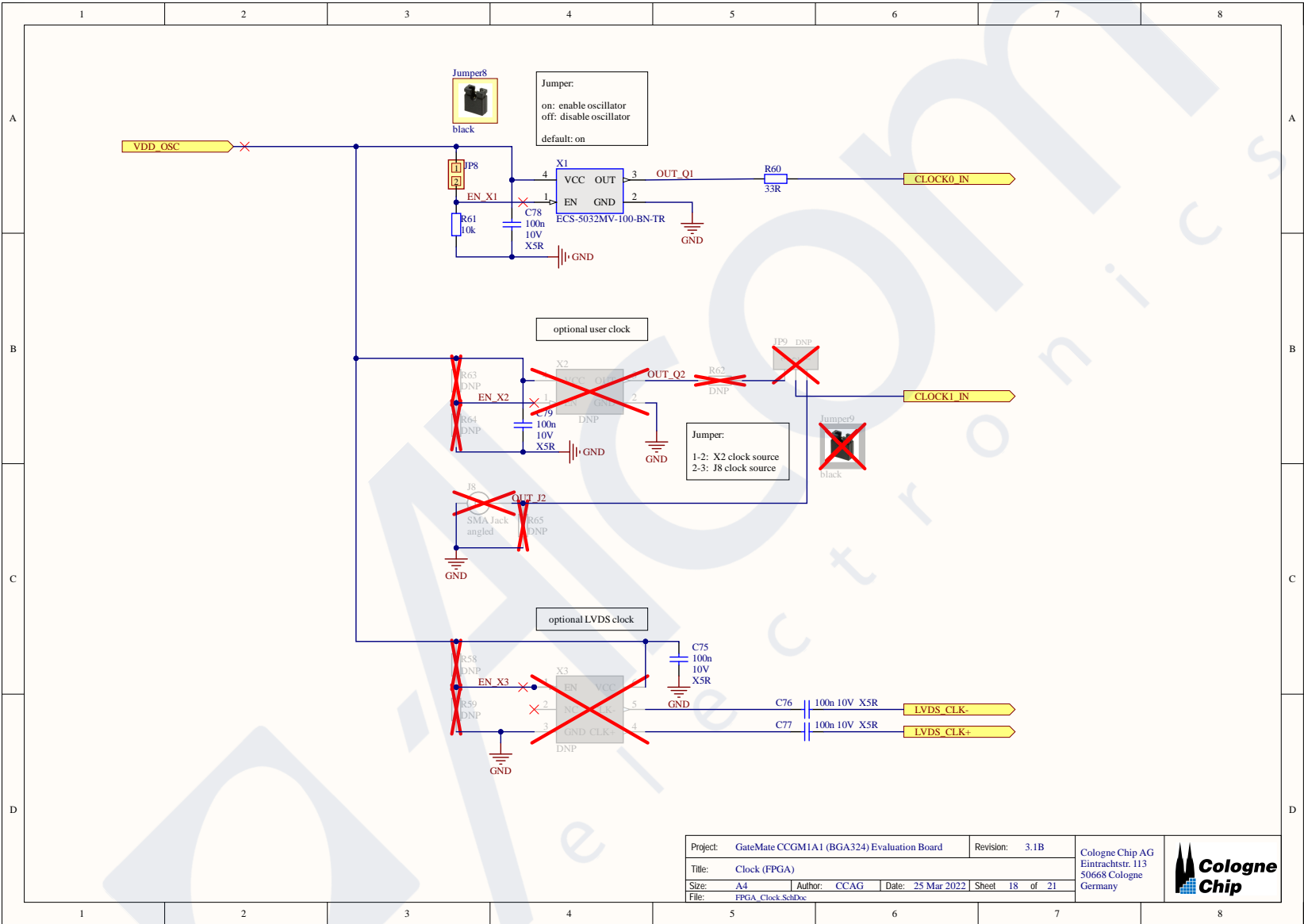


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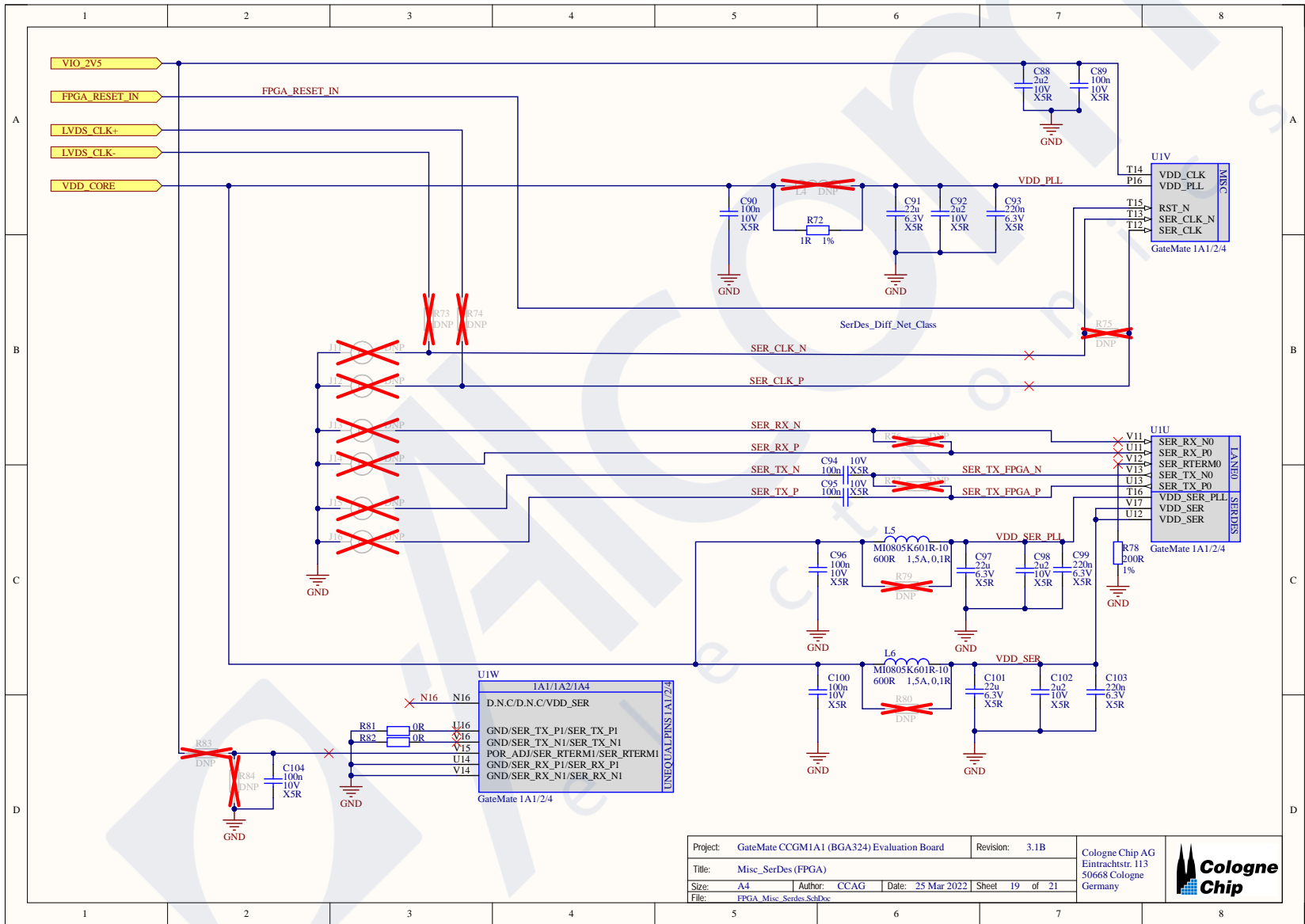


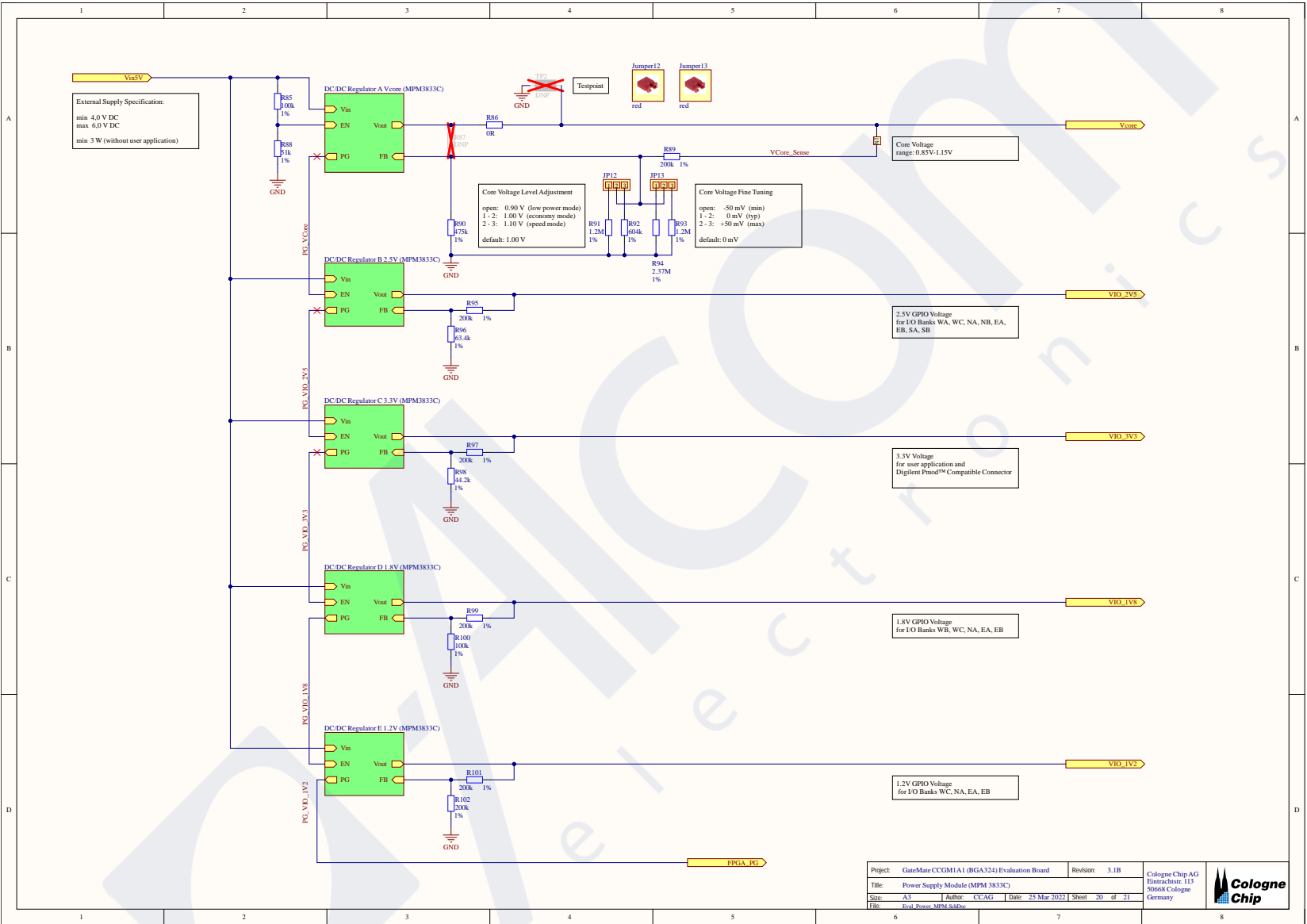


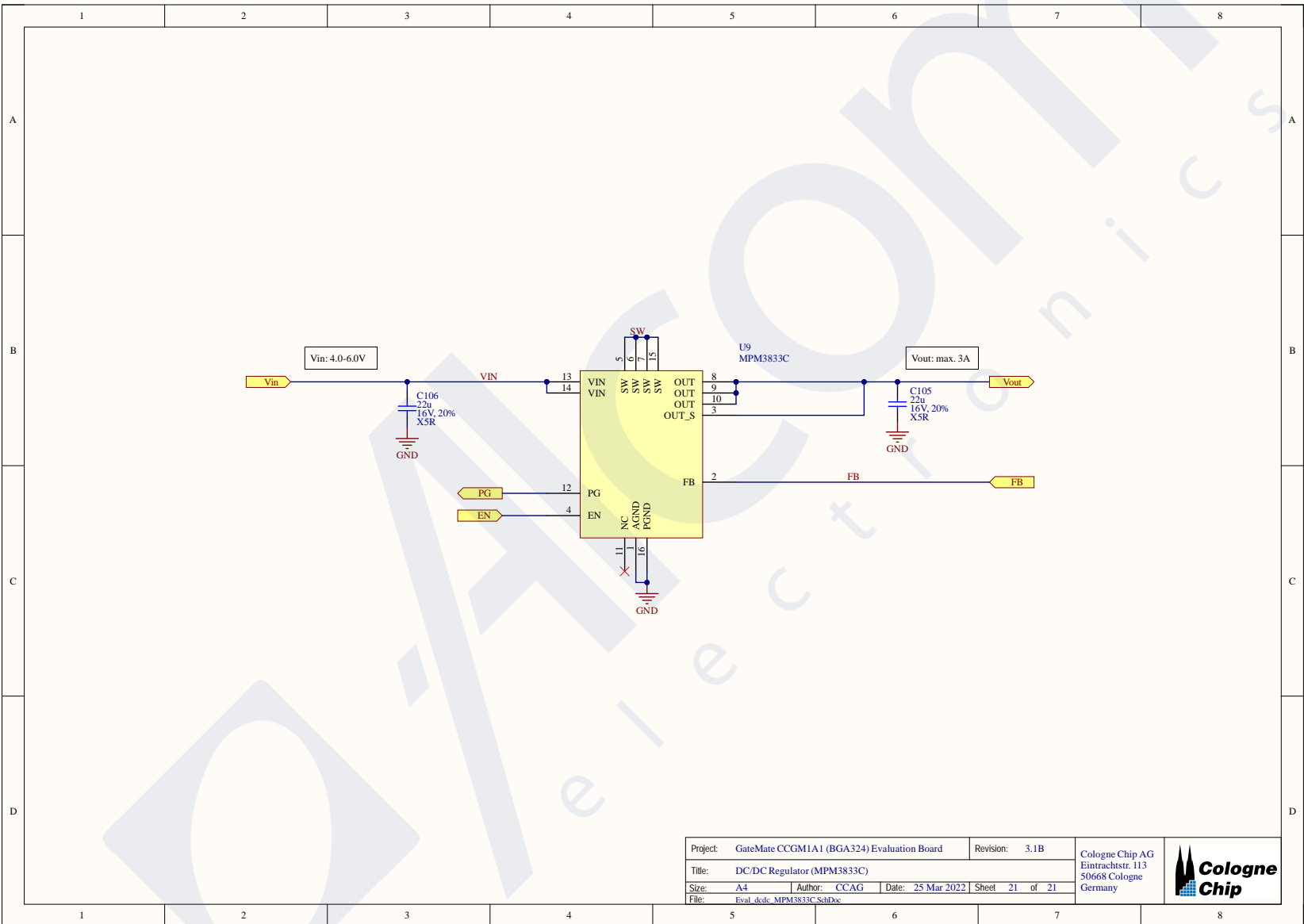













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# Acronyms

FPGA	field-programmable gate array	16
GPIO	general purpose input / output	5–7, 11, 16, 18, 23, 25, 28, 30, 32, 34, 35, 37, 42
JTAG	Joint Test Action Group	5, 11, 16, 26, 28, 42
LVDS	low-voltage differential signaling	5, 7, 30, 36, 37, 42
PCB	printed circuit board	5, 12, 16, 18, 21, 32, 42
Pmod	Peripheral module interface (Digilent)	6, 11, 23, 34, 42
SerDes	Serializer / Deserializer	5, 6, 11, 30, 36, 42
SPI	Serial Peripheral Interface	5, 11, 16, 26, 28, 42
USB	Universal Serial Bus	11, 16, 21

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**GateMate™ FPGA**  
**Evaluation Board Datasheet**  
**Evaluation Board Version 3.1**  
**DS1003**  
**April 2022**

