GOWIN MIPI Solution Capability Overview

White Paper

WP1153-1.1E, 2024-03-29

1 Scope

This document is trying to give a comprehensive overview of GOWIN's MIPI solutions capability to help users choose the best device for their design. It is important for users to work together with other GOWIN User Guides and Application notes in their detail implementation.

2 Introduction to MIPI

The mobile industry processor interface (MIPI®) standard defines industry specifications for the design of mobile devices such as smartphones, tablets, laptops, and hybrid devices. It is developed and maintained by Alliance, which is a global business alliance that develops technical specifications for the mobile ecosystem, particularly smartphones including mobile-influenced industries. GOWIN Semiconductor Corporation is a member of the MIPI Alliance.

For years, MIPI has been pretty much synonymous with mobile phones. But as higher-resolution image sensors increasingly are deployed in AI, IoT, automotive, and medical devices, interest in MIPI is spreading well beyond its core market. While standardized signal protocols and characteristics are becoming essential, an explosion of low-cost, high-performance image sensors for a growing number of applications is propelling the MIPI interface into a variety of new markets,

The MIPI standard defines four unique physical (PHY) layer specifications: MIPI DPHY®, C-PHY®, M-PHY®, and A-PHY®. You can find detailed information and Specs from the MIPI Alliance Website.

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3 GOWIN MIPI solutions overview

GOWIN has developed its MIPI D-PHY solution with its 1st FPGA device. Since then, various configurations and speed IP cores have been offered along almost all our FPGAs. GOWIN is the 1st FPGA vendor to offer MIPI C-PHY IP core in Arora-V family FPGAs. GOWIN is planning to offer M-PHY and A-PHY cores for the same Arora-V family FPGAs shortly. Below is an overview of the GOWIN MIPI PHYs. The detailed performance will be discussed in the following sections.

The Spec number listed in the document is from the best information to date. They are subject to be updated with future version release.

Table 1 Gowin MIPI D/C PHY Offering (May Update in Future)

	DPHY Rx	DPHY Tx	CPHY Rx	CPHY Tx	Notes
	GW1N(X) and GW2A(X) Series				
GPIO based (soft IP)	all: up to 1.2Gbps	all: up to 1.2Gbps	N/A	up to 1.0Gsps*	Max at C7 speed grade or above

Hard IP embedded	GW1N(X)-LV2: up to 2Gbps	N/A	N/A	N/A	1 core w/4-lanes
	GW5A(X) Series (138K)				
GPIO based (soft IP)	up to 1.5Gbps	up to 1.6Gbps	up to 1.1Gsps*	up to 1.1Gsps *	-
Hard IP embedded	up to 2.5Gbps	N/A	N/A	N/A	138K: 2 core w/4-lanes each (Rx) 25K: 1 core w/4-lane (Rx/Tx)
	GW5A(X) Series (60K/25K/15K)				
GPIO based (soft IP)	up to 2.0Gbps	up to 2.0Gbps	up to 1.2Gsps*	up to 1.2Gsps *	-
Hard IP embedded	up to 2.5Gbps	up to 3Gbps	up to 2.5Gsps	up to 3Gsps	1 core w/4-lane (Rx/Tx) 1 core w/3-Trios (Rx/Tx)

Note!

- "*" indicates the need to wire 6 GPIOs to make one trio at package and PCB to keep wiring length minimal.
- GW5A/T will provide GPIO based M-PHY and A-PHY IPs up to 2.5Gbps.
- The numbers here are subject to be updated with more testing results in house or in field.

4 Hardcore MIPI PHY IPs

GOWIN has developed the 1st hard MIPI D-PHY Rx core in their GW1N-LV2 device in-house. This IP core follows MIPI D-PHY Spec V2.1 with a maximum receiving data rate of 2Gbps.

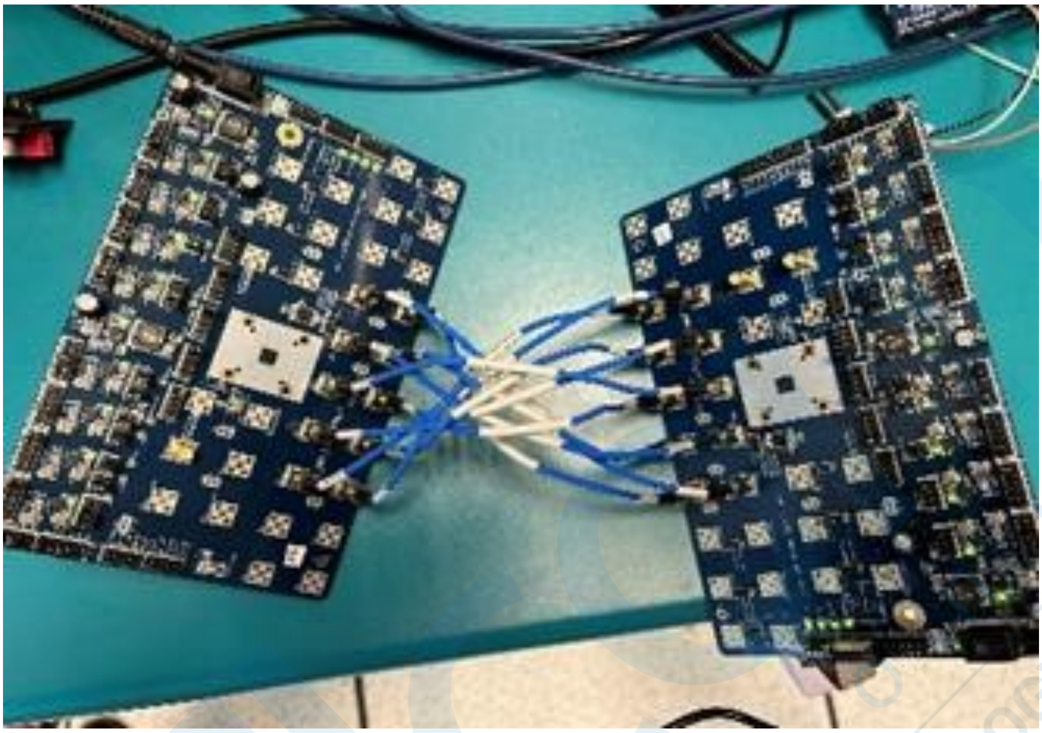
In the next generation Arora V FPGA family, GOWIN has developed both D-PHY V1.2 at 2.5Gbps and C-PHY V1.1 at 2.5Gsps (5.7Gbps) for various devices. The detail feature is shown in the table below:

Table 2 Key Features of Arora V Devices

Key Features	138K	75K	60K	45K	25K	15K
MIPI-DPHY RX/TX with de-skew function	Rx Only	Rx Only	Y	Y	Y	Y
Receiver Equalization with SoT HS-Sync, word and lane alignment	Y	Y	Y	Y	Y	Y
Configurable PHY as general source-sync high speed interface beyond MIPI	Y	Y	Y	Y	Y	Y
TX/RX PAD sharing for DPHY, 4 data lanes, lane-based config mode	Rx Only	Rx Only	Y	Y	Y	Y

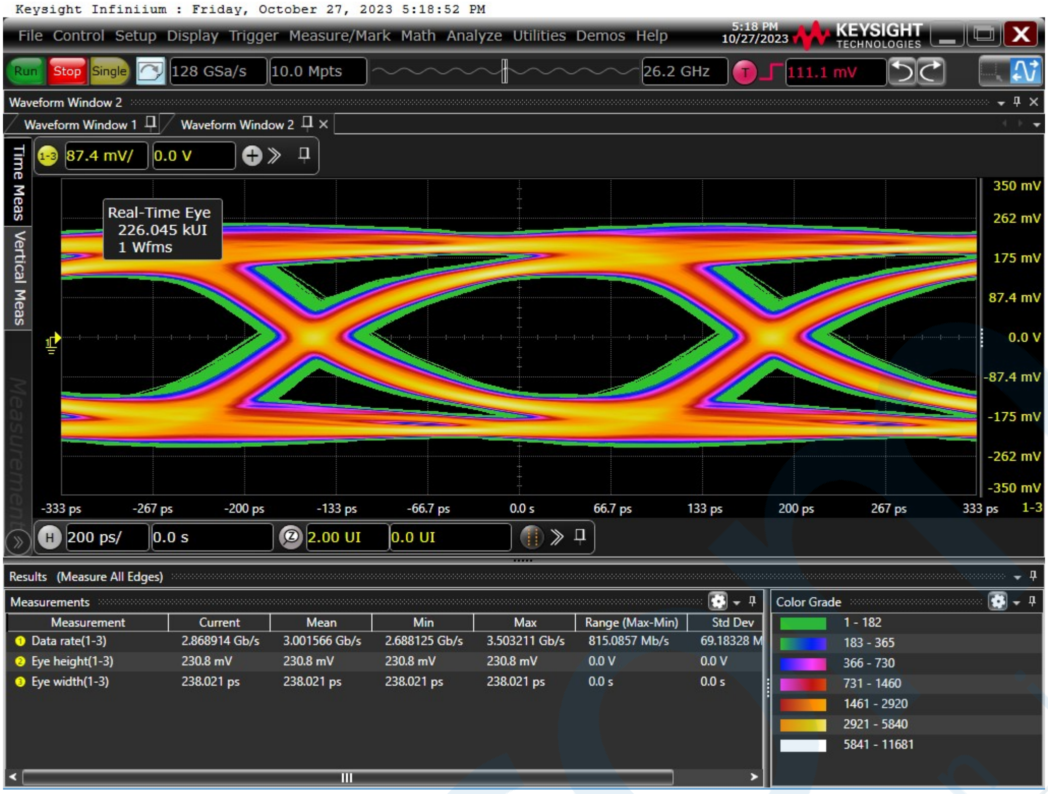
MIPI-CPHY RX/TX Pad Sharing up to 3Gsps, 3 trios	N	N	Y	Y	N	Y

Below is the loopback test setup for the 25K device in the MG121N package:

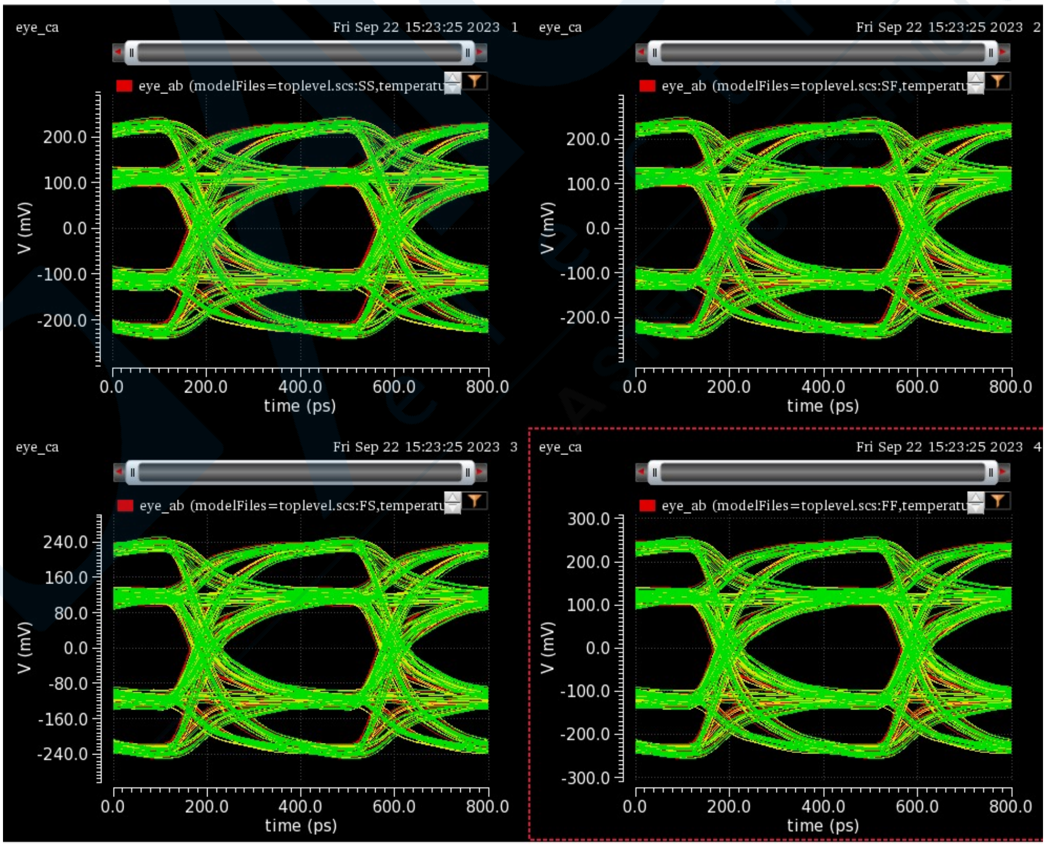


4 Hardcore MIPI PHY IPs

Below is the Eye Diagram from 25K at 3Gbps testing results:



For C-PHY, below is the simulation results for the 60K C-PHY core, and test results will be published with the document update expected in Q2, 24.



5 GPIO based soft MIPI PHY IPs

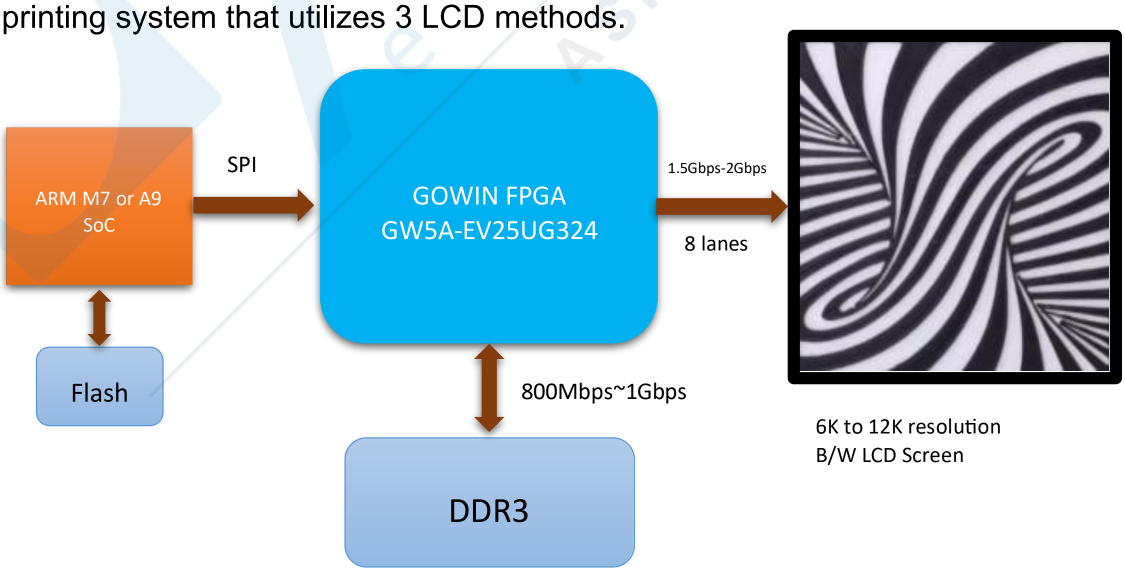
One more interesting piece of information is longer distance applications. MIPI standard is optimized for smartphones and other portable devices where small spaces with short distances are expected. With GOWIN's Hard IP, the equalization feature can give the user a boost when a longer distance is needed. The following user cases can be served as reference:

- For GW1N-LV2, 5-meter-long SATA/HDMI/DP type wire, data rate at 500Mbps.
- For GW5A family, 2-meter-long CAT6 wire, data rate at 1.25Gbps

There are applications with cameras and displays at separate locations. With this capability, a single-chip solution becomes possible.

5 GPIO based soft MIPI PHY IPs

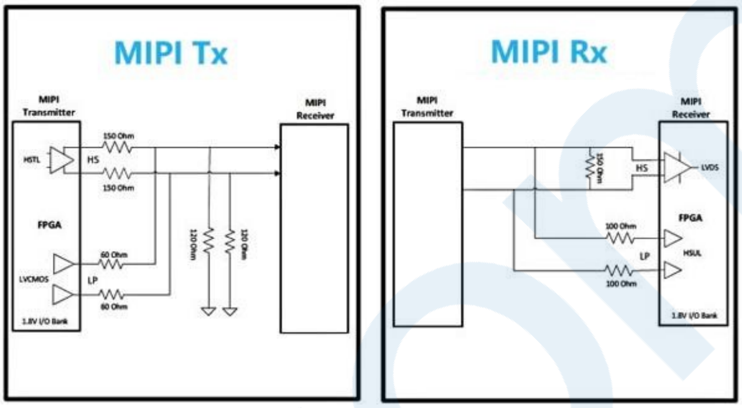
Due to FPGA's programmable IO, many interfaces can be emulated by them with the help of external passive resistor networks. The great advantage of using GPIO-based MIPI PHY solutions is the flexibility. As mentioned at the beginning of this white paper, the MIPI Standard has gone beyond the traditional smartphone space. This flexibility compound with the FPGA 's programmability suits well for the diversity in the new application fields. Here are a few examples: The Mult displays inside an EV car could require 6~8 MIPI Tx ports; The VR or drone system could require 12 cameras as inputs and aggregate the data to one output. Few of today's SOCs can handle such requirements. Below is a user case in a 3D printing system that utilizes 3 LCD methods.



Though many FPGAs today can support MIPI D-PHY, GOWIN's FPGAs are 1st ones that can support MIPI C-PHY, MIPI M-PHY, and MIPI A-PHY by the patented technology.

MIPI D-PHY

The below diagram shows one implementation of a passive resistor network to emulate MIPI signaling. It is very important to take the trace and signal integrity to achieve the best performance.



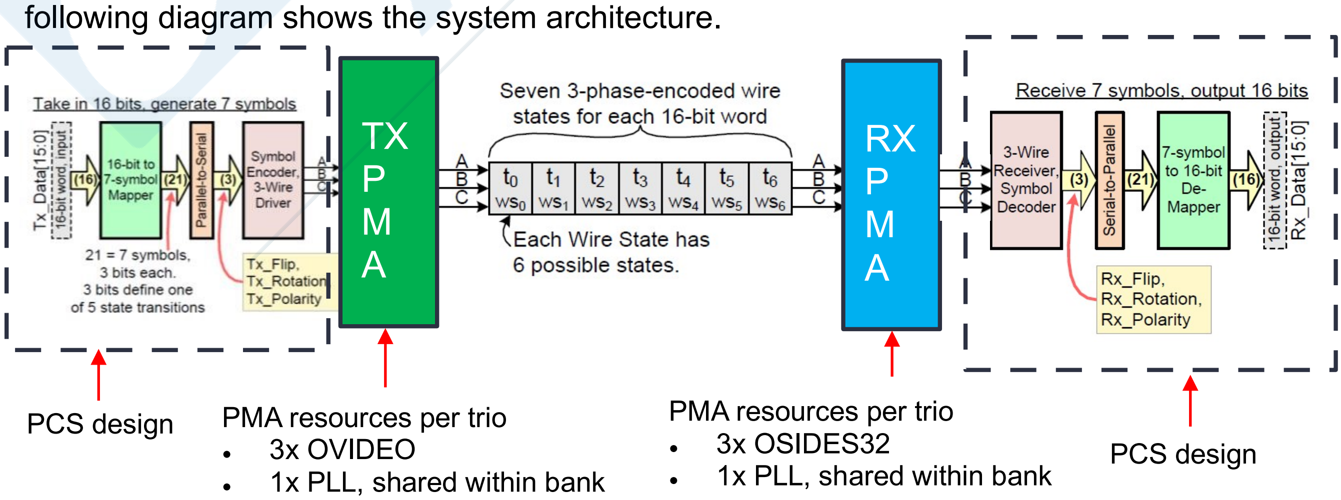
For Gowin devices, the following maximum data rates have been achieved from inhouse testing and customer reports:

- For GW1N family C6 speed grade devices, Max data rate 900Mbps~950Mbps
- For GW1N family C7 speed grade devices, Max data rate 1.1Gbps~1.2Gbps
- For GW2A family C8 Speed grade devices, Max data rate 1.1Gbps~1.2Gbps
- For GW5A family C0 speed grade devices, Max data rate 2.0Gbps (2.5Gbps observed in house loopback testing on raw data)

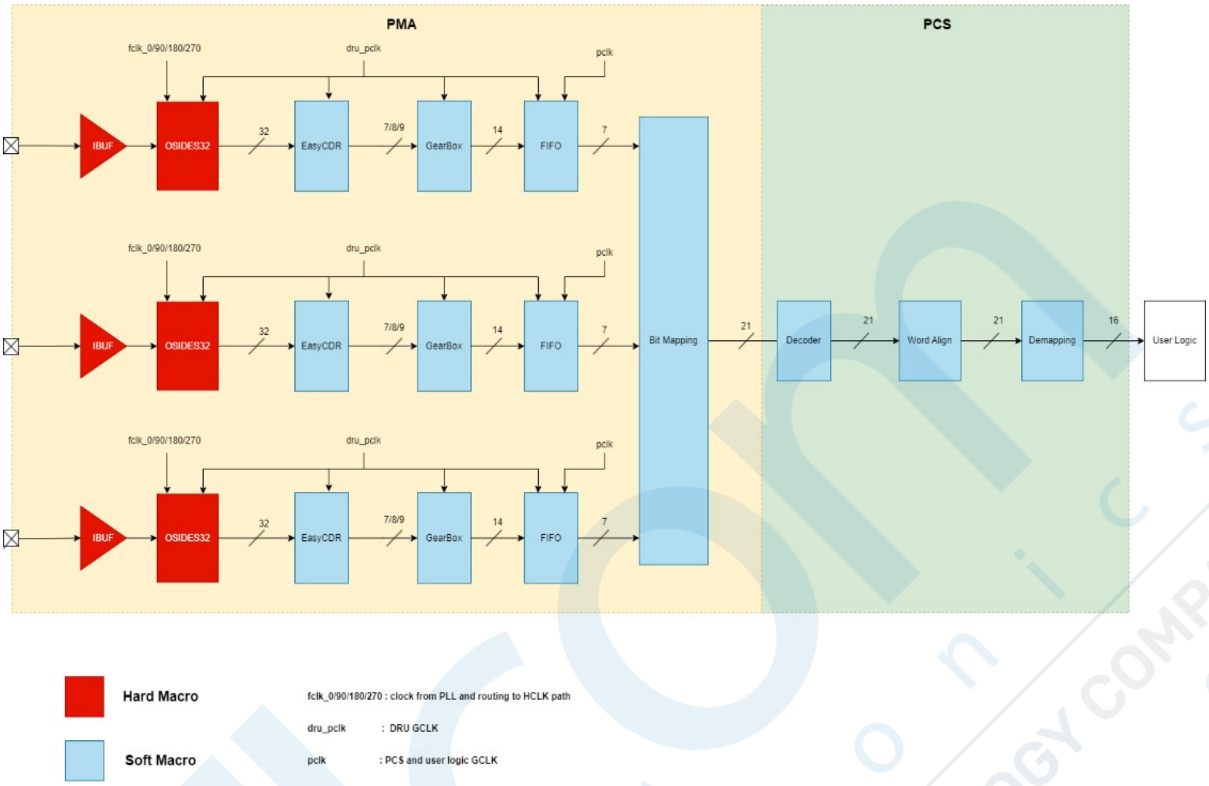
The maximum data rate is more related to internal clock performance than the GPIO. GW5AT-138/75 device has a max data rate of 1.6Gbps due to the local clock in a big die having relative underperformance to other devices.

MIPI C-PHY

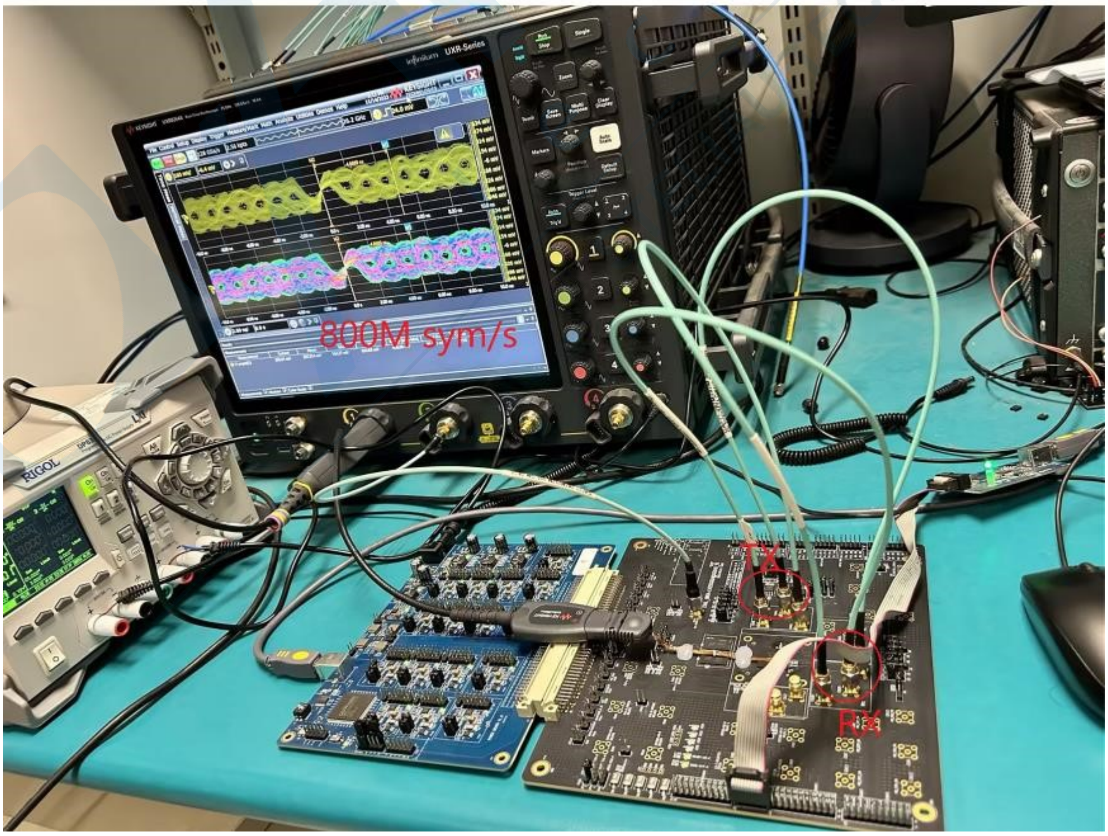
GOWIN is the 1st FPGA vendor to offer a GPIO-based MIPI C-PHY solution through our innovative GPIO system. These IPs are only available for Arora V family devices. The following diagram shows GOWIN's patented GPIO-based MIPI CPHY soft IP solution. The following diagram shows the system architecture.



Below is a more detailed Rx system implementation utilizing GOWIN's EasyCDR® IP.



A loopback test has been set up and measured on a 25K device. Below is the bench setup:



The test results show a loopback of 800Msps speed has been achieved. The following are eye diagrams at 400Msps and 700Msps.


400Msps 700Msps

Due to the limitation on the trace length control in the test PCB, we believe a higher speed can be achieved. There will be more data collected in the near future.

MIPI M-PHY

Compared to a traditional analog SerDes-based M-PHY design, the GPIO-based MPHY is much lower in power, cost, and is more flexible. These IPs are under development and will be available for Arora V family devices. We are targeting the following:

- HS-G1: 1.25, 1.45 Gb/s
- HS-G2: 2.5, 2.9 Gb/s

MIPI A-PHY

Compared to a traditional analog SerDes-based A-PHY design, the GPIO-based APHY is much lower in power, and cost, and more flexible. These IPs are under development and will be available for Arora V family devices. We are targeting the following:

- Gear Data rate G1
- Uplink

6 GOWIN MIPI PHY and Protocol layer IPs and reference designs

GOWIN offers many PHY IPs as well as Protocols layer soft core IPs such as MIPI CSI-2, and MIPI DSI through the GOWIN EDA tool core generator.

IP	Type	Device	RefDesign	Doc
MIPI_DPHY (Tx/Rx)	Hard Core	GW5A(X)	Contact Gowin Sales & FAE	http://cdn.gowinsemi.c om.cn/UG
MIPI_DPHY_RX	Hard Core	GW1N-2/ GW1NR-2 /GW1NZ-2	Contact Gowin Sales & FAE	http://cdn.gowinsemi.c om.cn/IPU
MIPI_TX_Advance	Soft Core	Refer to Doc	http://cdn.gowinsemi.com.cn/Gowin_MIPI_DPHY_Advance_refDesign.zip	https://www.gowinsemi .com/en/ ail/59/
MIPI_RX_Advance	Soft Core	Refer to Doc	http://cdn.gowinsemi.com.cn/Gowin_MIPI_DPHY_Advance_refDesign.zip	https://www.gowinsemi .com/en/ ail/59/
MIPI_DSI/CSI2_Receiver	Soft Core	All Devices	https://www.gowinsemi.com/upload/database_doc/2678/document/651543b559cd7.zip	https://www.gowinsemi .com/en/ ail/143/
MIPI_DSI/CSI2_Transmitter	Soft Core	All Devices	https://www.gowinsemi.com/upload/database_doc/2676/document/65153e70b71dd.zip	https://www.gowinsemi .com/en/ ail/144/
MIPI_Byte-to-Pixel_Converter	Soft Core	All Devices	https://www.gowinsemi.com/upload/database_doc/2678/document/651543b559cd7.zip	https://www.gowinsemi .com/en/ ail/141/
MIPI_Pixel-to-Byte_Converter	Soft Core	All Devices	https://www.gowinsemi.com/upload/database_doc/2676/document/65153e70b71dd.zip	https://www.gowinsemi .com/en/ ail/142/

7 Conclusion

GOWIN's MIPI solutions aim to assist users in selecting the most suitable solution for their design needs. By delving into the evolution and diverse capabilities of MIPI standards, it highlights how these interfaces have transcended their origins in smartphones to encompass a wide array of applications, including AI, IoT, automotive, and medical devices.

GOWIN's commitment to advancing MIPI integration is evident through its pioneering development of MIPI D-PHY solutions and its expansion into C-PHY, M-PHY, and upcoming A-PHY implementations within the Arora V family. This comprehensive range of solutions caters to various performance requirements and application scenarios.

The paper has elucidated two key approaches adopted by GOWIN: the development of both hard and GPIO-based soft MIPI PHY IPs. While hard IPs ensure standards compliance and optimized performance, soft IPs leverage FPGA programmability, offering unparalleled flexibility to suit diverse application needs.

Performance benchmarks across different FPGA families underscore scalability and

adaptability, demonstrating GOWIN's commitment to meeting varying performance demands. Furthermore, GOWIN's provision of Protocol layer soft core IPs, such as MIPI CSI-2 and MIPI DSI through their EDA tool core generator, enhances the breadth of their offerings, enabling seamless integration and design experiences.

Ultimately, this white paper serves as a practical guide, empowering designers to navigate GOWIN's versatile MIPI offerings effectively. By facilitating the integration of MIPI interfaces into diverse applications, GOWIN aims to support and propel innovation across industries.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

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Revision History

Date	Version	Description
2024/02/02	1.0E	Initial version published.
2024/3/29	1.1E	-Removing GW5A-45 from MIPI solutions overview table - Added * to GPIO bases for CPHY Rx column

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