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WG7801-B0 WLAN Module

TI WiLink8 IEEE 802.11b/g/n solution

Datasheet

Revision 0.4

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1. OVERVIEW

WG7801-B0, a WiFi SiP (system in package) module, is the most demanded design for mobile devices, Audio, Computer, PDA and embedded system applications with Wilink8 solution from TI.

1.1. Models Functional Blocks

Model	WLAN 2.4GHz	WLAN 5GHz	BT/BLE
WG7801-B0	V	-	-

1.2. General Features

- WLAN with Integrated RF Front-End Module (FEM), Power Amplifier (PA), and Power Management on a Single Module
- LGA106 pin package
- Dimension 12.8mm(L) x 12.0mm(W) x 1.63mm(H)
- Provides efficient direct connection to battery by employing several integrated switched mode power supplies (DC2DC).
- Seamless Integration with TI Sitara™ and Other Application Processors
- WLAN core is software and hardware compatible with prior WL127x and WL128x offerings, for smooth migration to device.
- SDIO for WLAN.
- Temperature detection and compensation mechanism ensures minimal variation in RF performance over the entire temperature range.
- Operating temperature: –40°C to 85°C

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram

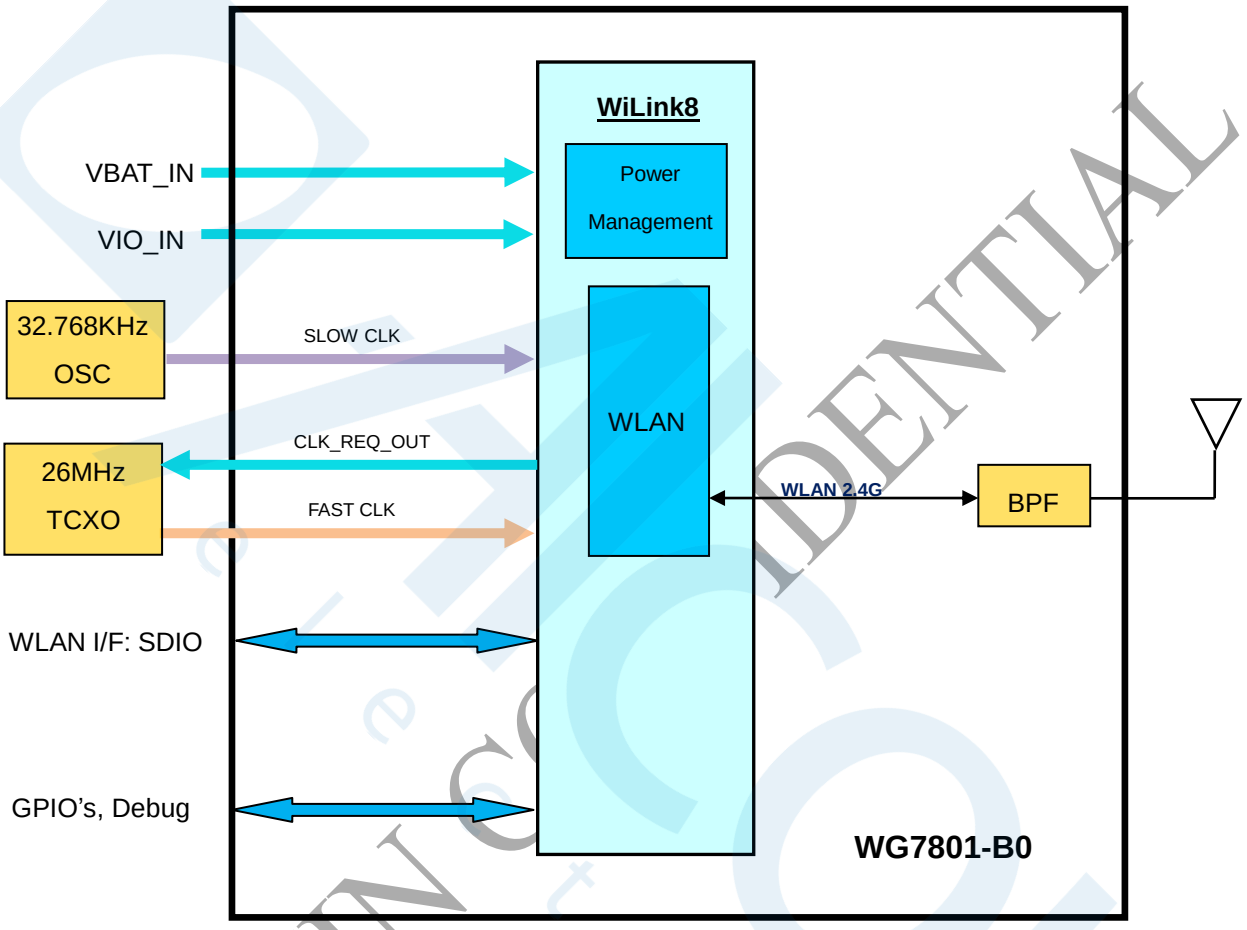


Figure 2-1. WG7801-B0 Block Diagram

2.2. Block Functional Feature

2.2.1. WLAN Features

- Integrated 2.4 GHz Power Amplifier (PA) for WLAN solution
- WLAN Baseband Processor and RF transceiver Supporting IEEE Std 802.11b/g/n
- WLAN 2.4 GHz SISO (20/40 MHz channels)
- Baseband Processor
  - IEEE Std 802.11b/g/n data rates and IEEE Std 802.11n data rates with 20 or 40 MHz SISO.
- Fully calibrated system. Production calibration not required.
- Medium Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys,
  - Supports requirements for Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [includes hardware-accelerated Advanced Encryption Standard (AES)]
  - Designed to work with IEEE Std 802.1x
- IEEE Std 802.11d,e,h,i,k,r PICS compliant.
- 2.4 GHz Radio
  - Internal LNA and PA
  - Supports: IEEE Std 802.11b, 802.11g and 802.11n
- Supports 4 bit SDIO host interface, including high speed (HS) and V3 modes.

3. MODULE OUTLINE

3.1. Signal Layout (Top View)

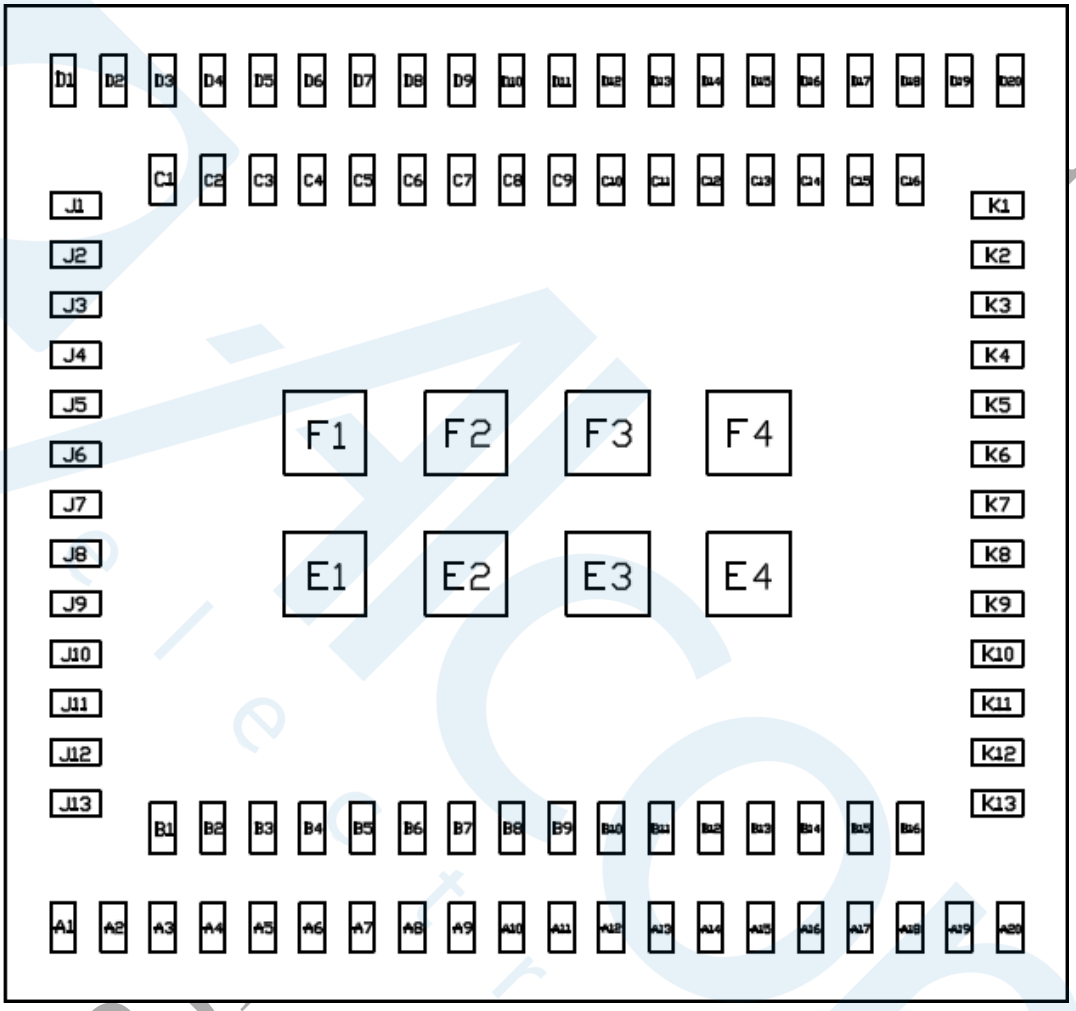


Figure 3-1 Device pins

3.2. Pin Description

Table 3-1. Pin Description

Pin No.	Signal Name	Type	Shut Down state	After Power Up(1)	Voltage Level	Description
A1	GND	GND				Ground
A2	WLAN_SDIO_D3	IO	HiZ	PU	1.8V	WLAN SDIO Data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detects. Later disabled by software during initialization. (2)
A3	WLAN_SDIO_CMD	I/O	HiZ	HiZ	1.8V	WLAN SDIO Command (2)
A4	WLAN_SDIO_D2	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 2 (2)
A5	WLAN_SDIO_D0	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 0(2)
A6	WLAN_SDIO_D1	IO	HiZ	HiZ	1.8V	WLAN SDIO Data bit 1 (2)
A7	WLAN_SDIO_CLK	IN	HiZ	HiZ	1.8V	WLAN SDIO Clock. Must be driven by the host.
A8	GND	GND				Ground
A9	BT_HCI_CTS	IN	PU	PU	1.8V	Not used. Leave NC.
A10	BT_HCI_RTS	OUT	PU	PU	1.8V	Not used. Leave NC.
A11	BT_HCI_TX	OUT	PU	PU	1.8V	Not used. Leave NC.
A12	BT_HCI_RX	IN	PU	PU	1.8V	Not used. Leave NC.
A13	NC					NC
A14	NC					NC
A15	NC					NC
A16	GND	GND				Ground
A17	NC					NC
A18	GND	GND				Ground
A19	VIO_IN	POW	PD	PD	1.8V	Connect to 1.8V external VIO
A20	GND	GND				Ground
B1	NC					NC
B2	NC					NC

B3	GPIO11	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B4	GPIO9	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B5	GPIO10	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B6	GPIO12	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B7	NC					NC
B8	NC					NC
B9	NC					NC
B10	NC					NC
B11	NC					NC
B12	NC					NC
B13	NC					NC
B14	NC					NC
B15	NC					NC
B16	NC					NC
C1	GND	GND				Ground
C2	NC					NC
C3	NC					NC
C4	BT_UART_DEBUG	OUT	PU	PU	1.8V	Not used. Leave NC.
C5	NC					NC
C6	WLAN_UART_DBG	OUT	PU	PU	1.8V	Option: WLAN logger
C7	GPIO1	I/O	PD	PD	1.8V	WL_RS232_TX (when IRQ_WL = 1 at power up)
C8	NC					NC
C9	TCXO_CLK_IN	ANA				TCXO clock input
C10	WLAN_EN	IN	PD	PD	1.8V	WLAN Mode setting: High = enable
C11	WLAN_IRQ	OUT	PD	0	1.8V	SDIO available, interrupt out. Active high. To use WL_RS232_TX and RX lines, need to pull up with 10K resistor.
C12	GND	GND				Ground
C13	GND	GND				Ground
C14	GND	GND				Ground
C15	GND	GND				Ground
C16	GND	GND				Ground
D1	GND	GND				Ground

D2	VBAT	POW			VBAT	Power supply input, 2.9 to 4.8 V
D3	NC					NC
D4	NC					NC
D5	NC					NC
D6	GND	GND				Ground
D7	NC					NC
D8	GND	GND				Ground
D9	PA_DC2DC_OUT	POW				Internal DC2DC output
D10	GPIO4	I/O	PD	PD	1.8V	Reserved for future use. NC if not used.
D11	GPIO2	I/O	PD	PD	1.8V	WL_RS232_RX (when IRQ_WL = 1 at power up)
D12	BT_EN	In	PD	PD	1.8V	Not used. Connect to GND.
D13	NC					NC
D14	NC					NC
D15	GND	GND				Ground
D16	GND	GND				Ground
D17	GND	GND				Ground
D18	GND	GND				Ground
D19	NC					NC
D20	GND	GND				Ground
E1	GND	GND				Ground
E2	GND	GND				Ground
E3	GND	GND				Ground
E4	GND	GND				Ground
F1	GND	GND				Ground
F2	GND	GND				Ground
F3	GND	GND				Ground
F4	GND	GND				Ground
J1	GND	GND				Ground
J2	GND	GND				Ground
J3	GND	GND				Ground
J4	NC					NC
J5	NC					NC
J6	NC					NC
J7	NC					NC

J8	NC					NC
J9	NC					NC
J10	CLK_REQ_OUT	OUT	PD	PD	1.8V	TCXO clock request out
J11	GND	GND				Ground
J12	GND	GND				Ground
J13	NC					NC
K1	GND	GND				Ground
K2	RF_ANT_BG	RF				WLAN 2.4G RF Port
K3	GND	GND				Ground
K4	GND	GND				Ground
K5	GND	GND				Ground
K6	GND	GND				Ground
K7	BT_AUD_OUT	OUT	PD	PD	1.8V	Not used. Leave NC.
K8	GND	GND				Ground
K9	SLOW_CLK	ANA				Input Sleep clock: 32.768 KHz
K10	GND	GND				Ground
K11	BT_AUD_IN	IN	PD	PD	1.8V	Not used. Leave NC.
K12	BT_AUD_CLK	OUT	PD	PD	1.8V	Not used. Leave NC.
K13	BT_AUD_FSYNC	OUT	PD	PD	1.8V	Not used. Leave NC.

(1) PU=pull up; PD=pull down.

(2) Host must provide PU for all non-CLK SDIO signals

4. MODULE SPECIFICATION

4.1. General Module Requirements and Operation

4.1.1. Absolute Maximum Ratings (1)

Parameter		Value	Units
VBAT		-0.5 to 5.5 (2)	V
VIO		-0.5 to 2.1	V
Input voltage to Analog pins		-0.5 to 2.1	V
Input voltage limits (CLK_IN)		-0.5 to VDD_IO	V
Input voltage to all other pins		-0.5 to (VDD_IO + 0.5V)	V
Operating ambient temperature range		-40 to +85 (3)	°C
Storage temperature range		-55 to +125	°C
ESD Stress Voltage (4)	Human Body Model (5)	>1000	V
	Charged Device Model (6)	>250	V

1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) 5.5V up to 10s cumulative in 7 years, 5V cumulative to 250s, 4.8V cumulative to 2.33 years - all includes charging dips and peaks.

3) Operating free-air temperature range. The device can be reliably operated for 7 years at ambient of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).

4) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into device.

5) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

6) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance

4.1.2. Recommended Operating Conditions

Parameter	Condition	Sym	Min	Max	Units
VBAT [1]	DC supply range for all modes		2.9	4.8	V
1.8 V IO ring power supply voltage			1.62	1.95	
IO high-level input voltage		VIH	0.65 x VDD_IO	VDD_IO	
IO low-level input voltage		VIL	0	0.35 x VDD_IO	
Enable inputs high-level input voltage		VIH_EN	1.365	VDD_IO	
Enable inputs low-level input voltage		VIL_EN	0	0.4	
High-level output voltage	@ 4 mA	VOH	VDD_IO -0.45	VDD_IO	
	@ 1 mA		VDD_IO -0.112	VDD_IO	
	@ 0.3 mA		VDD_IO -0.033	VDD_IO	
Low-level output voltage	@ 4 mA	VOL	0	0.45	
	@ 1 mA		0	0.112	
	@ 0.09 mA		0	0.01	
Input transitions time Tr/Tf from 10% to 90% (Digital IO) [2]		Tr/Tf	1	10	ns
Output rise time from 10% to 90% (Digital pins) [2]	CL < 25 pF	Tr		5.3	ns
Output fall time from 10% to 90% (Digital pins) [2]	CL < 25 pF	Tf		4.9	
Ambient operating temperature			-40	85	ºC
Maximum power dissipation	WLAN operation			2.8	W

(1) 4.8V is applicable only for 2.3 years (30% of the time). Otherwise, the maximum VBAT should not exceed 4.3V.

(2) Applies to all Digital lines except SDIO and slow clock lines

4.1.3. External Slow Clock Input (SLOW_CLK)

The supported digital slow clock is 32.768 kHz digital (square wave).

Parameter	Condition	Sym	Min.	Typ.	Max.	Units
Input slow clock Frequency				32.768		KHz
Input slow clock accuracy (Initial + temp + aging)	WLAN				+/-250	ppm
Input Transition time Tr/Tf - 10% to 90%		Tr/Tf			100	ns
Frequency input duty Cycle			15	50	85	%
Input Voltage Limits	Square Wave, DC-coupled	Vih	0.65xVDD_IO		VDD_IO	Vpeak
		Vil	0		0.35xVDD_IO	
Input Impedance			1			MΩ
Input Capacitance					5	pF

4.1.4. External Fast Clock Requirements (-40 to +85˚C)

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency			26		MHz
Frequency Accuracy	Short term (voltage and temp. effect)			± 20	ppm
	Long term (including aging)			± 20	
Input voltage limits (TCXO_CLK_IN)	Sine wave/ clipped sine wave, ac-coupled	0.2		1.4	Vp-p
Input impedance	Input resistance	20			KΩ
	Input capacitance			2.5	pF
Power-up time(1)				5	ms
Phase noise 2.4GHz for 26MHz, 20MHz SISO	Measured at 1 KHz offset			-123.4	dBc/Hz
	Measured at 10 KHz offset			-133.4	dBc/Hz
	Measured at 100 KHz offset			-138.4	dBc/Hz
Phase noise 2.4GHz for 26MHz, 40MHz SISO	Measured at 1 KHz offset			-128.4	dBc/Hz
	Measured at 10 KHz offset			-135.4	dBc/Hz
	Measured at 100 KHz offset			-139.9	dBc/Hz

(1) Power-up time is calculated from the time CLK_REQ_OUT asserted till the time the TCXO_CLK amplitude is within voltage limit specified above and TCXO_CLK frequency is within 0.1 ppm of final steady state frequency.

4.2. WLAN RF Performance

4.2.1. WLAN 2.4-GHz Receiver Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operation frequency range		2412		2484	MHz
Sensitivity 20MHz Bandwidth At < 10% PER limit	1 Mbps DSSS		-96.8	-93.9	dBm
	2 Mbps DSSS		-93.7	-91.0	
	5.5 Mbps CCK		-91.1	-88.4	
	11 Mbps CCK		-88.4	-86.2	
	6 Mbps OFDM		-92.5	-89.7	
	9 Mbps OFDM		-90.9	-88.2	
	12 Mbps OFDM		-90.0	-87.3	
	18 Mbps OFDM		-87.7	-85.0	
	24 Mbps OFDM		-84.6	-81.9	
	36 Mbps OFDM		-81.2	-78.5	
	48 Mbps OFDM		-77.0	-74.3	
	54 Mbps OFDM		-75.4	-72.9	
	MCS0 MM 4K		-90.9	-87.9	
	MCS1 MM 4K		-88.1	-85.4	
	MCS2 MM 4K		-86.4	-83.7	
	MCS3 MM 4K		-83.3	-80.6	
	MCS4 MM 4K		-79.9	-77.2	
	MCS5 MM 4K		-75.7	-73.0	
	MCS6 MM 4K		-74.0	-71.3	
	MCS7 MM 4K		-72.9	-70.2	
	MCS0 MM 4K 40MHz		-87.9	-83.2	
	MCS7 MM 4K 40MHz		-69.5	-66.0	
Max Input Level At < 10% PER limit	OFDM(11g/n)	-21.3	-11.3		dBm
	CCK	-6.3	-2.3		
Adjacent channel rejection Sensitivity level +3dB for OFDM, Sensitivity level +6dB for 11b	2Mbps DSSS	42.7			dBm
	11Mbps CCK	37.9			
	54Mbps OFDM	2.0			
LO Leakage			-80		dBm
PER Floor			1.0	2.0	%

4.2.2. WLAN 2.4-GHz Transmitter Power

Parameter	Condition	Min	Typ	Max	
Output Power - Maximum RMS output power measured at 1dB from IEEE spectral mask or EVM	1 Mbps DSSS	15.5	17.5	–	dBm
	2 Mbps DSSS	15.5	17.5	–	
	5.5 Mbps CCK	15.5	17.5	–	
	11 Mbps CCK	15.5	17.5	–	
	6 Mbps OFDM	15.5	17.5	–	
	9 Mbps OFDM	15.5	17.5	–	
	12 Mbps OFDM	15.5	17.5	–	
	18 Mbps OFDM	15.5	17.5	–	
	24 Mbps OFDM	14.5	16.7	–	
	36 Mbps OFDM	13.6	15.8	–	
	48 Mbps OFDM	12.9	15.1	–	
	54 Mbps OFDM	12.3	14.3	–	
	MCS0 MM	14.4	16.6		
	MCS1 MM	14.4	16.6		
	MCS2 MM	14.4	16.6		
	MCS3 MM	14.4	16.6		
	MCS4 MM	13.8	15.8		
	MCS5 MM	12.9	15.1		
	MCS6 MM	12.3	14.3		
	MCS7 MM	11.1	13.1		
	MCS0 MM 40MHz	12.8	15.3		
	MCS7 MM 40MHz	10.7	12.7		
Output power accuracy		-1.5		+1.5	dB
Output power resolution			0.125		dB
Operation frequency range		2412		2484	MHz
Return loss			-10		dB
Reference input impedance			50		Ω

4.3. POWER CONSUMPTION

4.3.1. Shutdown and Sleep Currents

Parameter	Power Supply Current	Typ	Max.	Unit
Shutdown mode All functions shut down.	VBAT	10	20	uA
	VIO	2	5	
WLAN sleep mode	VBAT	160	340	

4.3.2. Operating Conditions

Parameter	Power Supply Current	Typ	Max.	Unit
Connected IDEL	VBAT	750	960	uA
VBAT(1)	VBAT	420	850	mA
VIO(2)	VIO	40	450	uA

1) VBAT quoted to max operational TX consumption and periodic calibration current.

2) VIO quoted for operational IO's (WLAN + BT IF) without debug IO.

4.3.3. WLAN Power Currents

Parameter	Conditions	Typ (avg) - 25C	Max.	Units
LPM	2.4GHz RX LPM	49	61	mA
Receiver	2.4GHz RX search SISO20	54	66	mA
	2.4GHz RX search SISO40	59	72	mA
	2.4GHz RX 20M SISO 11CCK	56	72	mA
	2.4GHz RX 20M SISO 6OFDM	61	72	mA
	2.4GHz RX 20M SISO MCS7	65	77	mA
	2.4GHz RX 40MHz MCS7	77	90	mA
Transmitter	2.4GHz TX 20M SISO 6OFDM 16dBm	285	374	mA
	2.4GHz TX 20M SISO 11CCK 16dBm	273	357	mA
	2.4GHz TX 20M SISO 54OFDM 12.8dBm	247	328	mA
	2.4GHz TX 20M SISO MCS7 11.6dBm	238	321	mA
	2.4GHz TX 40M SISO MCS7 11.2dBm	243	329	mA

5. HOST INTERFACE TIMING CHARACTERISTICS

5.1. WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the WIFI module uses an SDIO interface and supports a maximum clock rate of 50MHz.

The Device SDIO also supports the following features of the SDIO V3 specification:

- 4 bit data bus
- Synchronous and Asynchronous In-Band-Interrupt
- Default and High-Speed (50MHz) timing
- Sleep/wake commands

5.2. SDIO Timing Specifications

5.2.1. SDIO Switching Characteristics – Default Rate

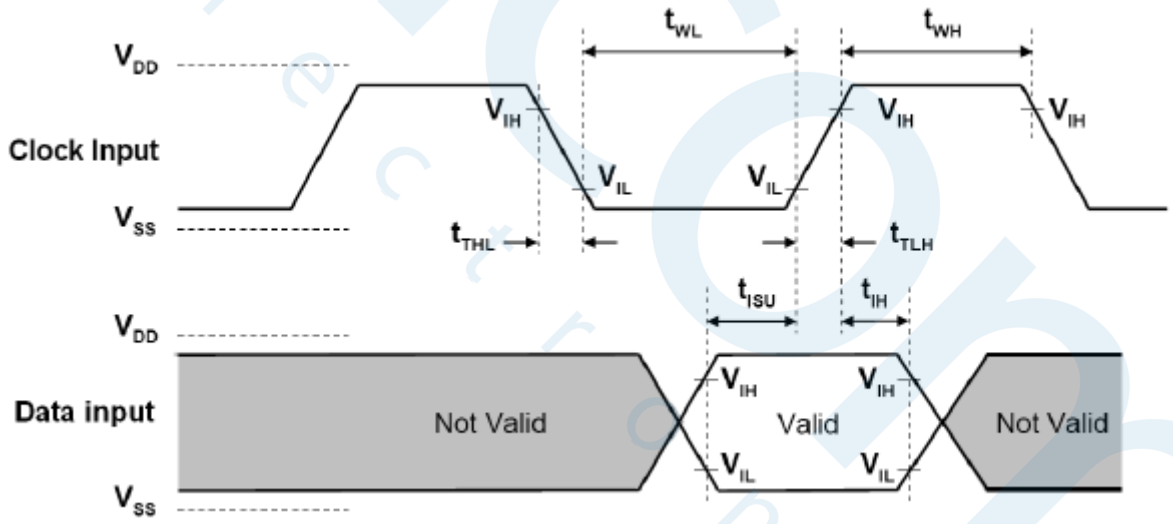


Figure 5-1. SDIO default input timing

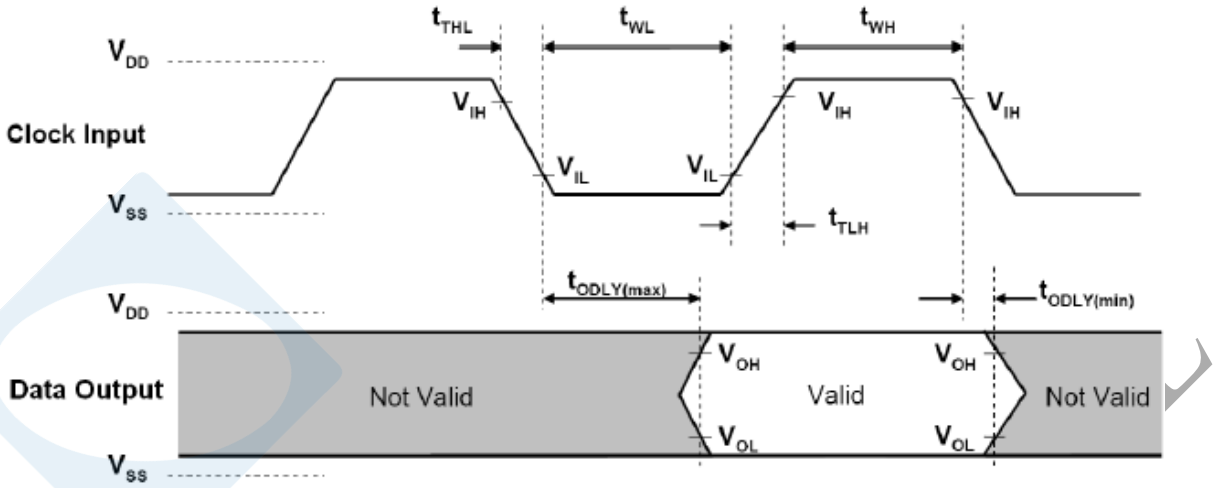


Figure 5-2. SDIO default output timing

Table 5-1. SDIO Default Timing Characteristics(1)

PARAMETER(2)		MIN	MAX	UNIT
Fclock	Clock frequency, CLK	0	26	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		10	ns
tTHL	Fall time, CLK		10	ns
tISU	Setup time, input valid before CLK↑	3		ns
tIH	Hold time, input valid after CLK↑	2		ns
tODLY	Delay time, CLK↓ to output valid	2.5	14.8	ns
CI	Capacitive load on outputs		15	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.

(2) Parameter values reflect maximum clock frequency.

5.2.2. SDIO Switching Characteristics – High Rate

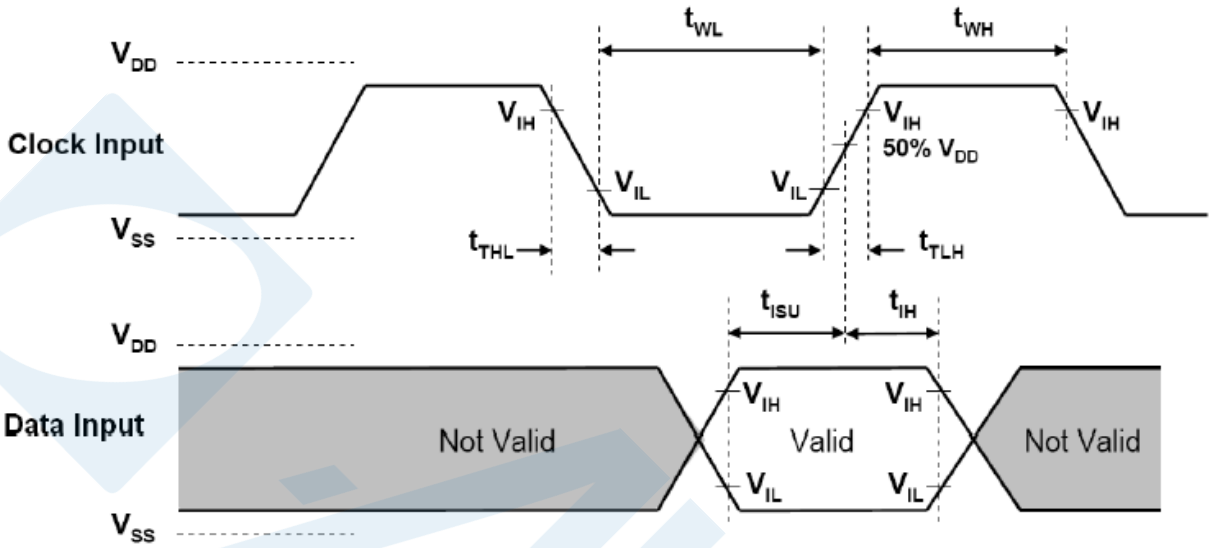


Figure 5-3. SDIO HS input timing

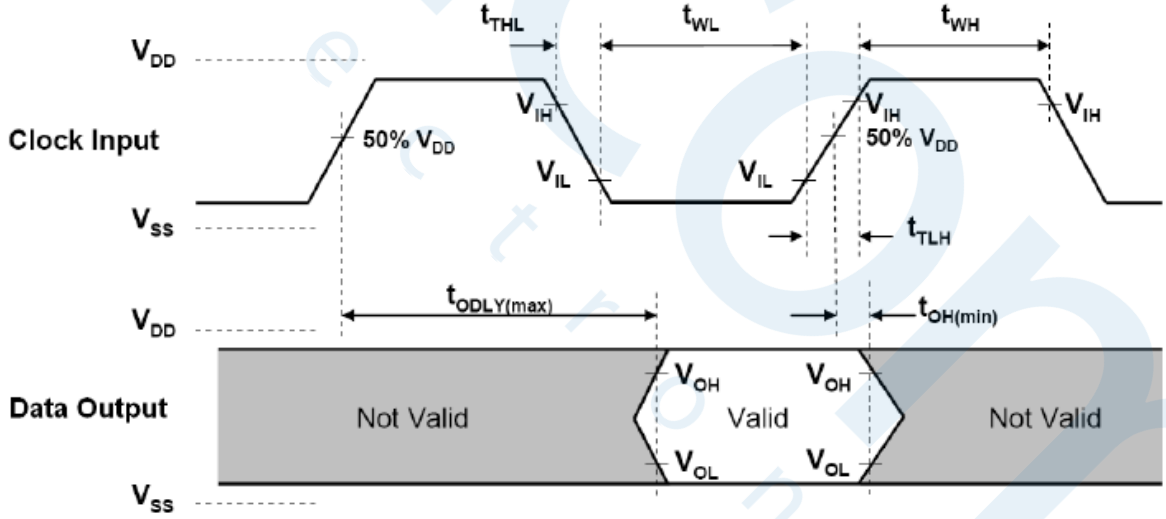


Figure 5-4. SDIO HS output timing

Table 5-2. SDIO HS Timing Characteristics

PARAMETER		MIN	MAX	UNIT
Fclock	Clock frequency, CLK	0	50	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		3	ns
tTHL	Fall time, CLK		3	ns
tISU	Setup time, input valid before CLK↑	3		ns
tIH	Hold time, input valid after CLK↑	2		ns
tODLY	Delay time, CLK↓ to output valid	2.5	14	ns
CI	Capacitive load on outputs		10	pF

6. CLOCK AND POWER MANAGEMENT

The slow clock is a free-running, 32.768 kHz clock supplied from an external clock source. The clock is connected to the SLOW_CLK pin and is a digital square-wave signal in the range of 0 to 1.8V nominal

6.1. Reset-Power-Up System

After VBAT and VIO are fed to the device and while WL_EN is deasserted (low), the device is in SHUTDOWN state, during which functional blocks, internal DC-DCs, and LDOs are disabled. The power supplied to the functional blocks is cut off. When one of the signal (WL_EN) is asserted (high), a power-on reset (POR) is performed. Stable slow clock, VIO, and VBAT are prerequisites for a successful POR.

6.2. WLAN Power-Up Sequence

Figure 6-1 shows the WLAN power-up sequence.

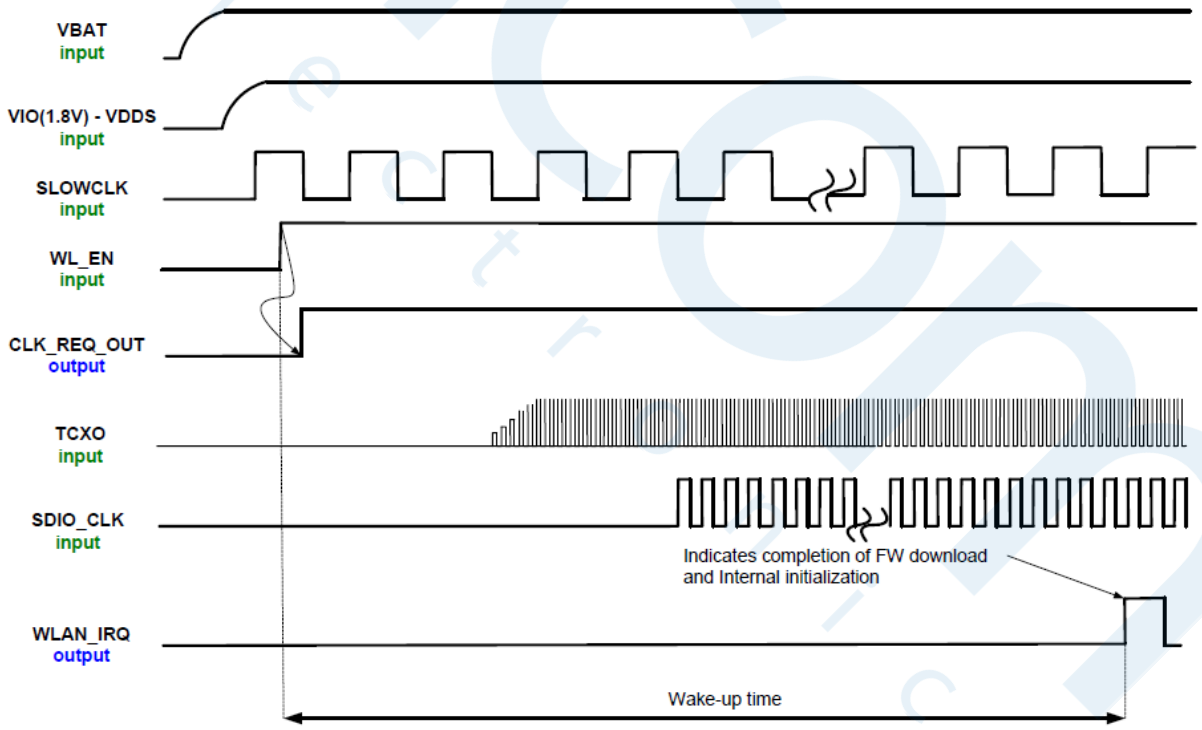


Figure 6-1. WLAN Power-Up Sequence

7. REFERENCE SCHEMATIC

7.1. Module Reference Design

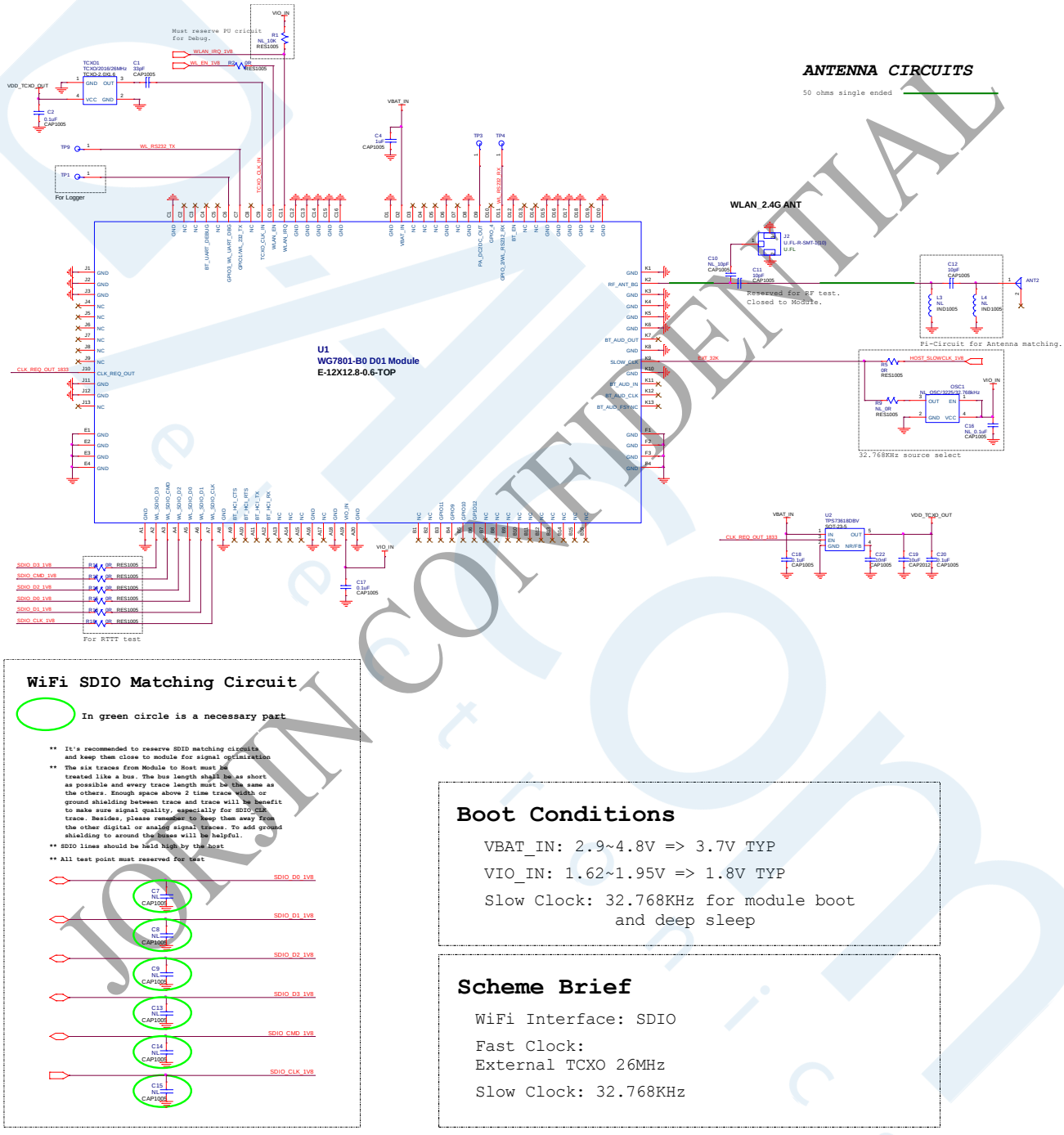


Figure 7-1 Module Reference Schematic

8. DESIGN RECOMMENDATIONS

8.1. Design Note on Debug Port

- Pin# C6 serves as WLAN debug port, respectively. So test point for this signal should be reserved for debugging purpose.
- Pin# C11 (WLAN_IRQ) needs to be pulled high via 10Kohm and use Pin# D11, C7 (WL_RS232_RX, WL_RS232_TX) as hardware interface to communicate with system platform and TI RTTT test utility for WLAN RF performance test, debug and manufacturing application.

8.2. Module Layout Recommendations

Follow these module layout recommendations:

- Digital Signals Layout
  - SDIO signals traces (CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible. **(Less than 12cm) Besides, every trace length must be the same as the others.**
  - Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Remember to keep them away from the other digital or analog signal traces. Adding ground shielding around these bus is recommended.
  - Route trace of SDIO_CLK at Top layer without vias.
  - SDIO Clock, this digital clock signal is a source of noise. Keep the trace of this signal as short as possible. Whenever possible, maintain a clearance around them.

- RF Trace & Antenna
  - Keep 50ohm trace impedance.
  - Move all the high-speed traces and components far away from the antenna.
  - Check antenna vendor for the layout guideline and clearance.

- Power Trace
  - Power trace for VBAT should be 20mil wide. 1.8V trace should be 15mil wide, at least.
  - Isolate different power traces with Ground plane

- Ground

- Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation.
- Have a complete Ground pour in layer 2 for thermal dissipation.
- Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
- Move GND vias close to the pad.

- Clocks
  - To avoid adding noise to the clock signal, keep the primary clock away from fast digital switching lines and power traces.
  - It is preferable to keep all clocks between the ground/power layers.
  - Primary TCXO placement
    - To reduce clock drift, place the TCXO far from a heat source on the board.
    - For better thermal mass, ensure good grounding for the TCXO.
    - If the TCXO cannot be placed far from a heat source, add a scratch in the ground layers to isolate the heat spreading toward the TCXO

9. PACKAGE INFORMATION

9.1. Module Mechanical Outline

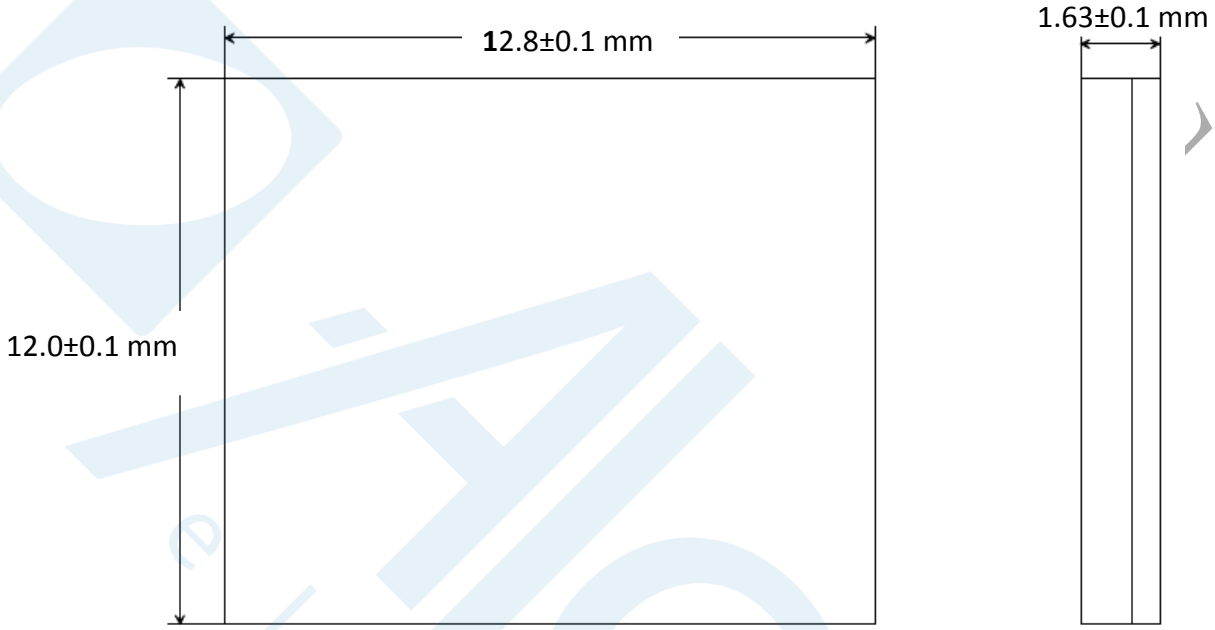


Figure 9-1. Module mechanical outline

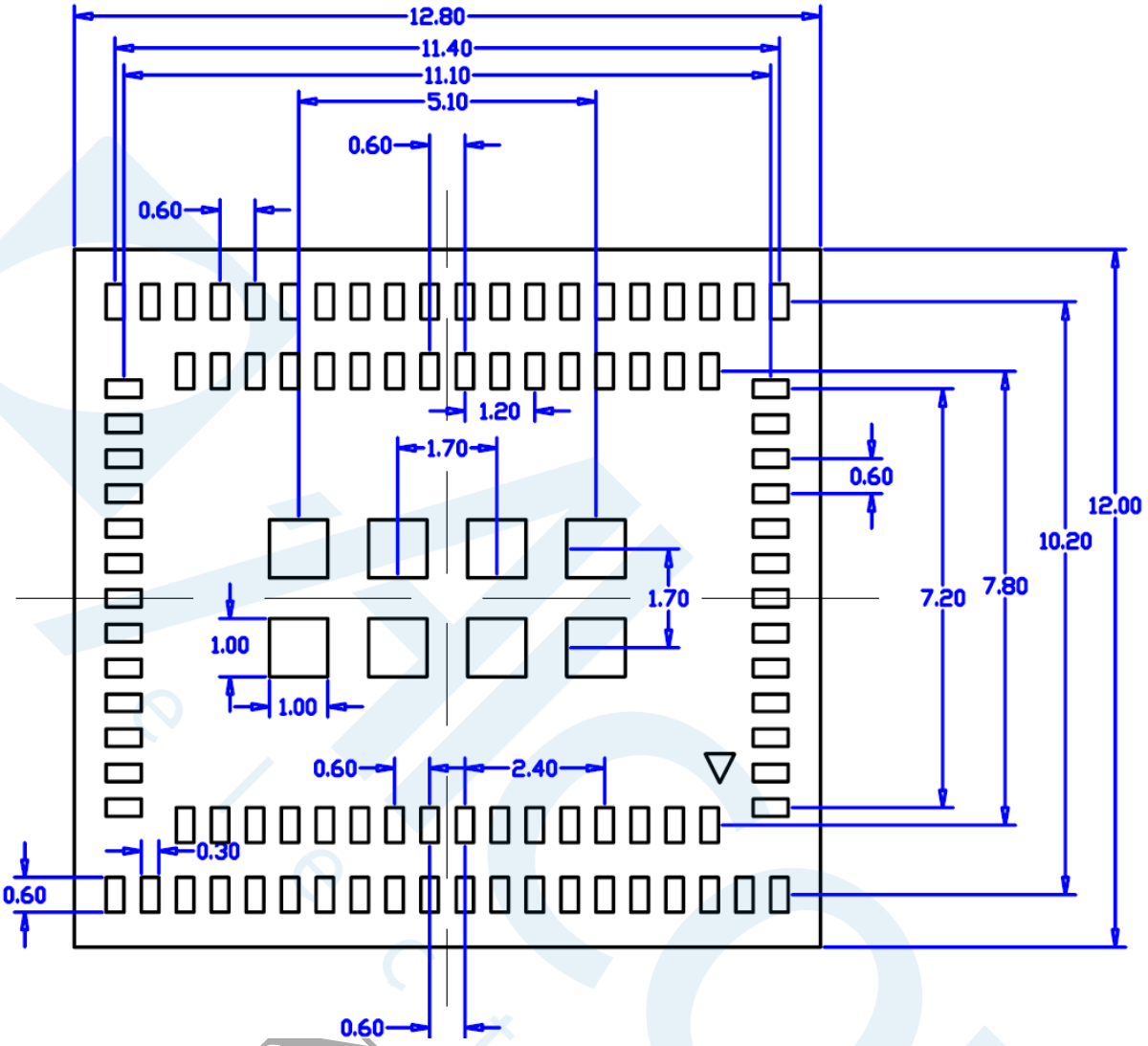


Figure 9-2. Module pad dimensions

*We recommend adopting the same dimensions listed above for building PCB footprint.

** Pad tolerance as +/- 30um

9.2. Ordering Information

Part number:	WG7801-B0

9.3. Package Marking

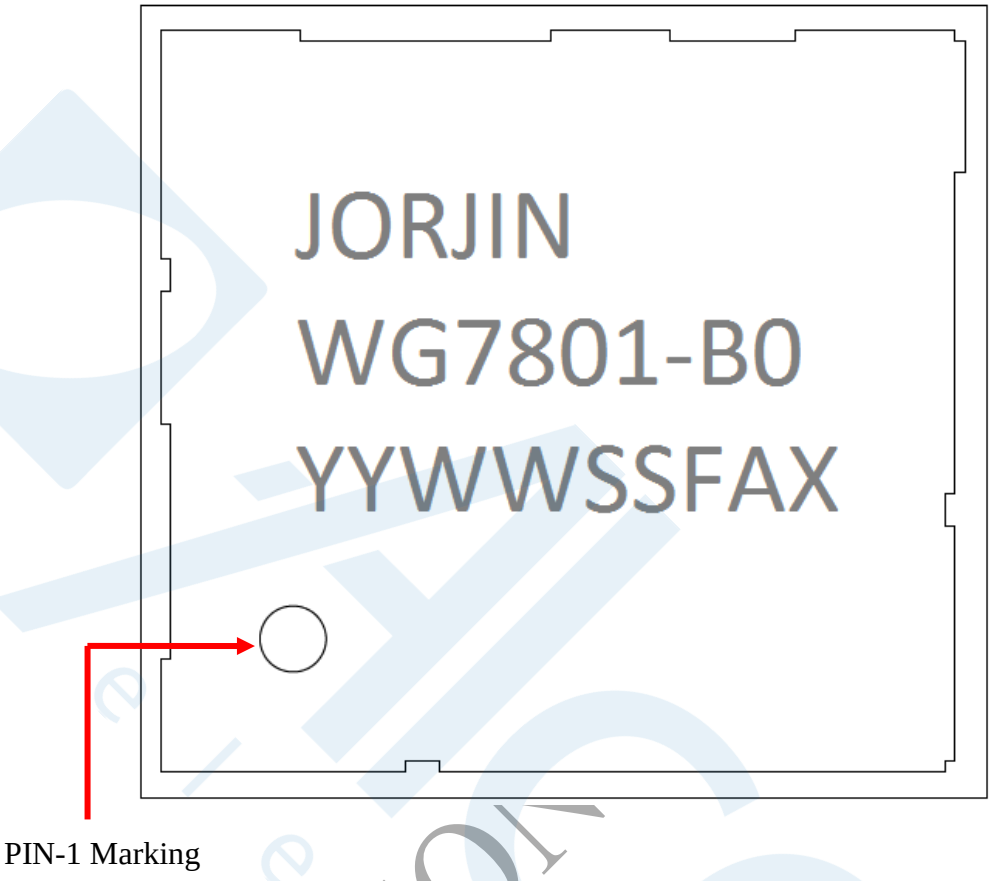


Figure 9-3. Package Marking

Date Code: **YYWWSSFAX**

YY = Digit of the year, ex: 2011=11

WW = Week (01~52)

SS = Serial number from 01 ~99 match to manufacture's lot number

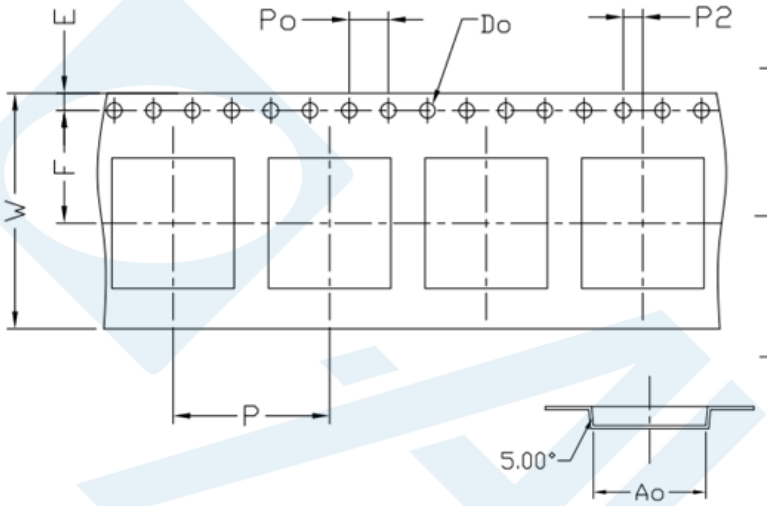
F = Reserve for internal use

A = Module version from A to Z

X = Chip version

9.4. Packaging

9.4.1. Tape Specification

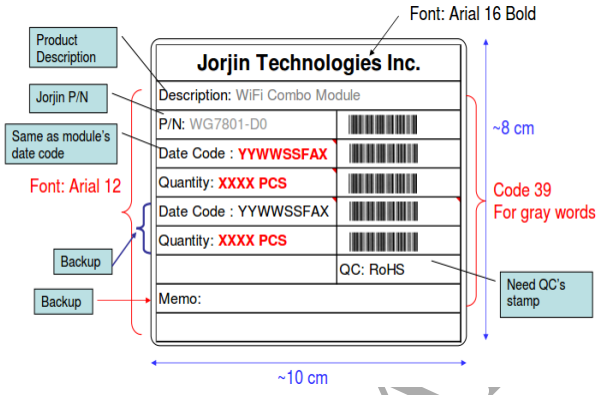


ITEM	DIM	ALTERNATE
W	24.00 +0.30 −0.30	
E	1.75 +0.10 −0.10	
F	11.50 +0.10 −0.10	
P	16.00 +0.10 −0.10	
Po	4.00 +0.10 −0.10	
P2	2.00 +0.10 −0.10	
Do	ø1.50 +0.10 −0.00	
T	0.35 +0.05 −0.05	
Ao	12.50 +0.10 −0.10	
Bo	13.30 +0.10 −0.10	
Ko	2.10 +0.10 −0.10	

<Reel : 1.8K pcs per reel>

<Pizza box : 1 reel per pizza box>

<Carton : 5 pizza boxes per carton>



Product label

10. SMT AND BAKING RECOMMENDATION

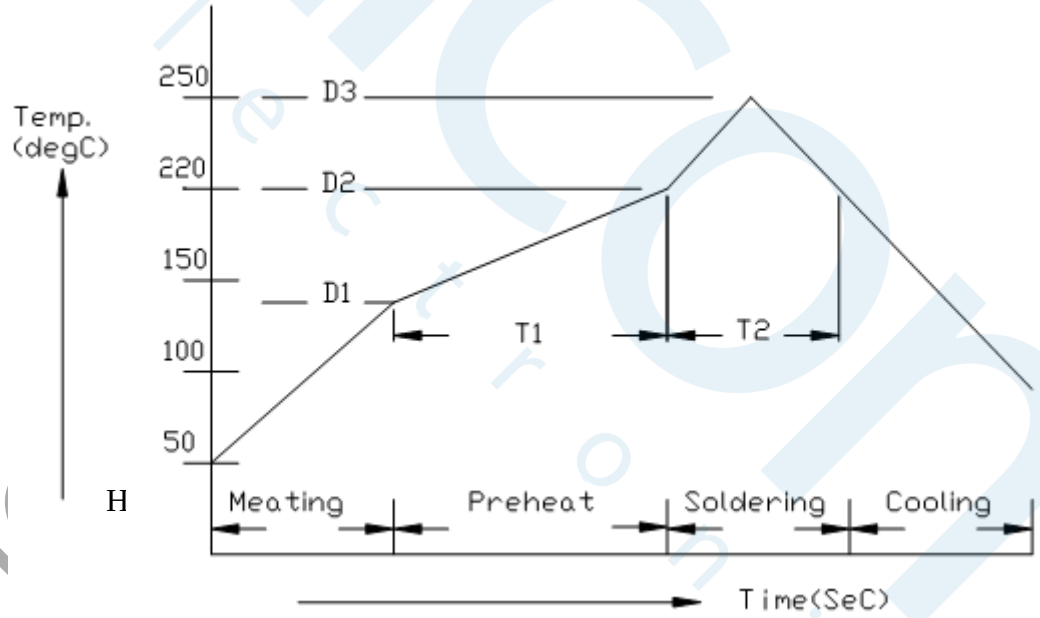
10.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs. at 125 °C.

10.2. SMT Recommendation

- Recommended Reflow profile：



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

- **Stencil thickness**： 0.1~ 0.13 mm (Recommended)
- **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

11. HISTORY CHANGE

Revision	Date	Description
R 0.1	2014/08/28	New Released
R 0.2	2014/09/29	Modify the module thickness from 1.7±0.05 mm to 1.63±0.1 mm Modify the package marking.
R 0.3	2015/01/05	Separated from WG78XX-B0 series datasheet.
R 0.4	2015/11/17	1. Corrected functional block table.