Plus1 Story

Although there are many embedded Linux CPUs on the market, few were designed to address the needs of the IoT and industrial control markets directly. Most CPUs found on popular boards such as the Raspberry Pi were initially meant for something else (for example, a set-top box) and were merely repurposed for the needs of the IoT and industrial control communities.

Such CPUs usually have adequate processing power but lack I/O features, which is not surprising: Set-top boxes have very different I/O needs than IoT or industrial control devices. These CPUs are also rather complex, need multiple additional components to work, are available only in difficult-to-handle BGA packaging, and require six or eight-layer boards. All this poses severe obstacles to low and medium-volume device vendors.

Take the BGA packaging as an example. Everything about BGA is an order of magnitude more complex compared to other packaging choices, such as LQFP. BGA represents the cut-off line, where it becomes impossible to handle the chips manually. Everything from soldering to desoldering and verifying the assembly quality requires specialized and expensive equipment. Smartphone manufacturers accept BGA challenges as the inevitable side effect of the desired board miniaturization that the technology enables, but vendors of IoT or industrial control devices view this differently. IoT and industrial control products rarely have any size pressure, and having to deal with ever-smaller IC packages only brings complications without any apparent benefits.

As another example, consider the logic levels of GPIO lines. As processor designs take advantage of ever-more advanced fabrication processes, chip supply voltages have also decreased. Subsequently, standard semiconductor I/O libraries have dropped support for 5V and even 3.3V logic levels. This did not bother the designers of set-top boxes and other "closed" products but was bad news for the architects of control hardware.

To summarize, there was an apparent gap between existing processor offerings and the requirements of IoT and industrial control applications. Recognizing the unmet needs of IoT and industrial control vendors, Sunplus Technology Co., Ltd. and Tibbo Technology, Inc. in late 2017 set out to develop a Linux-grade chip that would directly address these markets. The idea was to create a powerful SoC with I/O features and packaging specifically targeting IoT and industrial control applications, as well as the needs of low-to-medium-volume hardware manufacturers. Thus, the Plus1 concept was born.

Here are the key characteristics of the SP7021, the first member of the new Plus1 line:

- Easy-to-use LQFP package
- Quad-core 1GHz Cortex-A7 CPU, plus A926 and 8051 cores
- Single 3.3V power*
- Integrated 128MB or 512MB DDR3 DRAM
- Eight 8-bit 5V-tolerant I/O ports, plus one high-current port
- Flexible Peripheral Multiplexing (PinMux)
- Dual PinMuxable Ethernet MACs
- Four PinMuxable Enhanced UARTs, plus one console UART
- Industrial operating temperature range: -40°C to 85°C
- Low EMI simplifies certification
- Modern, Yocto-based Linux distribution
- Ten-year supply guarantee
- And much more...

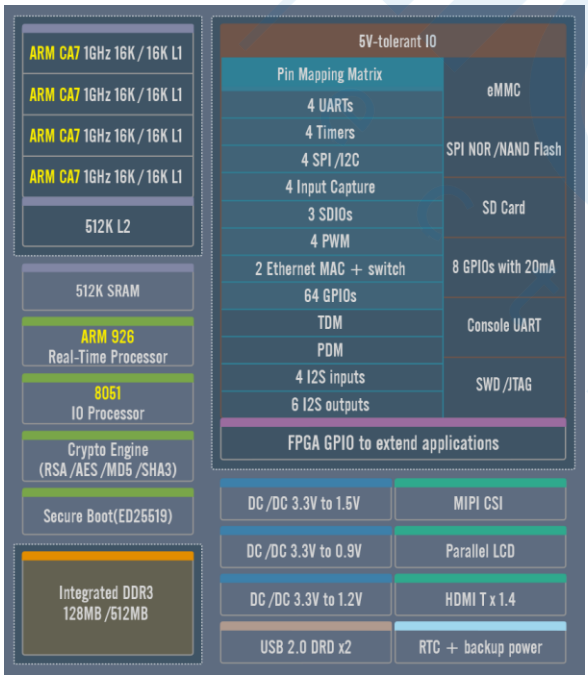
**Some limitations apply*

Plus1 (SP7021) Hardware Specifications

- Easy-to-use 20x20mm LQFP176-EP package
- Processing cores
  - Quad-core ARM Cortex-A7 (CA7)
    - Operating speed up to 960MHz
    - NEON multimedia processing engine (SIMDv2/VFPv4 ISA)
    - 16KB L1 I-cache and 16KB L1 D-cache
    - 512KB unified L2 cache
    - Generic Interrupt Controller (GIC) v2.0
  - ARM926 real-time core
    - Operating speed up to 202MHz
    - 16KB I/D cache
    - 32KB L1 I-cache and 32KB L1 D-cache
  - 8051 low-power core
    - Selectable 32KHz or 202MHz operating speed
    - Intended to be used as a supervisory core
    - Low-power operation—500uA @ 32KHz for the entire IC
  - All I/O lines and peripherals are accessible from all cores of the chip
- Single 3.3V power*
  - Built-in regulators for 1.5V, 1.2V*, and 0.9V power
  - Only a few passive components to be added externally
- Integrated DDR3 DRAM
  - SP7021-IS: 128MB
  - SP7021-IF: 512MB
- General-purpose I/O (GPIO) ports
  - Nine 8-bit ports (P0-8)
  - All GPIO lines have 3.3V logic levels
  - 16mA source/sink current for all lines of GPIO port 0
  - GPIO lines of ports 1-8 are **5V-tolerant**
  - Eight individual interrupt lines
  - Interrupt lines can be configured as wake-up lines of the chip
  - Each GPIO line can be individually
    - Tri-stated (work as an input) or enabled (work as outputs)
    - Configured as a push-pull or open collector output
    - Configured as a regular or Schmitt trigger input
    - Each line's signal can be inverted on the way in or out
  - Two ways of controlling GPIO lines
    - Through 8-bit registers (eight lines read or written simultaneously)
    - Using bitwise access to individual lines
- Flexible Peripheral Multiplexing (PinMux)
  - Any line of these peripherals can be connected to any line of P1-8
    - Dual Ethernet MACs
    - SDIO interface
    - Two PWM modules (with four channels in each module)
    - Four SPI modules
    - Four I2C modules
    - Four enhanced UARTs
    - Four timers/counters
    - Eight interrupts.
- Dual PinMuxable Ethernet MACs
  - Two IEEE 802.3 10/100Mb ports with RMII interface
  - Support for half and full-duplex communications
  - Two operating modes
    - Single NIC/daisy chain — the chip acts as an unmanaged switch transparently routing external traffic between two ports:
      - The built-in switch features a 1K MAC address table with programmable aging time
    - Dual NICs — two independent Ethernet interfaces

    - Support for IEEE802.1Q VLAN tagging and un-tagging
    - Support for MAC cloning and MAC security
    - Support of four traffic classes (per IEEE802.1D-2004)
- Five UARTs:
    - Four PinMuxable Enhanced UARTs
        - 128-byte TX and 128-byte RX FIFOs on each UART
        - Optional automatic RTS/CTS flow control
    - One fixed console UART (TX and RX lines only) in P0
    - Baudrates up to 921,600bps (with baud rate deviation under 3%)
    - Clocking from internal 27MHz source or CLK pin
    - Independent TX and RX DMA channels for each port
- Flash interface
    - Supports eMMC, SPI NAND, and SPI NOR memories
    - Supports BCH error correction
    - 1-bit, 2-bit, and 4-bit interface modes
- PinMuxable SD2.0 interface
- PinMuxable SDIO (SD2.0) interface (for connecting a Wi-Fi/BT module)
- Two OTG USB2.0 ports with Linux boot and USB video class support
- Four PinMuxable SPI modules
    - Support for master and slave modes
    - 8-byte RX and 8-byte TX FIFOs in each module
    - Independent TX and RX DMA channels in each module

** An external 1.2V power regulator is required if the chip's current consumption on the 1.2V rail exceeds 1,200mA.*



SP7021 Block Diagram

- Four PinMuxable I2C modules
    - Support for master and slave modes
    - Optional clock stretching
    - 32-byte RX and 32-byte TX FIFOs in each module
    - Independent TX and RX DMA channels in each module
- Two PinMuxable PWM modules
    - Four synchronized PWM channels in each module

    - Clock frequency up to 70MHz
    - 8-bit resolution for each channel
- Up to four 8-bit or up to two 16-bit PinMuxable timers/counters
- Four PinMuxable capture modules
- MIPI-CSI camera port
    - Supports up to two cameras
    - Compliant with
        - MIPI CSI-2 Specification, rev. 1.01
        - MIPI D-PHY interface Specification, v1.1
    - Supported modes
        - High-speed (HS) mode—1.0Gbps per lane
        - Low-power (LP) mode—10Mbps per lane
    - Camera resolution up to 1328x864 (Including non-image data)
    - Frame rate up to 60fps
    - 10 bits per pixel color depth
    - 810Mbps total bandwidth
    - Power-down mode
    - MIPI CSI-2 short- and long-packet formats
    - Supports MIPI CSI-2 one data lane
    - Supports MIPI CSI-2 RAW8 and RAW10 data formats
- MIPI video interface supports resolutions up to 1366x768/1312x816
- HDMI 1.4 video interface supports resolutions up to 720p
- TFT LCD controller with parallel bus interface (res. up to 320x240x24)
- I2S/SPDIF/PWM audio output for up to five channels
- PDM interface for 8-channel MEMS microphone array
- 32-bit FPGA bus IO (FBIO) interface
- Temperature sensor for estimating the internal temperature of the IC
- Real-time clock (RTC)
    - Alarm function with a dedicated output pin
    - Dedicated backup power input
    - Built-in charging circuit for a rechargeable battery (supercapacitor)
- 128-byte one-time programmable (OTP) memory
    - Preprogrammed before shipping
        - Vendor and device ID
        - Serial number
        - Two registered MAC addresses
    - 64 bytes are available to the user
    - No high-voltage or additional hardware required for programming
- SWD and JTAG debug interfaces
- Watchdog timer
- Secure boot: boot image verified by ED25519 algorithm
- Crypto engines
    - PKA engine (RSA)
    - Hash engine (SHA3, MD5)
    - Encryption/decryption engine (AES)
- Industrial operating temperature range: -40°C to 85°C
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