NuMicro® Family

Arm® Cortex®-M0-based Microcontroller

M071MD2AE/M071MC2AE

Datasheet

Nuvoton is providing this document only for reference purposes of NuMicro® microcontroller and microprocessor based system design. Nuvoton assumes no responsibility for errors or omissions.

All data and specifications are subject to change without notice.

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

TABLE OF CONTENTS

List of Figures

List of Tables

1 GENERAL DESCRIPTION

The NuMicro® M071M is a 32-bit microcontroller based on Arm Cortex®-M0 core targeted for smart home appliance applications. It offers up to 50 MHz CPU frequency, 68 KB Flash memory for code storage, 8 KB SRAM for runtime operation. Additionally, in response to the code security requirements, the M071M integrates flash security lock to provide a secure code execution area to protect the developer's intellectual property. The M071M also supports online updates using In-System Programmer (ISP), In-Circuit Programmer (ICP) and In-Application Programmer (IAP). The In-System Programmer (ISP) with 4 KB Loader ROM (LDROM) supports firmware updates through the Firmware Over-The-Air (FOTA) process.

The M071M supports plenty of peripherals, including one built-in temperature sensor with 1°C resolution, adjustable VDDIO pins to meet a wide voltage range from 1.8V to 5.5V, 12 channels of 16-bit 144 MHz high-speed PWM for precise control, 4 sets of UART, 1 set of SPI, 1 set of I²C. The M071M also provides rich analog peripherals including 8 channels of 12-bit ADC.

1.1 Key Features Support Table

Product Line	UART	SPI	I²C	Timer	PWM	ADC	Package
M071M	4	1	1	4	12	12	LQFP44(10x10)

Table 1.1-1 M071M Connectivity Support Table

2 FEATURES

- Arm® Cortex®-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 68/36 KB Flash for program code
  - Configurable Flash memory for data memory (Data Flash), 4 KB Flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for Flash
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8 KB SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 °C and V_{DD} = 5 V
    - Trimmed to ±2 % at -40 °C ~ +105°C and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, output frequency up to 200 MHz, PWM clock frequency up to 100 MHz, and System operation frequency up to 50 MHz
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter

- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function

- Watchdog Timer
  - Multiple clock sources
    - System clock (HCLK)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- PWM/Capture
  - Supports maximum clock frequency up to 100 MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition

- Supports input rising edges, falling edges or both edges capture interrupt
- Supports rising edges, falling edges or both edges capture with counter reload option

- UART
  - Up to 4 UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports three wire, no slave select signal, bi-direction interface
- I^2C
  - One set of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- ADC
  - 12-bit SAR ADC with 760 KSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels

  - Threshold voltage detection
  - Conversion started by software programming or external input
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ +105°C
- Packages:
  - All Green package (RoHS)
  - LQFP 44-pin (10mm x 10mm)

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

LQFP 44
M071MC2AE
M071MD2AE

3.2 M071M Selection Code

PART NUMBER		M071MC2AE	M071MD2AE
Flash (KB)		36	68
Data Flash (KB)		Configurable	
SRAM (KB)		8	
LDROM (KB)		4	
PLL (MHz)		200	
LXT		-	
I/O		38	
32-bit Timer		4	
PWM		12	
BPWM		-	
WDT/WWDT		√	
RTC		-	
Connectivity	USCI*	-	
	UART	4	
	SPI	1	
	I^2C	1	
	SC/UART	-	
	EBI	-	
	PSIO	-	
12-bit ADC		12	
ACMP		-	
USB 2.0 FS Device		-	
PDMA		-	
V_{BAT} pin		-	
ISO-7816-3		-	
Package		LQFP44*	

Conf*: Configurable
LQFP44*: 10x10 mm

3.3 M071M Naming Rule

M0	71	M	D	2	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex®-M0	71: Home appliance	Q: LQFP44 (10x10) 0.8mm	C: 36 KB D: 68 KB	2: 8 KB		E:-40˚C ~ 105˚C

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Multi-function Pin Diagram

4.1.1 M071M LQFP44-Pin Multi-function Pin Diagram

Corresponding Part Number: M071MD2AE, M071MC2AE

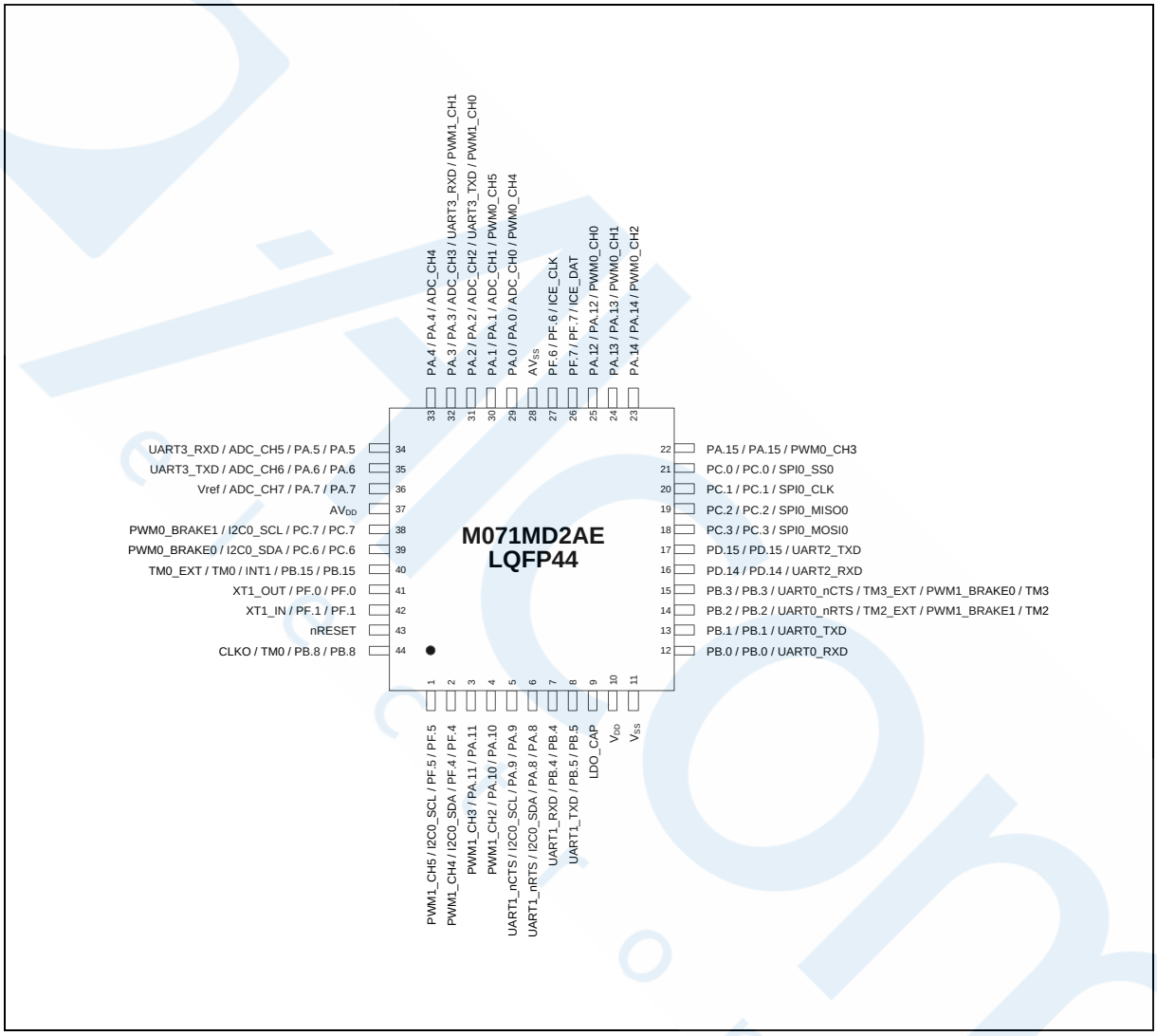


Figure 4.1-1 M071M LQFP 44-pin Diagram

4.2 Pin Function Description

4.2.1 M071M Pin Description

Pin No. LQFP 44-pin	Pin Name	Pin Type	Description
1	PF.5	I/O	General purpose digital I/O pin.
	I2C0_SCL	I/O	I2C0 clock pin.
	PWM1_CH5	I/O	PWM1 CH5 output/Capture input.
2	PF.4	I/O	General purpose digital I/O pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	PWM1_CH4	I/O	PWM1 CH4 output/Capture input.
3	PA.11	I/O	General purpose digital I/O pin.
	PWM1_CH3	I/O	PWM1 CH3 output/Capture input.
4	PA.10	I/O	General purpose digital I/O pin.
	PWM1_CH2	I/O	PWM1 CH2 output/Capture input.
5	PA.9	I/O	General purpose digital I/O pin.
	I2C0_SCL	I/O	I2C0 clock pin.
	UART1_nCTS	I	Clear to Send input pin for UART1.
6	PA.8	I/O	General purpose digital I/O pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	UART1_nRTS	O	Request to Send output pin for UART1.
7	PB.4	I/O	General purpose digital I/O pin.
	UART1_RXD	I	Data receiver input pin for UART1.
8	PB.5	I/O	General purpose digital I/O pin.
	UART1_TXD	O	Data transmitter output pin for UART1.
9	LDO_CAP	P	LDO output pin.
10	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
11	V_{SS}	P	Ground pin for digital circuit.
12	PB.0	I/O	General purpose digital I/O pin.
	UART0_RXD	I	Data receiver input pin for UART0.
13	PB.1	I/O	General purpose digital I/O pin.
	UART0_TXD	O	Data transmitter output pin for UART0.
14	PB.2	I/O	General purpose digital I/O pin.
	UART0_nRTS	O	Request to Send output pin for UART0.
	TM2_EXT	I	Timer2 external capture input pin.

Pin No. LQFP 44-pin	Pin Name	Pin Type	Description
	TM2	O	Timer2 toggle output pin.
	PWM1_BRAKE1	I	PWM1 brake input pin.
15	PB.3	I/O	General purpose digital I/O pin.
	UART0_nCTS	I	Clear to Send input pin for UART0.
	TM3_EXT	I	Timer3 external capture input pin.
	TM3	O	Timer3 toggle output pin.
	PWM1_BRAKE0	I	PWM1 brake input pin.
16	PD.14	I/O	General purpose digital I/O pin.
	UART2_RXD	I	Data receiver input pin for UART2.
17	PD.15	I/O	General purpose digital I/O pin.
	UART2_TXD	O	Data transmitter output pin for UART2.
18	PC.3	I/O	General purpose digital I/O pin.
	SPI0_MOSI0	I/O	SPI0 MOSI (Master Out, Slave In) pin.
19	PC.2	I/O	General purpose digital I/O pin.
	SPI0_MISO0	I/O	SPI0 MISO (Master In, Slave Out) pin.
20	PC.1	I/O	General purpose digital I/O pin.
	SPI0_CLK	I/O	SPI0 serial clock pin.
21	PC.0	I/O	General purpose digital I/O pin.
	SPI0_SS0	I/O	SPI0 slave select pin.
22	PA.15	I/O	General purpose digital I/O pin.
	PWM0_CH3	I/O	PWM0 CH3 output/Capture input.
23	PA.14	I/O	General purpose digital I/O pin.
	PWM0_CH2	I/O	PWM0 CH2 output/Capture input.
24	PA.13	I/O	General purpose digital I/O pin.
	PWM0_CH1	I/O	PWM0 CH1 output/Capture input.
25	PA.12	I/O	General purpose digital I/O pin.
	PWM0_CH0	I/O	PWM0 CH0 output/Capture input.
26	PF.7	I/O	General purpose digital I/O pin.
	ICE_DAT	I/O	Serial wire debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
27	PF.6	I/O	General purpose digital I/O pin.
	ICE_CLK	I	Serial wire debugger clock pin.

Pin No. LQFP 44-pin	Pin Name	Pin Type	Description
			Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
28	AV_{SS}	AP	Ground pin for analog circuit.
29	PA.0	I/O	General purpose digital I/O pin.
	ADC_CH0	AI	ADC_CH0 analog input.
	PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
30	PA.1	I/O	General purpose digital I/O pin.
	ADC_CH1	AI	ADC_CH1 analog input.
	PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
31	PA.2	I/O	General purpose digital I/O pin.
	ADC_CH2	AI	ADC_CH2 analog input.
	PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
	UART3_TXD	O	Data transmitter output pin for UART3.
32	PA.3	I/O	General purpose digital I/O pin.
	ADC_CH3	AI	ADC_CH3 analog input.
	PWM1_CH1	I/O	PWM1 CH1 output/Capture input.
	UART3_RXD	I	Data receiver input pin for UART3.
33	PA.4	I/O	General purpose digital I/O pin.
	ADC_CH4	AI	ADC_CH4 analog input.
34	PA.5	I/O	General purpose digital I/O pin.
	ADC_CH5	AI	ADC_CH5 analog input.
	UART3_RXD	I	Data receiver input pin for UART3.
35	PA.6	I/O	General purpose digital I/O pin.
	ADC_CH6	AI	ADC_CH6 analog input.
	UART3_TXD	O	Data transmitter output pin for UART3.
36	PA.7	I/O	General purpose digital I/O pin.
	ADC_CH7	AI	ADC_CH7 analog input.
	V_{REF}	AP	Voltage reference input for ADC.
37	AV_{DD}	AP	Power supply for internal analog circuit.
38	PC.7	I/O	General purpose digital I/O pin.
	I2C0_SCL	I/O	I2C0 clock pin.
	PWM0_BRAKE1	I	PWM0 brake input pin.
39	PC.6	I/O	General purpose digital I/O pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.

Pin No. LQFP 44-pin	Pin Name	Pin Type	Description
	PWM0_BRAKE0	I	PWM0 brake input pin.
40	PB.15	I/O	General purpose digital I/O pin.
	INT1	I	External interrupt1 input pin.
	TM0_EXT	I	Timer0 external capture input pin.
	TM0	O	Timer0 toggle output pin.
41	PF.0	I/O	General purpose digital I/O pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
42	PF.1	I/O	General purpose digital I/O pin.
	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
43	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.
44	PB.8	I/O	General purpose digital I/O pin.
	TM0	I/O	Timer0 event counter input / toggle output.
	CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 M071M Block Diagram

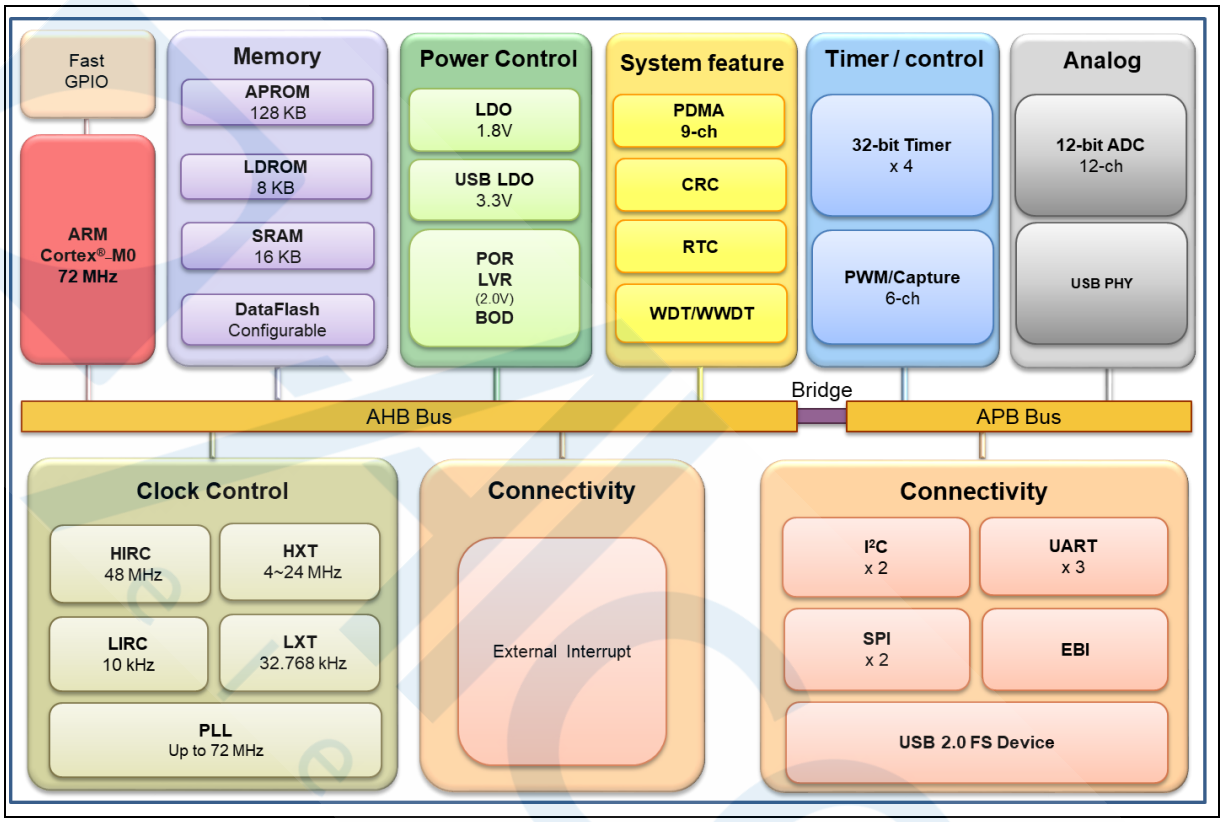


Figure 5.1-1 M071M Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6.1-1 shows the functional controller of processor.

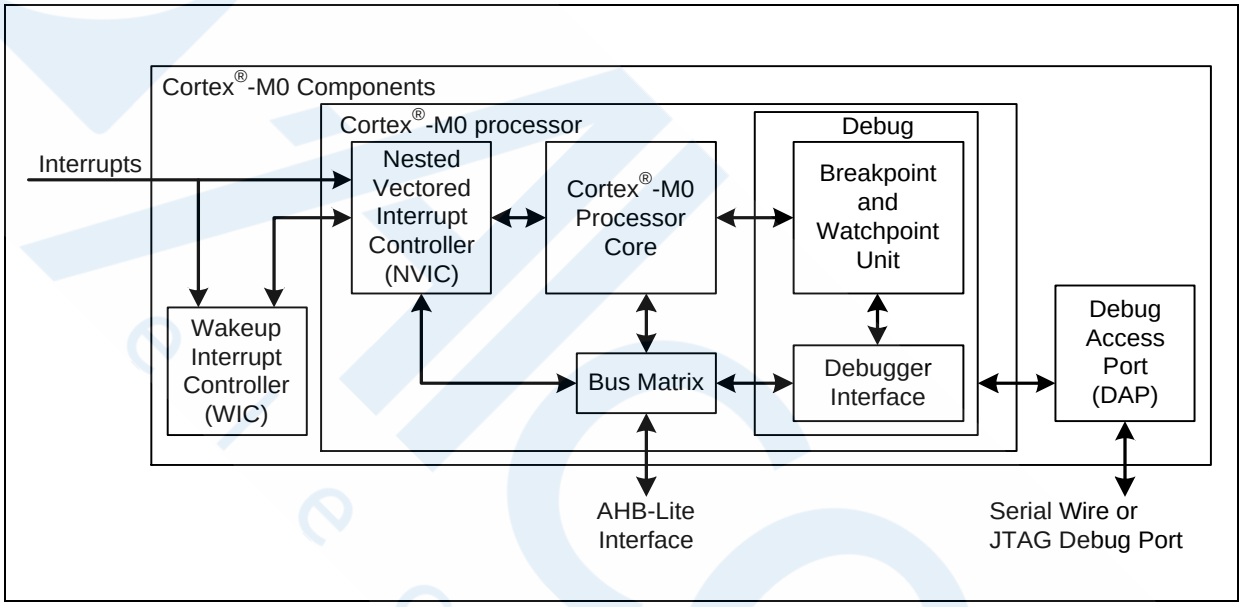


Figure 6.1-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - Armv6-M Thumb® instruction set
  - Thumb-2 technology
  - Armv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 6.2-1 shows the NuMicro® M071M power distribution.

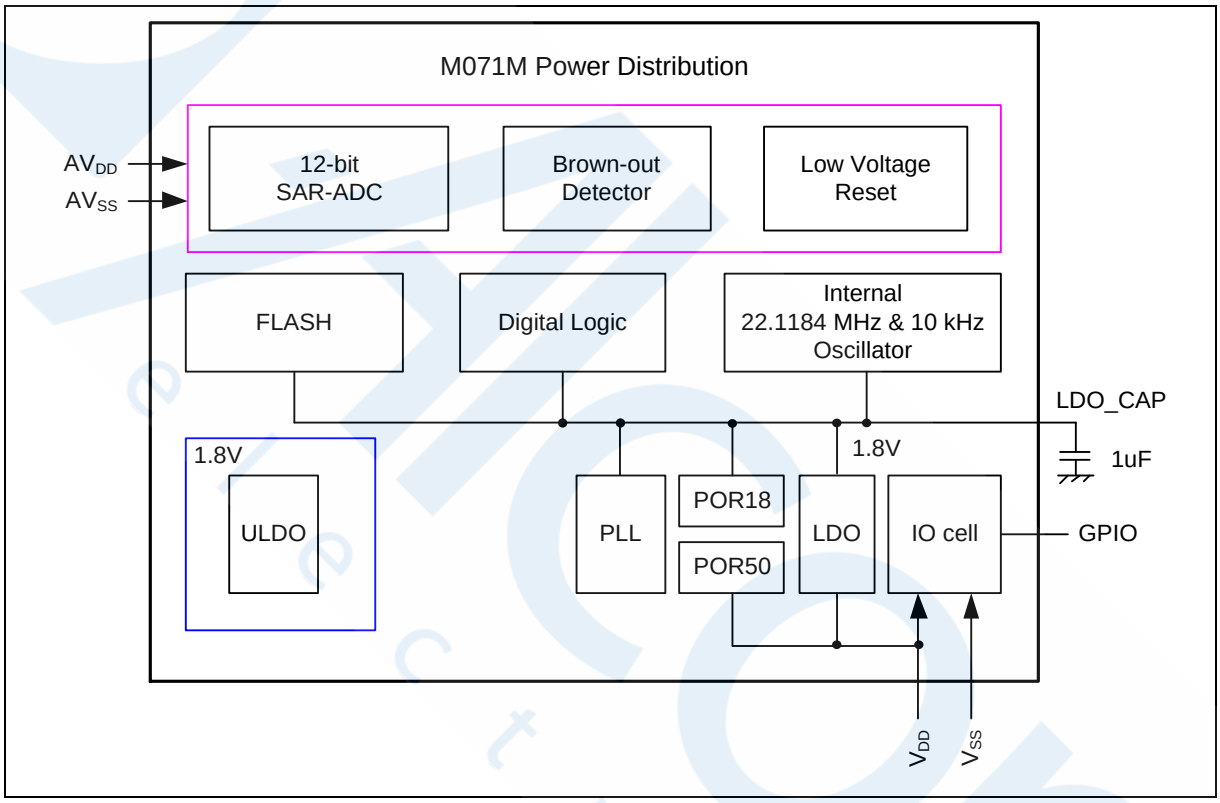


Figure 6.2-1 M071M Power Distribution Diagram

6.2.4 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.2.5 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "Arm® Cortex®-M0 Technical Reference Manual" and "Arm® v6-M Architecture Reference Manual".

6.2.5.1 Exception Model and System Interrupt Map

Table 6.2-1 lists the exception model supported by NuMicro® M071M . Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-1 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description
1 ~ 15	-	-	-	System exceptions
16	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt
17	1	WDT_INT	WDT	Watchdog Timer interrupt
18	-	-	-	Reserved
19	3	EINT1	GPIO	External signal interrupt from PB.15 pin
20	4	GPAB_INT	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDF_INT	GPIO	External interrupt from PC[15:0]/PD[15:0]/PF[8:0]
22	6	-	-	Reserved
23	7	-	-	Reserved
24	8	TMR0_INT	TMR0	Timer 0 interrupt
25	9	TMR1_INT	TMR1	Timer 1 interrupt
26	10	TMR2_INT	TMR2	Timer 2 interrupt
27	11	TMR3_INT	TMR3	Timer 3 interrupt
28	12	UART02_INT	UART0/2	UART0 and UART2 interrupt
29	13	UART1_INT	UART1	UART1 interrupt
30	14	SPI0_INT	SPI0	SPI0 interrupt
31	15	UART3_INT	UART3	UART3 interrupt

32	16	-	-	Reserved
33	17	-	-	Reserved
34	18	I2C0_INT	I2C0	I2C0 interrupt
35	19	-	-	Reserved
36	20	CAN0_INT	CAN0	CAN0 interrupt
37	21	-	-	Reserved
38	22	PWM0_INT	PWM0	PWM0 interrupt
39	23	PWM1_INT	PWM1	PWM1 interrupt
40	24	-	-	Reserved
41	25	-	-	Reserved
42	26	BRAKE0_INT	PWM0	PWM0 brake interrupt
43	27	BRAKE1_INT	PWM1	PWM1 brake interrupt
44	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	ADC_INT	ADC	ADC interrupt
46	30	CKD_INT	CLKC	Clock detection interrupt
47	31	-	-	Reserved

Table 6.2-2 System Interrupt Map

6.2.5.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-3 Vector Table Format

6.2.5.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.6 System Control

The Cortex®-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. Figure 6.3-1 and Figure 6.3-2 show the clock generator and the overview of the clock source control.

The clock generator consists of 5 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT),PLL source can be from 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

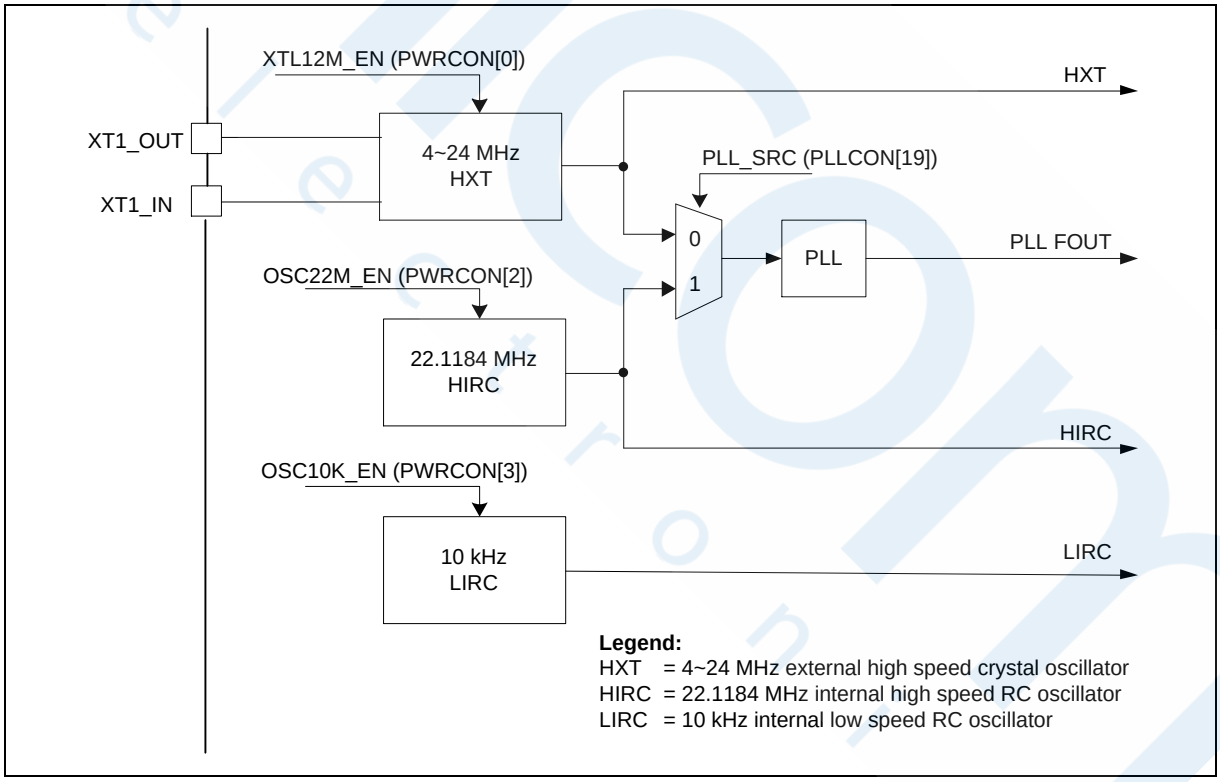


Figure 6.3-1 Clock Generator Block Diagram

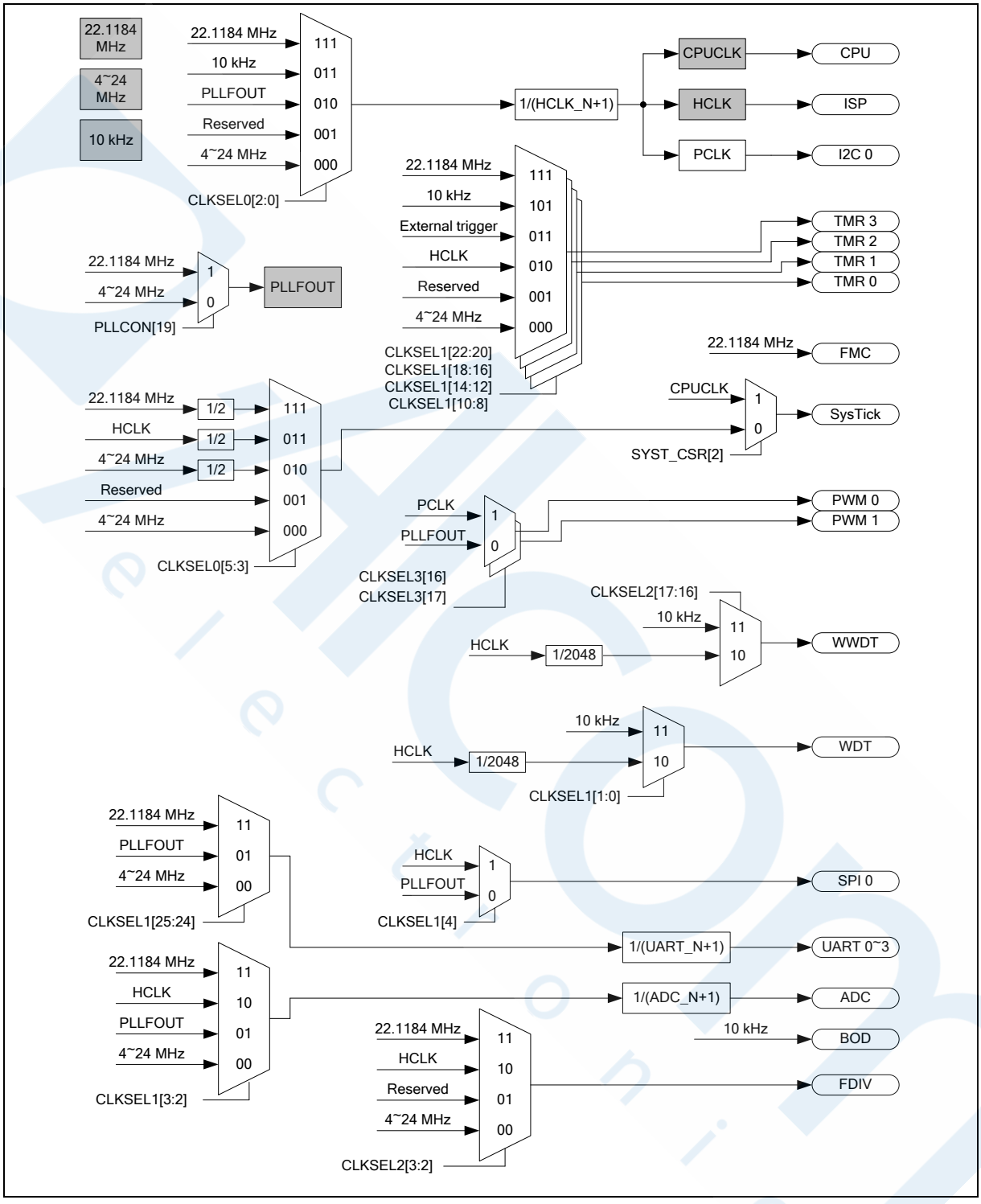


Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

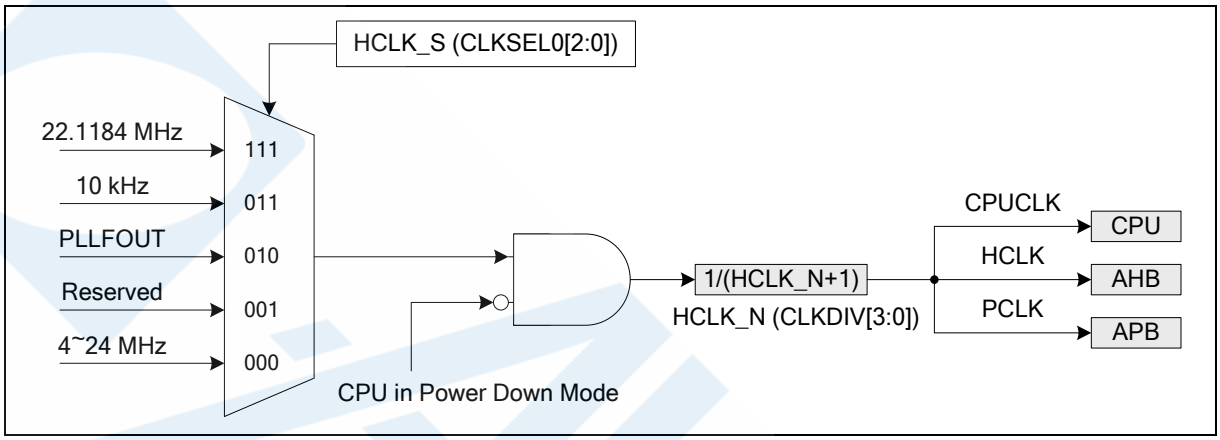


Figure 6.3-3 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

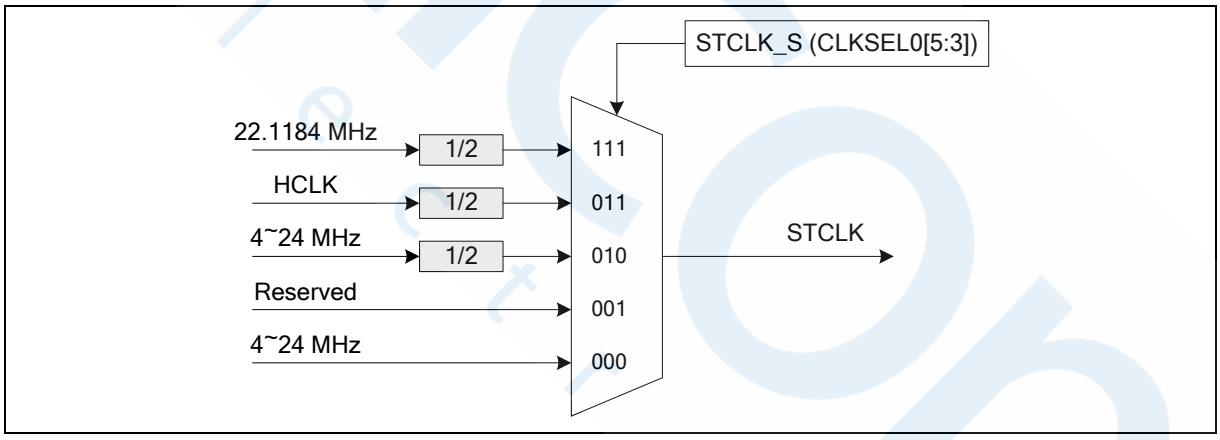


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
- WDT/Timer Peripherals Clock (when 10 kHz intertnal low speed RC oscillator (LIRC) is adopted as clock source)

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

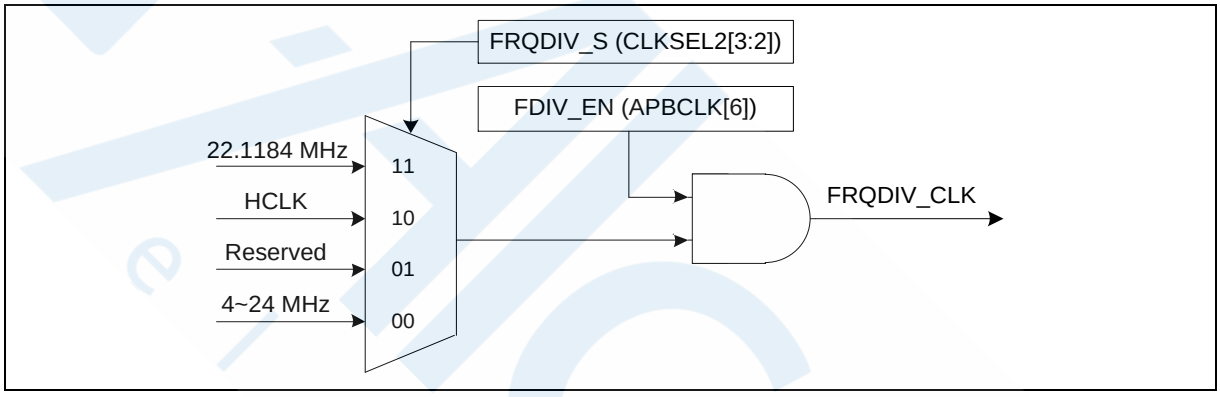


Figure 6.3-5 Clock Source of Frequency Divider

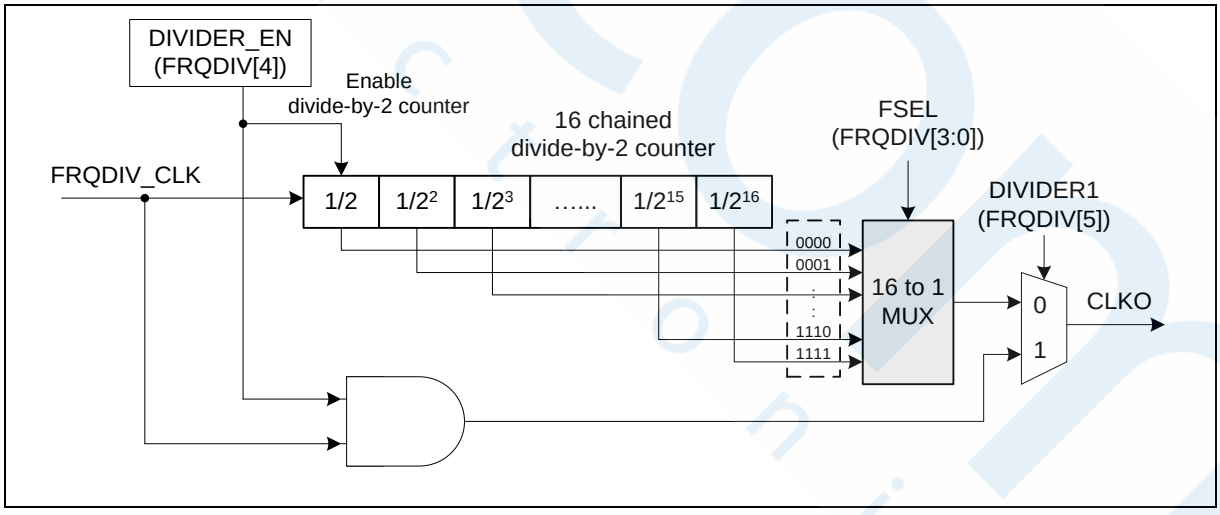


Figure 6.3-6 Frequency Divider Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® M071M has 68 KB on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro® M071M also provides additional Data Flash for user to store some application dependent data.

The NuMicro® M071M supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4 KB and the address is started from 0x0001_F000, and the APROM size is become 68/36 KB. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68/36 KB. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68/36 KB continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded Flash memory supports 512 bytes page erase
- 68/36 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® M071M has up to 42 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 42 pins are arranged in 5 ports named as GPIOA, GPIOB, GPIOC, GPIOD and GPIOF. The GPIOA port has the maximum of 16 pins. The GPIOB port has the maximum of 9 pins. The GPIOC port has the maximum of 6 pins. The GPIOD port has the maximum of 4 pins. The GPIOF port has the maximum of 7 pins. Each of the 42 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function

6.6 Timer Controller (TIMER)

6.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (TM0~TM3)
- Supports external pin capture (TM0_EXT~TM3_EXT) for interval measurement
- Supports external pin capture (TM0_EXT~TM3_EXT) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The M071M provides two PWM generators – PWM0 and PWM. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses the comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, which have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.7.2 Features

6.7.2.1 PWM function features

- Supports maximum clock frequency up to 100 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter match zero, period value or compared value

6.7.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution

- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable it includes (1026, 130, 18 or 3) * WDT_CLK reset delay period.
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (WWDTVAL[5:0]) and 6-bit compare window value (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

6.10 UART Interface Controller (UART)

6.10.1 Overview

The NuMicro® M071M provides up to 4 channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.10.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (uA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin

6.11 I²C Serial Interface Controller (I²C)

6.11.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.11.2 Features

The I²C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports one I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® M071M contains one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. This SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications.

6.12.2 Features

- One set of SPI controller
- Supports Master or Slave mode operation
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports 3-wire, no slave select signal, bi-direction interface

6.13 Analog-to-Digital Converter (ADC)

6.13.1 Overview

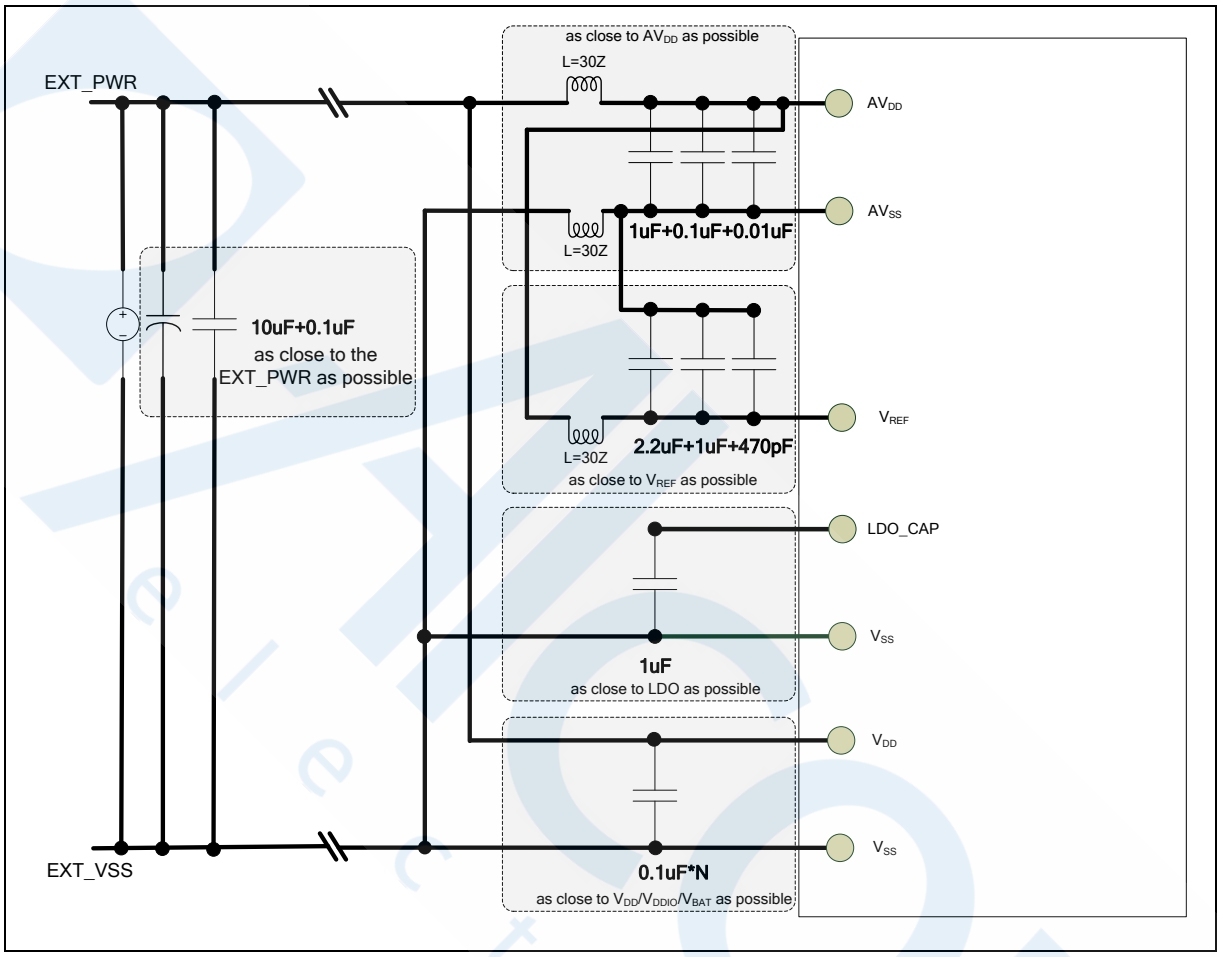
The NuMicro® M071M contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM, BPWM trigger and external STADC pin.

6.13.2 Features

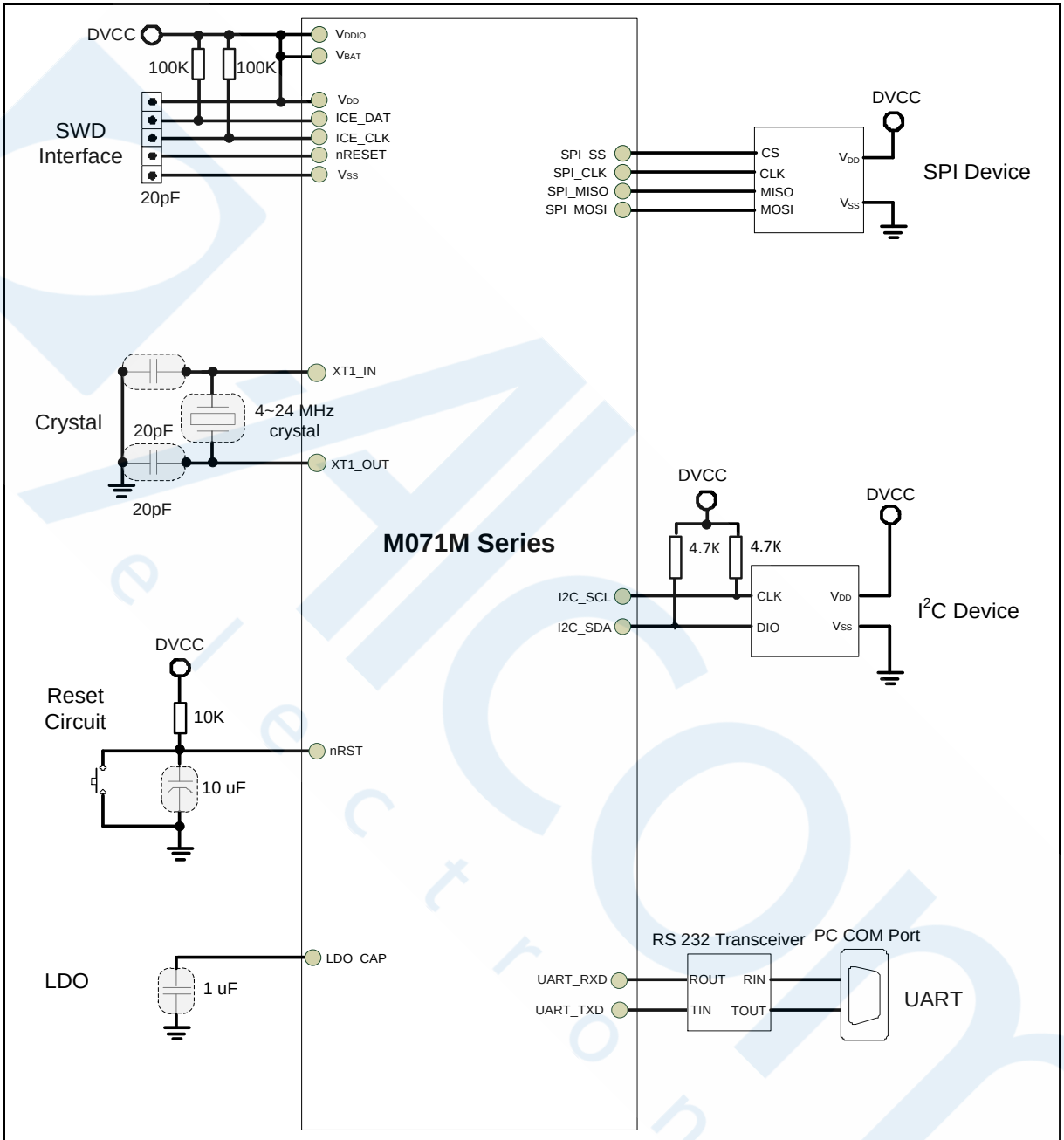
- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 760 KSPS conversion rate (chip working at 5V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11])through software
  - PWM trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Supports two set digital comparators. The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: external analog voltage, and internal Band-gap voltage

7 APPLICATION CIRCUIT

7.1 Power supply scheme



7.2 Peripheral Application scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.

Note 3: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the M071M chip supply voltage must also be 3.3 V

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
VBAT-V_{SS}[*1]	V_{BAT} Power Supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\lvert V_{SS} - AV_{SS} \rvert$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Notes:
1. All main power (V_{DD}, V_{DDIO}, V_{BAT}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	120	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	120	
I_{IO}	Maximum current sunk by a I/O Pin	-	35	
	Maximum current sourced by a I/O Pin	-	35	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:
1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>AV_{DD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 44-pin LQFP(10x10 mm)	-	64.1	-	°C/Watt

Note:
1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	

Symbol	Description	Min	Typ	Max	Unit
LU[*3]	Pin current for latch-up[*3]	-200	-	+200	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
44-pin QFN(10x10 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

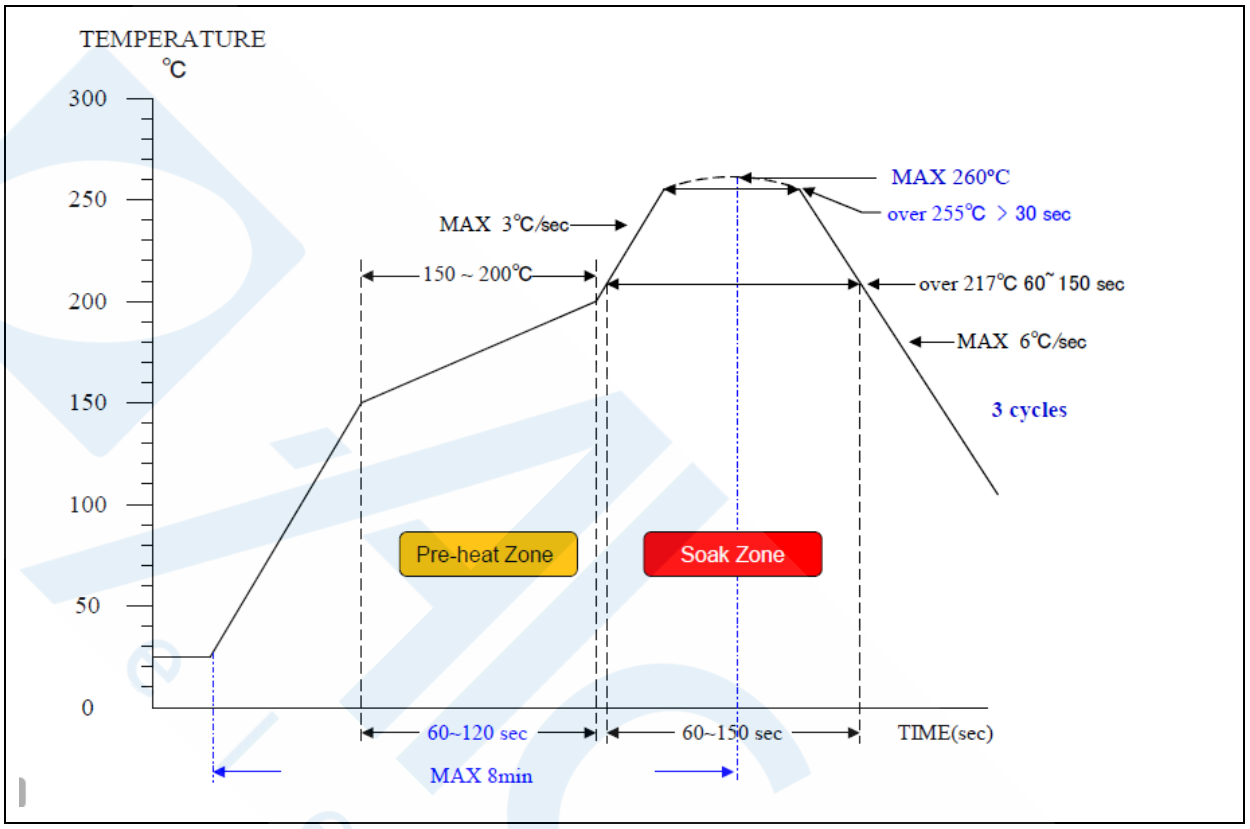


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	2.5	-	5.5	V	
V_{BAT}	V_{BAT} Operation voltage	2.5	-	5.5		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	2.5	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.16	1.2	1.24	mV	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (TA), and the typical values for TA= 25 °C and V_{DD} = 2.5 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock, fPCLK0, 1 = fHCLK.
- Program run while(1) code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]	Max[*1][*2]	Unit
			T_A = 25 °C	T_A = 25 °C	TA = 105 °C	
I_{DD_RUN}	Normal run mode with, executed from Flash, all peripherals disable	50 MHz	10	13	14.5	mA
		22.1184 MHz	3.7	4.1	5.1	
		12 MHz	2.5	4.6	5.6	
		4 MHz	1.2	3.1	4.1	
		10 kHz	0.101	0.185	1.2	
	Normal run mode with, executed from Flash, all peripherals enable	50 MHz	16.5	21	22.5	
		22.1184 MHz	7.9	9.2	10.2	
		12 MHz	4.1	6.5	7.5	
		4 MHz	1.8	3.6	4.6	
		10 kHz	0.102	0.19	1.2	

Notes:

1. When analog peripheral blocks such as ADC, PLL, HIRC, LIRC and HXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]	Max[*1][*2]	Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode with PL0, all peripherals disable	50 MHz	5.8	8.3	9.8	mA
		22.1184 MHz	1.8	2.1	3.1	
		12 MHz	1.5	3.45	3.45	
		4 MHz	0.9	2.6	3.6	
		10 kHz	0.1	0.18	1.2	

	Idle mode with PL0, all peripherals enable	50 MHz	12.56	16	17.5	
		22.1184 MHz	5.77	6.7	7.7	
		12 MHz	3.11	5.3	6.3	
		4 MHz	1.41	3.2	4.2	
		10 kHz	0.101	0.185	1.2	

Notes:

1. When analog peripheral blocks such as ADC, PLL, HIRC, LIRC and HXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	Typ[*1]	Max[*2][*3]	Max[*2][*3]	Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	10	53	1000	µA

Notes:

1. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. When analog peripheral blocks such as ADC are ON, an additional power consumption should be considered.

Table 8.3-3 Chip Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 5.5 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 22.1184 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PWM0	0.555	mA
PWM1	0.558	
ADC[*2]	0.139	
WDT/WWDT	0.070	
SPI0	0.277	
UART0	0.527	
UART1	0.539	

UART2	0.522	
UART3	0.374	
I2C0	0.050	
TMR0	0.52	
TMR2	0.53	
TMR3	0.51	

Notes:
1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 Low-power mode wakeup timings is measured on a wakeup phase with a 22.1184 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_DPD}[*1][*2]	Wakeup from deep Power-down mode	23	-	µS

Notes:
1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative Injection	Positive Injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PA0~PA7 and PF0~PF1 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.6		V_{DD} = 2.5 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.0 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 5 V, Open-drain or input only mode on any other 5v tolerance pins

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O input characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-250	-400		µA	V_{DD} = V_{BAT} = 4.5V V_{IN} = 2.4V
		-50	-80		µA	V_{DD} = V_{BAT} = 2.7V V_{IN} = 2.2V
		-40	-73		µA	V_{DD} = V_{BAT} = 2.5V V_{IN} = 2.0V
	Source current for push-pull mode and high level	-15	-27		mA	V_{DD} = V_{BAT} = 4.5V V_{IN} = 2.4V
		-3	-5.5		mA	V_{DD} = V_{BAT} = 2.7V V_{IN} = 2.2V
		-2.5	-5		mA	V_{DD} = V_{BAT} = 2.5V V_{IN} = 2.0V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	8	15		mA	V_{DD} = V_{BAT} = 4.5V V_{IN} = 0.45V
		5	9.5		mA	V_{DD} = V_{BAT} = 2.7V V_{IN} = 0.45V

		4	9		mA	V_{DD} = V_{BAT} = 2.5V V_{IN} = 0.45V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Notes:
1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O output characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	0	-	0.2*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	V_{DD}	V	
R_{RST}[*1]	Internal nRESET pull up resistor	-	45	-	kΩ	
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	µS	Normal run and Idle mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 22.1184 MHz Internal Median Speed RC Oscillator (HIRC)

The 22.1184 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
F_{HRC}	Oscillator frequnecy	-	22.1184	-	MHz	T_A = 25 °C, V_{DD} = 5V
	Frequency drift over temperarure and volatge	-1	-	+1	%	T_A = 25 °C, V_{DD} = 5V
		-2	-	+2	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{MRC}[*1]	Operating current	-	1200	-	μA	
T_S[*1]	Stable time	-	-	20	μS	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V

Notes:
1. Guaranteed by characterization result, not tested in production.

Table 8.4-1 22.1184 MHz Internal Median Speed RC Oscillator(MIRC) characteristics

8.4.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{LRC} [*2]	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} =2.5V~5V
		-50	-	50	%	T_A=-40~105°C V_{DD}=2.5V~5.5V Without software calibration
I_{LRC}	Operating current	-	1	-	μA	V_{DD} = 2.5V~5.5V
T_S	Stable time	100	-	200	μS	T_A=-40~105°C V_{DD}=2.5V~5.5V

Notes:
1. Guaranteed by characterization, not tested in production.
2. The 10 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-2 10 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

8.4.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	1.9	-	µA	4 MHz, V_{DD} = 5.5V
		-	0.63	-		4 MHz, V_{DD} = 3.3V
		-	2.4	-		12 MHz, V_{DD} = 5.5V
		-	0.93	-		12 Mhz, V_{DD} = 3.3V
		-	3.27	-		24 MHz, V_{DD} = 5.5V
		-	1.31	-		24 MHz, V_{DD} = 3.3V
T_S	Stable time	-	1900	-	µS	4 MHz, CL = 12.5 pF
		-	560	-		12 MHz, CL = 12.5 pF
		-	350	-		24 MHz, CL = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	

Notes:

1. Guaranteed by characterization, not tested in production.

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

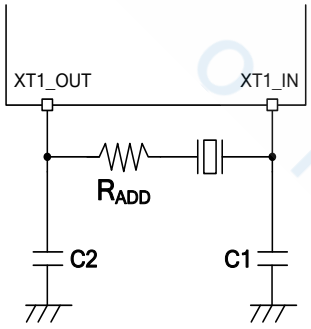


Table 8.4-3 External 4~24 MHz High Speed Crystal(HXT) Characteristics

8.4.3.1 *Typical Crystal Application Circuits*

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

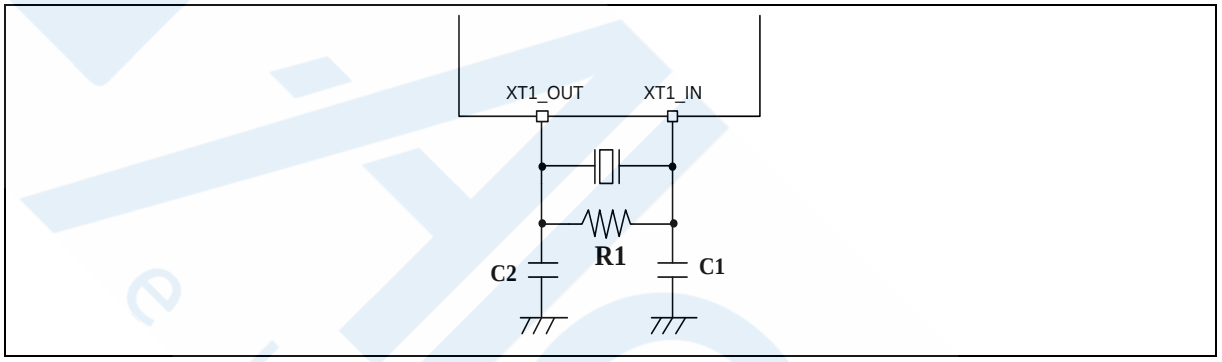


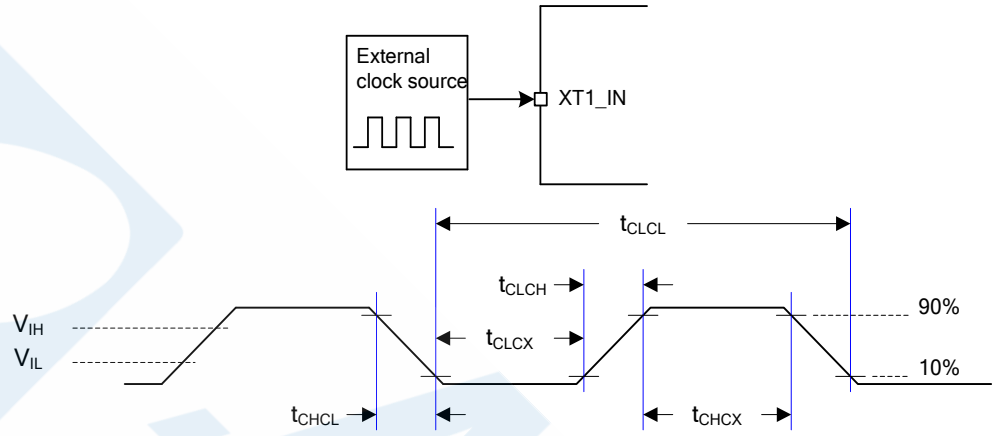
Figure 8.4-1 Typical Crystal Application Circuit

8.4.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	10	-	-	nS	
t_{CLCX}	Clock low time	10	-	-	nS	
t_{CLCH}	Clock rise time	2	-	15	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	2	-	15	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-4 External 4~24 MHz High Speed Clock Input Signal

8.4.5 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	16	-	100	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	64	-	100	MHz	
T_L	PLL locking time	-	-	100	µS	
Jitter[*2]	Cycle-to-cycle Jitter	-	-	500	pS	
I_{DD}	Power consumption	-	1	2	mA	V_{DD}=5.5V @ f_{PLL_VCO} = 100 MHz

Notes:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-5 PLL characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	2.5	-	5.5	V	
V_{LDO}	Output voltage	1.62	1.8	1.98	V	
T_A	Temperature	-40	-	105	°C	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{LVR}[*1]	LVR operating current	-	-	1.65	μA	AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-		150		AV_{DD} = 5.5V, Normal mode
V_{POR}	POR reset voltage	1.30	-	2.46	V	
V_{LVR}	LVR reset voltage	1.5	-	2.4		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	4.3	4.4	4.5		BOD_VL[1:0]=11
		3.6	3.7	3.8		BOD_VL [1:0]=10
		2.6	2.7	2.7		BOD_VL [1:0]=01
		2.1	2.2	2.3		BOD_VL [1:0]=00
	BOD brown-out detect voltage (Rising edge)	4.32	4.42	4.52		BOD_VL[1:0]=11
		3.62	3.72	3.82		BOD_VL [1:0]=10
		2.62	2.72	2.72		BOD_VL [1:0]=01
		2.12	2.22	2.32		BOD_VL [1:0]=00
T_{LVR_SU}[*1]	LVR startup time	-	-	300	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	-	240		-
T_{BOD_SU}[*1]	BOD startup time	-	-	1100		-
T_{BOD_RE}[*1]	BOD respond time	-	-	150		Normal mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

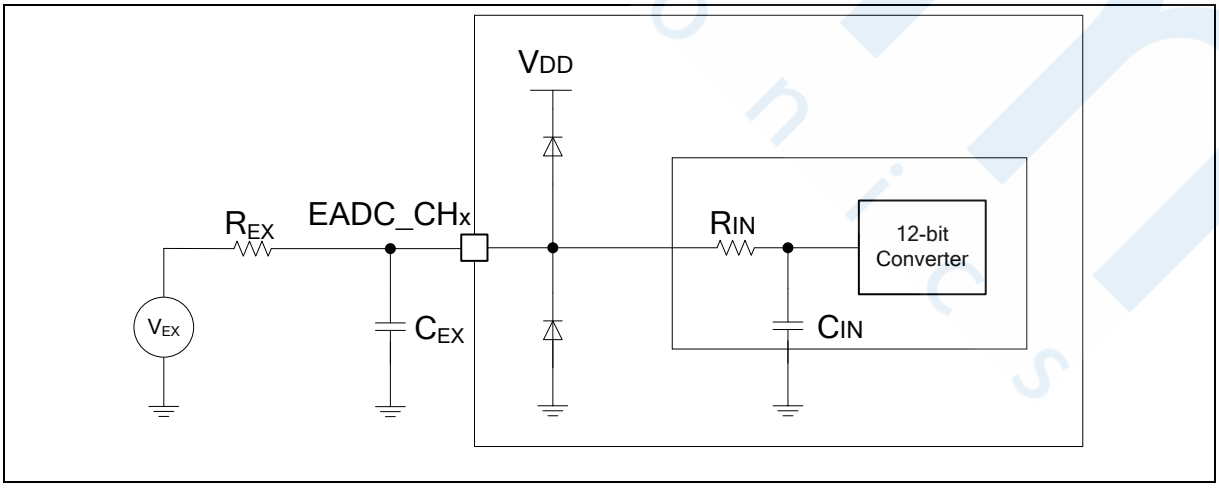
8.5.3 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	2.5	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.5	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	3	-	mA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{SPS} = 1MSPS
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	-	-	21	MHz	
F_{SPS}[*1]	Sampling Rate	-	-	1000	KSPS	
INL[*1]	Integral Non-Linearity Error	-	±2	±4	LSB	$V_{REF} = AV_{DD}$,
DNL[*1]	Differential Non-Linearity Error	-	-1~2	-1~4	LSB	$V_{REF} = AV_{DD}$,
E_G[*1]	Gain error	-	-3	-	LSB	$V_{REF} = AV_{DD}$,
E_O[*1]$_T$	Offset error	-	3	-	LSB	$V_{REF} = AV_{DD}$,
E_A[*1]	Absolute Error	-	4	-	LSB	$V_{REF} = AV_{DD}$,
C_{IN}[*1]	Internal Capacitance	-	6	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	6.5	-	kΩ	

Notes:

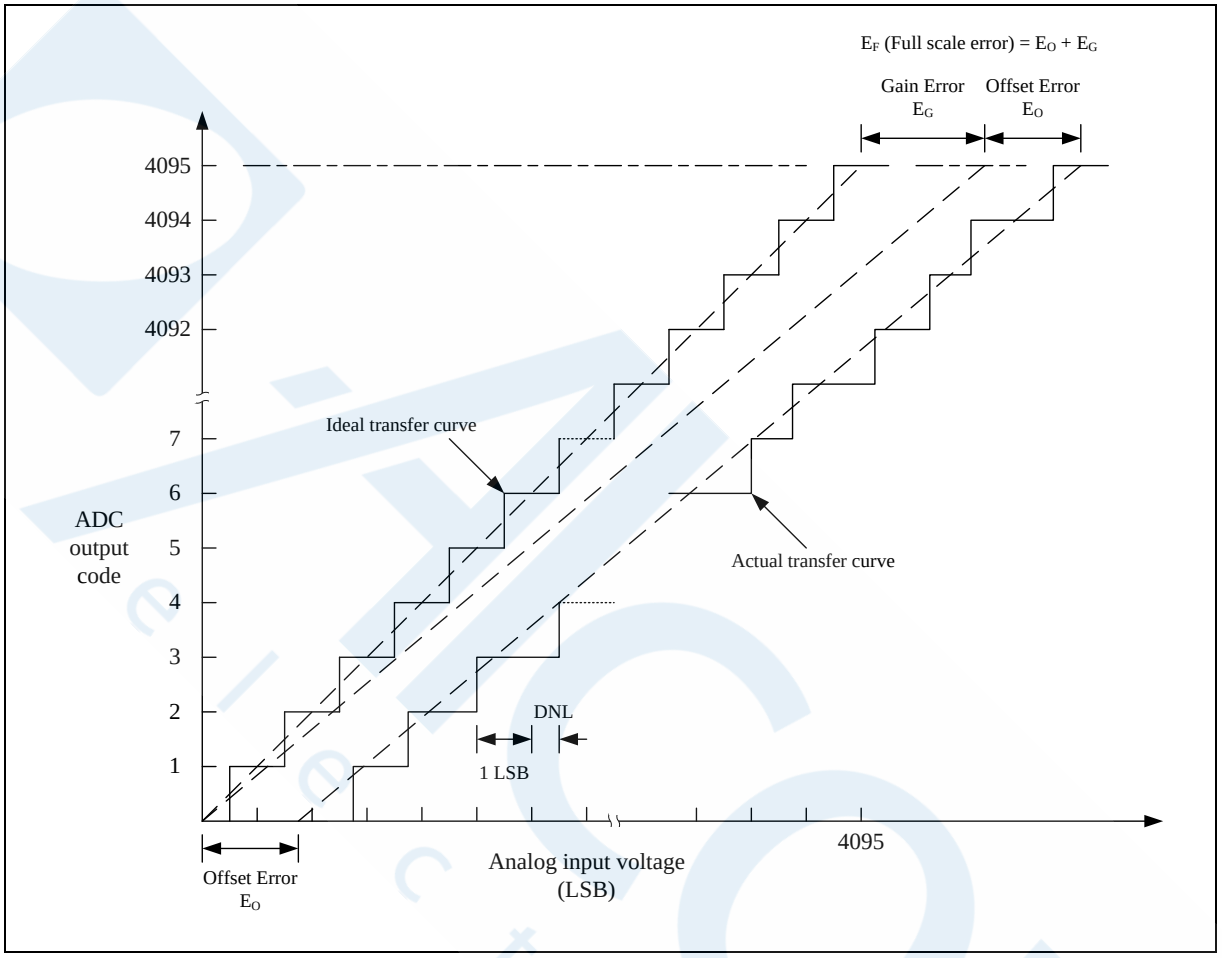
1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins

should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.

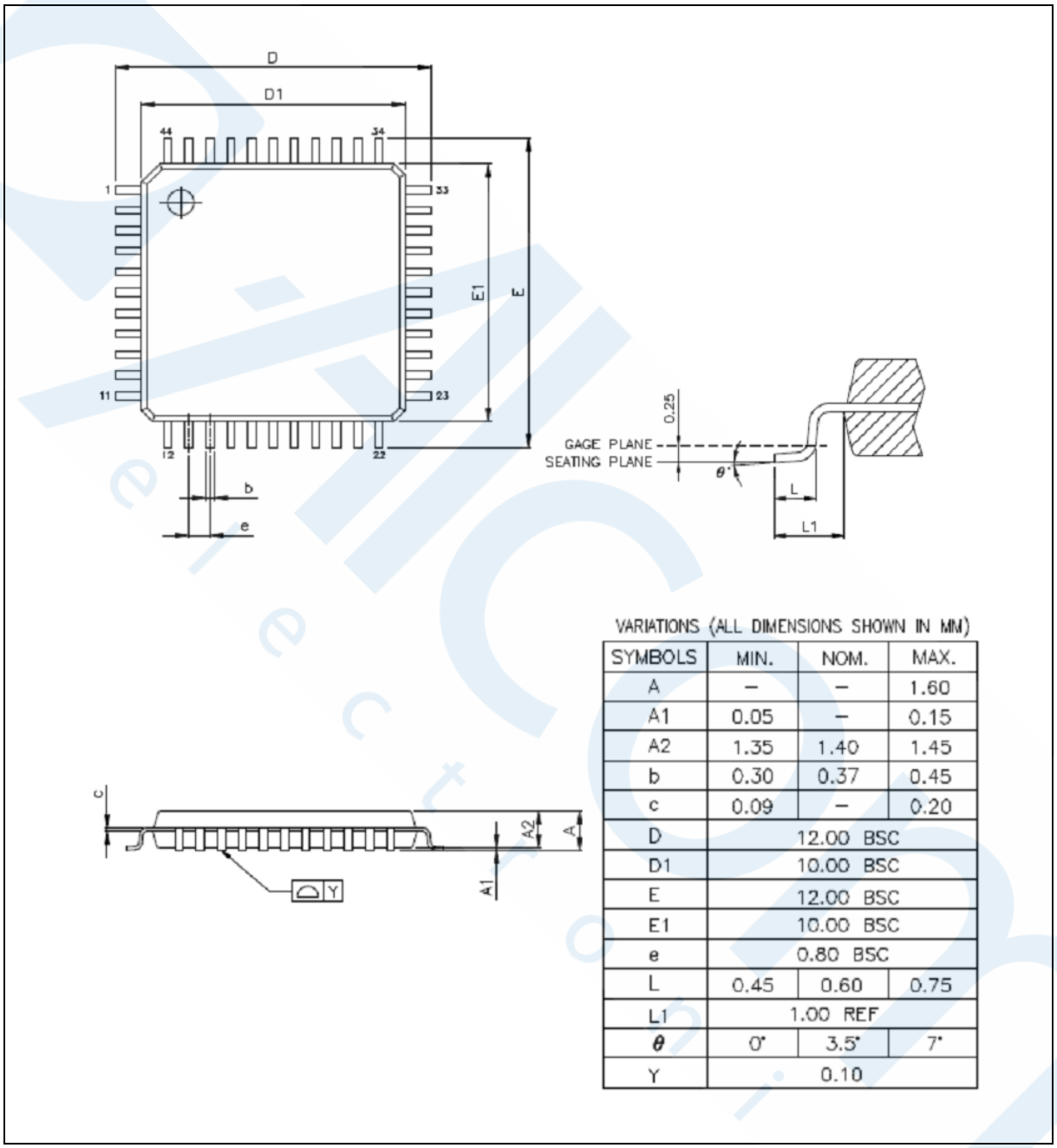


Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

9.1 44-pin LQFP (10x10x1.4 mm footprint 0.8 mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	–	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
Y	0.10		

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

11 REVISION HISTORY

Date	Revision	Description
2020.08.11	1.00	• Initial version.
2022.11.24	1.01	• Added Package Type table in section 3.1. • Added Selection guide in section 3.2. • Added Naming Rule table in section 3.3. • Added “Package is Halogen-free, RoHS-compliant and TSCA-compliant.” in chapter 3 and 9 . • Moved Abbreviations to chapter 10.
2022.12.21	1.02	• Modified general description in chapter 1 • Modified the package type table in section 3.1. • Modified M071M selection guide table in section 3.2. • Modified the M071M naming rule table in section 3.3. • Modified the M071M multi-function pin diagram in section 4.1. • Modified the M071M block diagram in section 5.1.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.