MPM3650

2.75V to 17V, 6A, 1.2MHz, Synchronous, Ultra-Thin Power Module

DESCRIPTION

The MPM3650 is a fully integrated high-frequency, synchronous, rectified, step-down power module with an internal inductor. It offers a very compact solution to achieve 6A of continuous output current over a wide input range, with excellent load and line regulation. The MPM3650 offer synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MPM3650 requires a minimal number of readily available, standard external components. It is available in a space-saving QFN-24 (4mmx6mm) package.

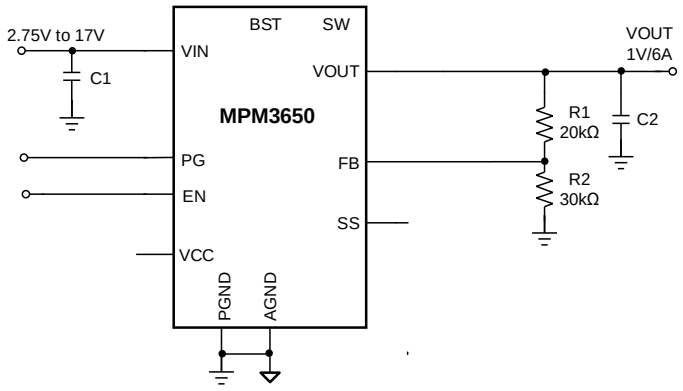
FEATURES

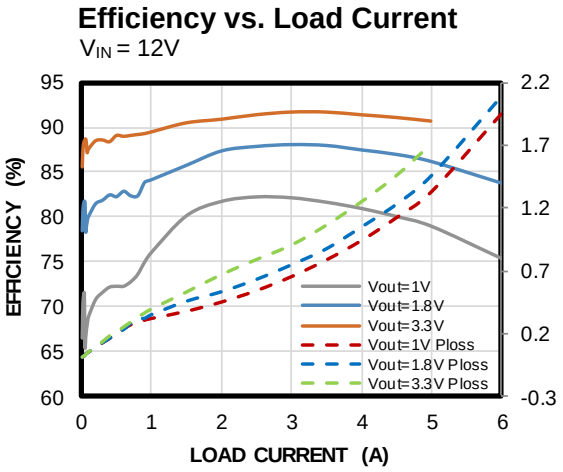
- Wide 2.75V to 17V Operating Input Range
- Output Current:
  - 0.6V to 1.8V, 6A Output
  - Above 1.8V, 5A Output
- Internal Power MOSFETs
- Output Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- High Efficiency with DCM at Light-Load
- Supports Pre-Biased Start-Up
- Fixed 1200kHz Switching Frequency
- External Programmable Soft-Start Time
- EN and Power Good for Power Sequencing
- Over-Current Protection and Hiccup Mode
- Thermal Shutdown
- Available in a QFN-24 (4mmx6mmx1.6mm) Package

APPLICATIONS

- FPGA Power Systems
- Optical Modules
- Telecom
- Networking
- Industrial Equipment

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3650GQW	QFN-24 (4mmx6mmx1.6mm)	*See Below*	3

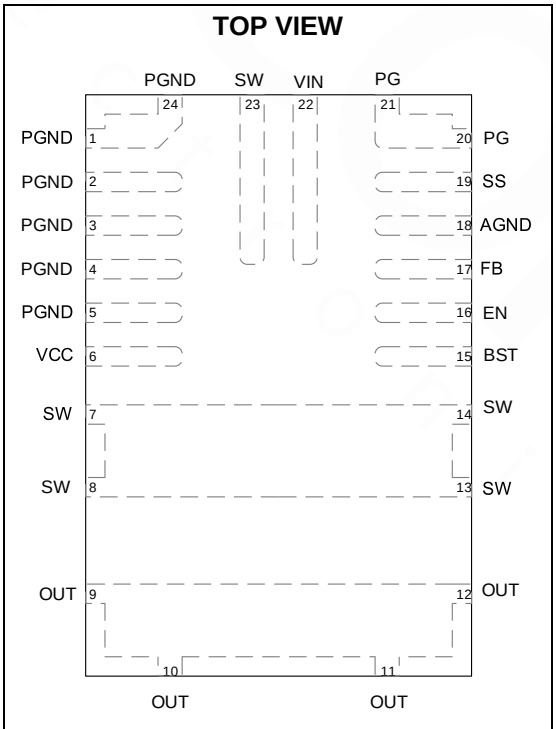
* For Tape & Reel, add suffix –Z (e.g. MPM3650GQW–Z).

TOP MARKING

MPSYWW
MP3650
LLLLLL
M

MPS: MPS prefix
Y: Year code
WW: Week code
MP3650: First six digits of the part number
LLLLLL: Lot number
M: Module

PACKAGE REFERENCE



QFN-24 (4mmx6mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4, 5, 24	PGND	**System ground.** This pin is the reference ground of the regulated output voltage. Because of this, extra care must be taken when designing the PCB layout. It is recommended to connect this pin to GND with copper pours and vias.
6	VCC	**Internal bias supply output.**
7, 8, 13, 14, 23	SW	**Switch output.** Float the SW pins.
9, 10, 11, 12	OUT	**Output pin.** Connect OUT to the output capacitor (C_{OUT}).
15	BST	**Bootstrap.** Float the BST pin.
16	EN	**Enable.** Pull the EN pin high to enable the part. When EN is floating, the device is disabled. EN is pulled down to GND by an internal 3.3MΩ resistor.
17	FB	**Feedback.** Sets the output voltage when connected to the tap of an external resistor divider that is placed between output and GND.
18	AGND	**Signal ground.** AGND is not internally connected to the system ground, so ensure that AGND is connected to the system ground in the PCB layout.
19	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time and avoid start-up inrush current. This pin includes an internal 22nF SS capacitor.
20, 21	PG	**Power good output.** The output of the PG pin is an open-drain output. The PG pin changes its state if under-voltage protection (UVP), over-current protection (OCP), over-temperature protection (OTP), or an over-voltage (OV) condition occurs.
22	VIN	**Supply voltage.** The part operates from a 2.75V to 17V input rail. Use a 0402 size, 0.1µF input capacitor to decouple the input rail. Use wide PCB traces to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +20V
V_{SW}..... - 0.3V (-5V < 10ns) to V_{IN} + 0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) 3.816W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +125°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM).....2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.75V to 17V
Output voltage (V_{OUT})……..0.6V to V_{IN} x D_{MAX} or 12V maximum (4)
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVM3650-QW-00A (5)…...32.75….10.217..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation on the EVM3650-QW-00A evaluation board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Operation voltage after V_{OUT} is regulated to a 0.6V or higher voltage.
5) Measured on EVM3650-QW-00A, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.75		17	V
Supply Current						
Shutdown supply current	I_{IN}	V_{EN} = 0V		2	5	µA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 7V			5	µA
Current Limit						
Valley current limit	I_{LIMIT_VY}		6	7		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		0.9	1.2	1.6	MHz
Minimum on time (7)	t_{ON_MIN}			50		ns
Minimum off time (7)	t_{OFF_MIN}			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	µA
Enable and UVLO						
EN rising threshold	V_{EN_RISING}		1.19	1.23	1.27	V
EN falling threshold	$V_{EN\_FALLING}$		0.96	1	1.04	V
EN pin pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout rising threshold	VCC_{VTH}		2.4	2.5	2.6	V
VCC under-voltage lockout threshold	VCC_{HYS}			200		mV
VCC regulator	V_{CC}	V_{IN} = 5V		3.5		V
VCC load regulation	REG_{VCC}	I_{CC} = 5mA		3		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{VTH\_HI}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{VTH\_LO}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{VTH\_HI}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{VTH\_LO}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{TD}	Both edges		50		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

Notes:

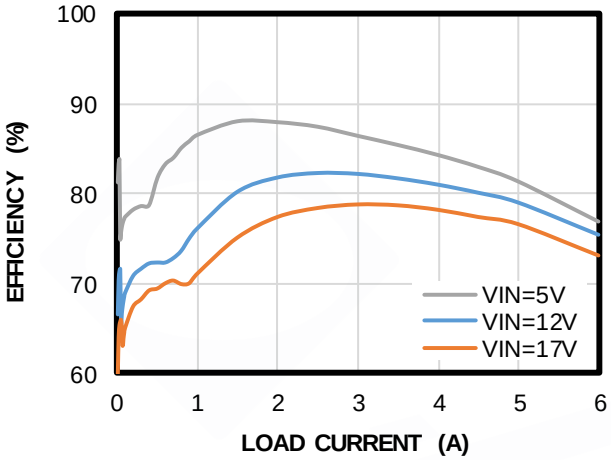
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by design and characterization tests.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

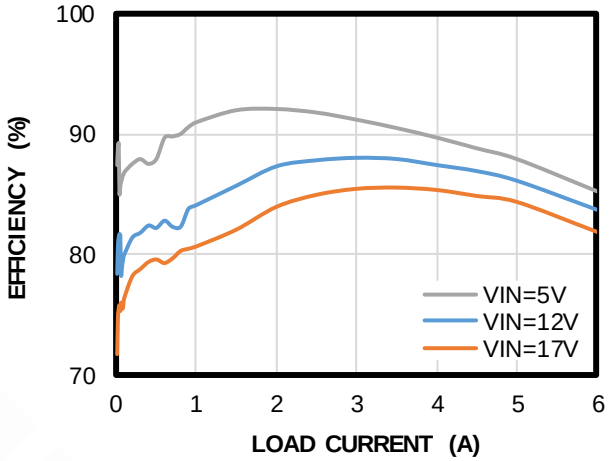
Efficiency vs. Load Current

V_{OUT} = 1V



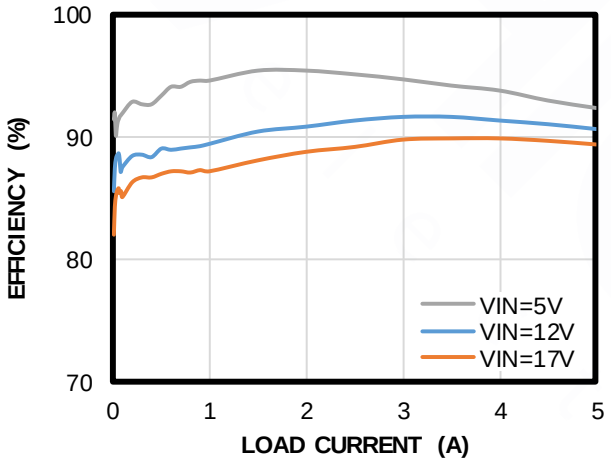
Efficiency vs. Load Current

V_{OUT} = 1.8V



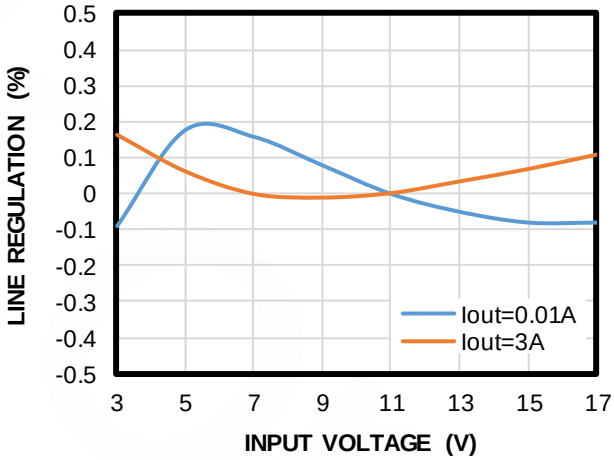
Efficiency vs. Load Current

V_{OUT} = 3.3V



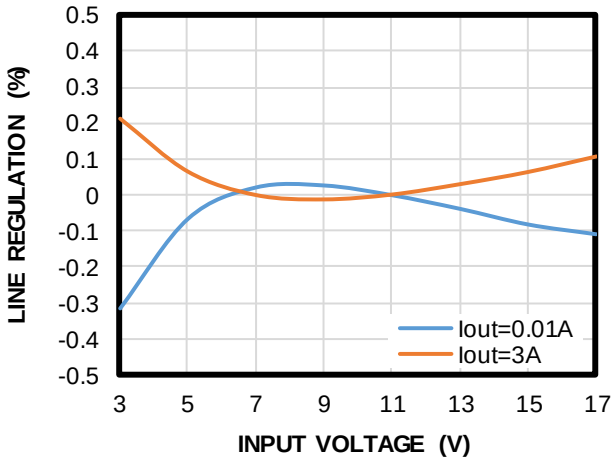
Line Regulation

V_{OUT} = 1V



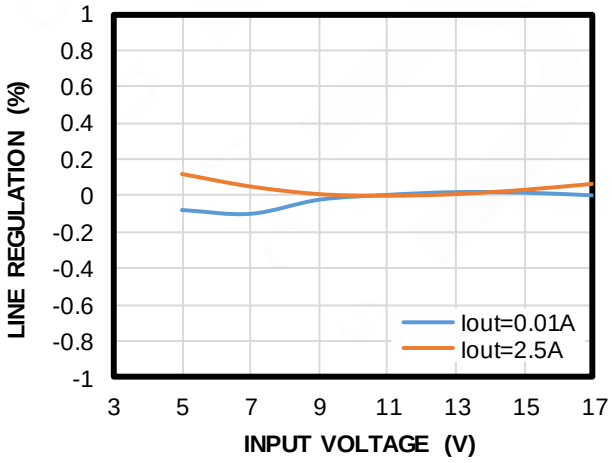
Line Regulation

V_{OUT} = 1.8V



Line Regulation

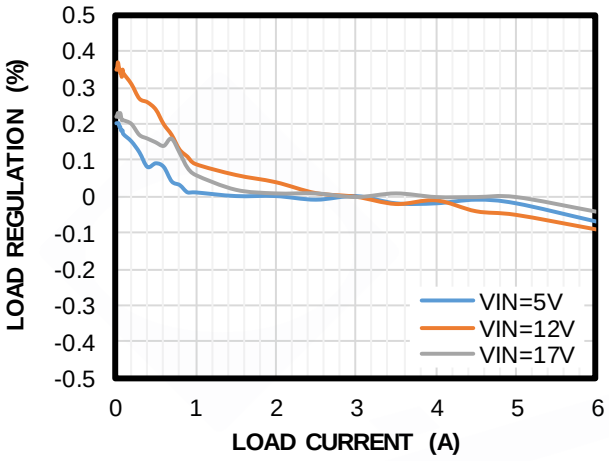
V_{OUT} = 3.3V



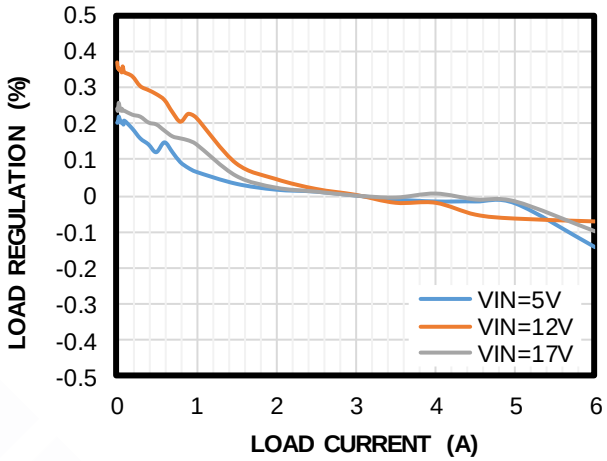
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

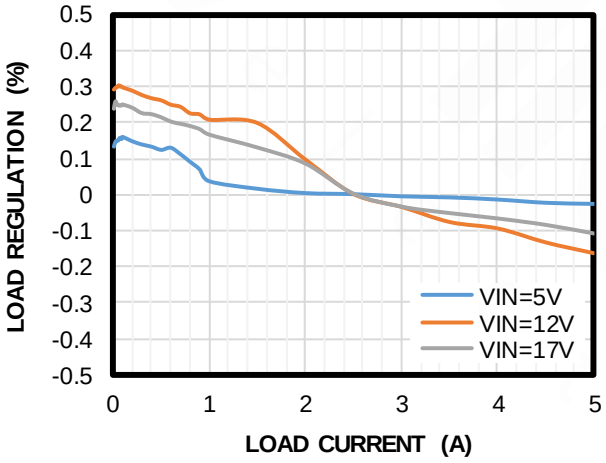
Load Regulation
V_{OUT} = 1V



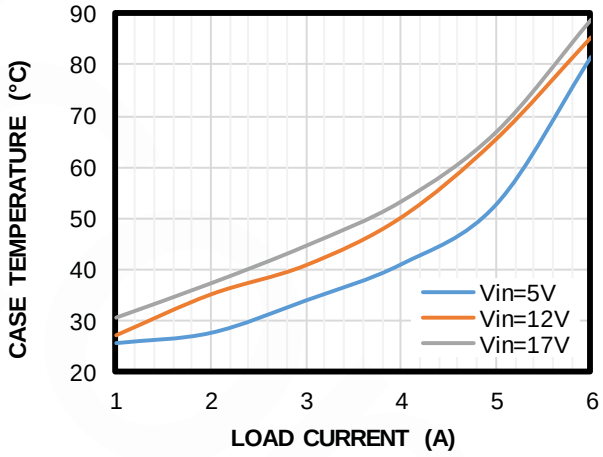
Load Regulation
V_{OUT} = 1.8V



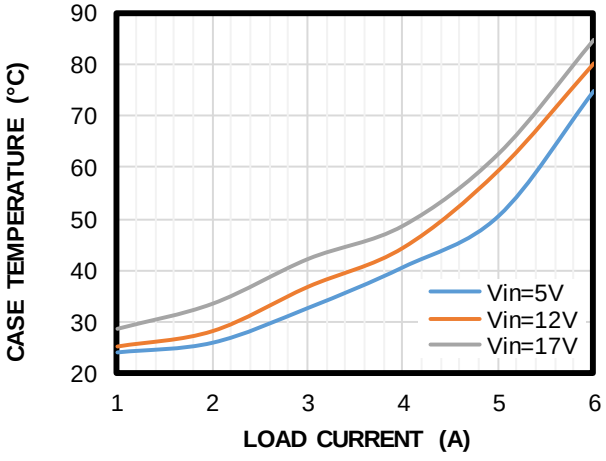
Load Regulation
V_{OUT} = 3.3V



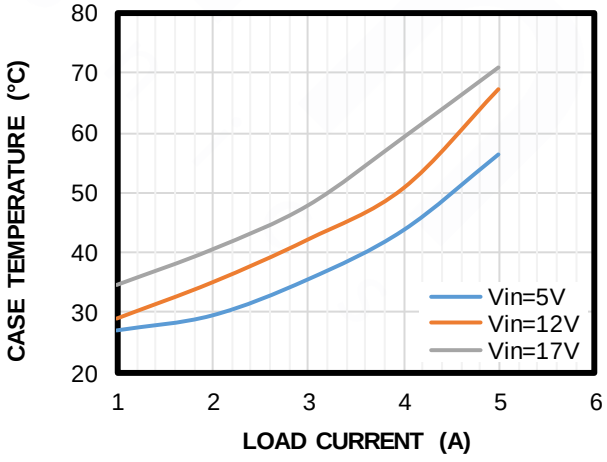
Temperature vs. I_{OUT}
V_{OUT} = 1.8V



Temperature vs. I_{OUT}
V_{OUT} = 1V, T_A = 15°C



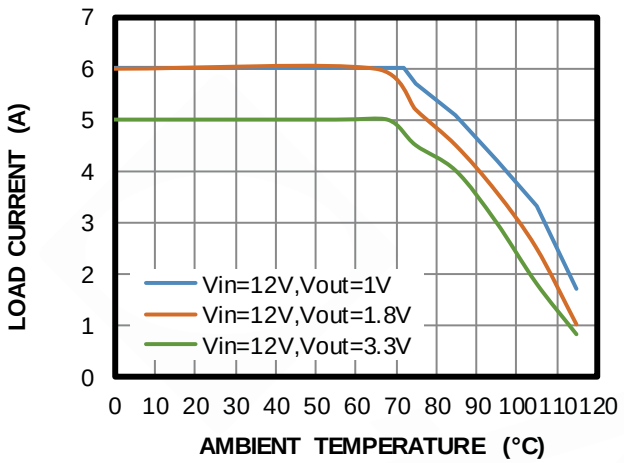
Temperature vs. I_{OUT}
V_{OUT} = 3.3V



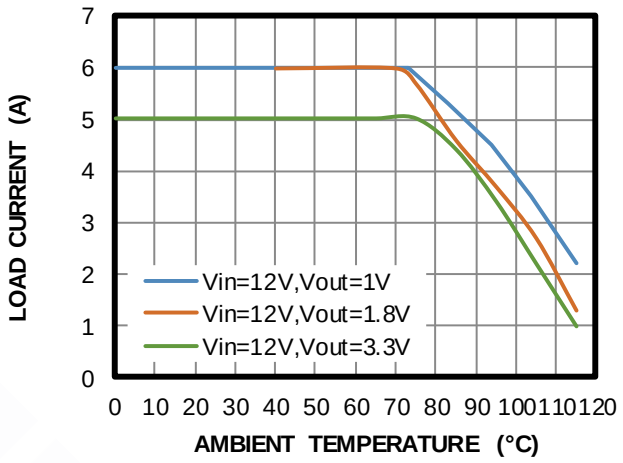
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

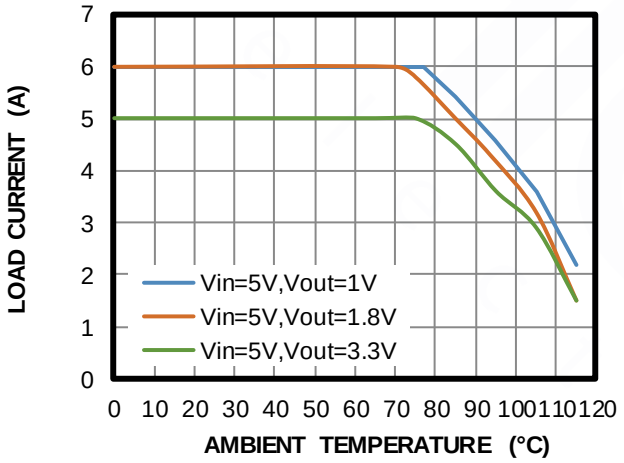
Thermal Derating
V_{IN} = 12V without airflow



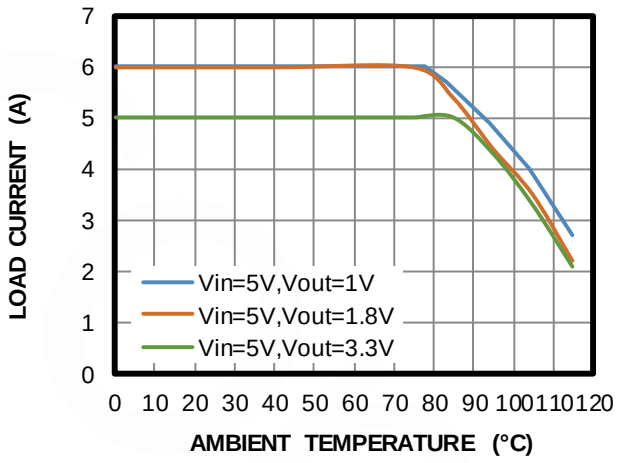
Thermal Derating
V_{IN} = 12V with airflow



Thermal Derating
V_{IN} = 5V without airflow



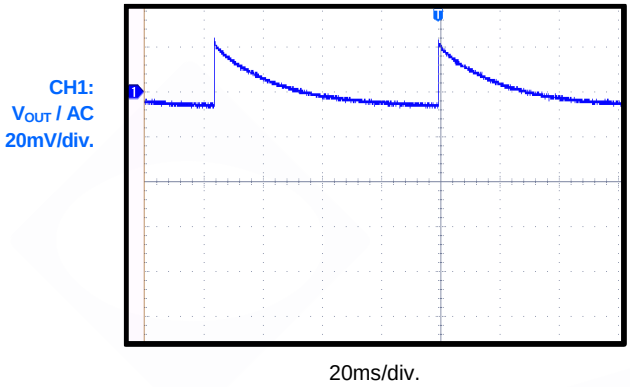
Thermal Derating
V_{IN} = 5V with airflow



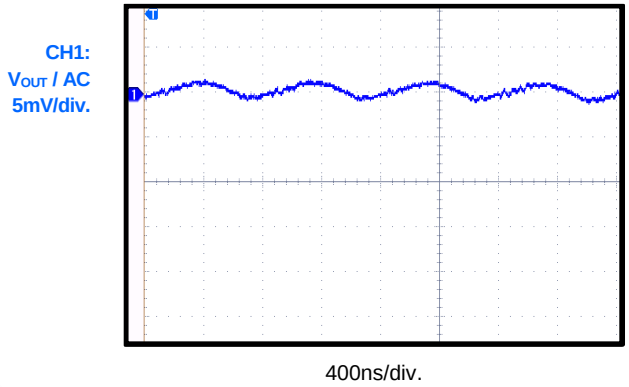
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

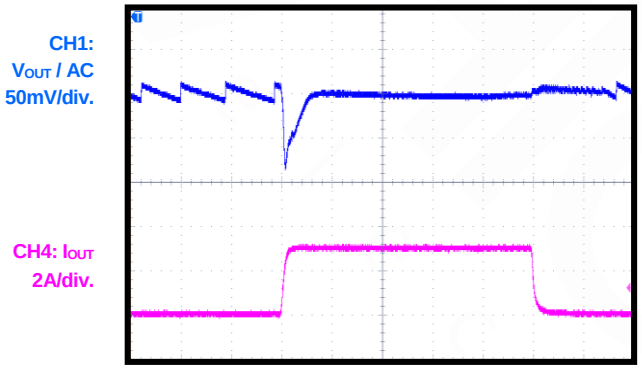
V_{OUT} Ripple
I_{OUT} = 0A



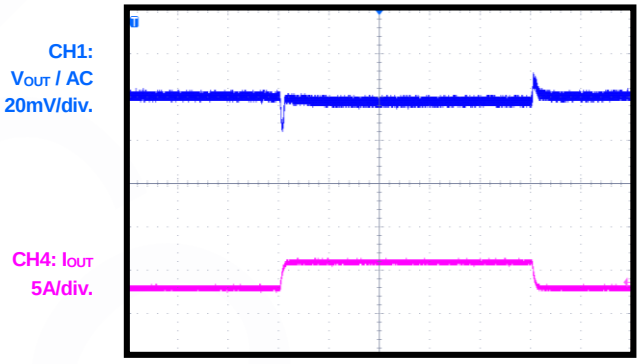
V_{OUT} Ripple
I_{OUT} = 6A



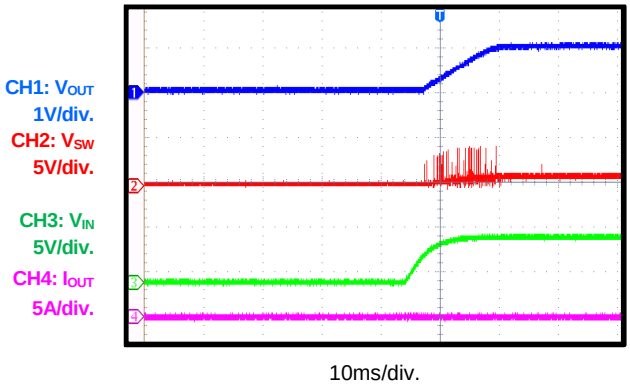
Load Transient
I_{OUT} = 0A to 3A



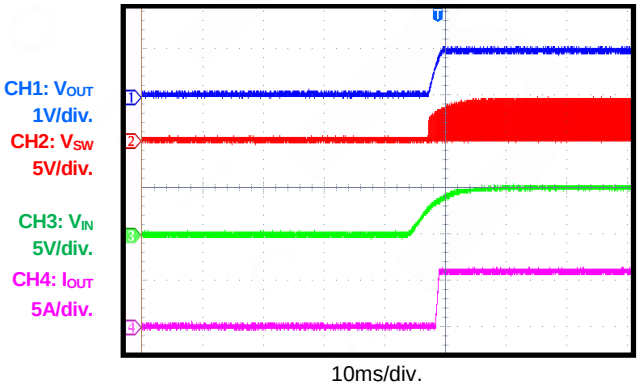
Load Transient
I_{OUT} = 3A to 6A



VIN On
I_{OUT} = 0A



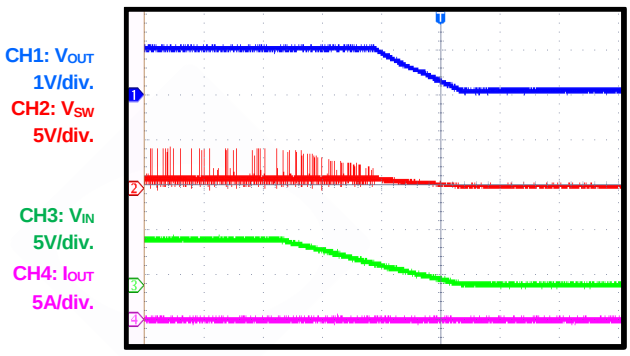
VIN On
I_{OUT} = 6A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

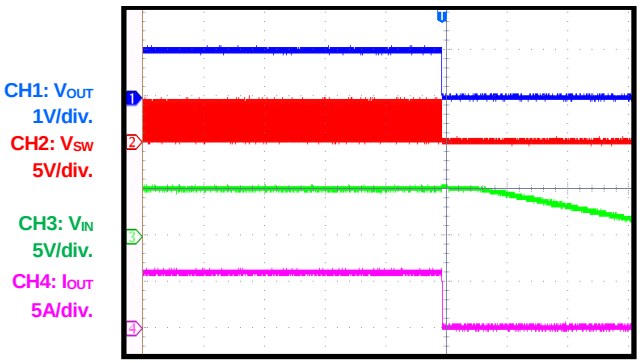
V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

VIN Off
I_{OUT} = 0A



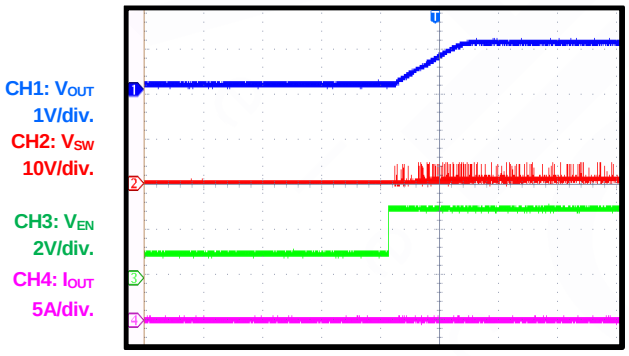
10ms/div.

VIN Off
I_{OUT} = 6A



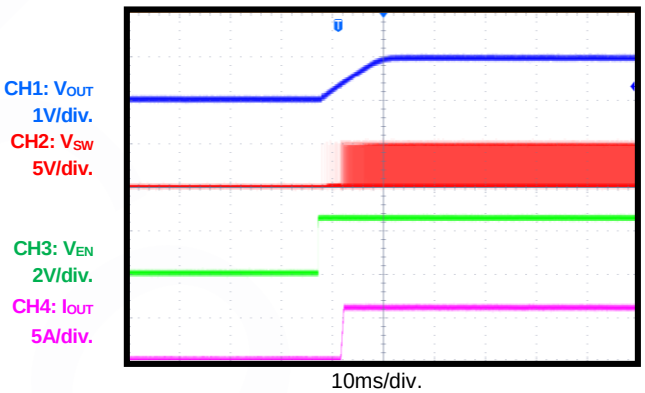
10ms/div.

EN On
I_{OUT} = 0A



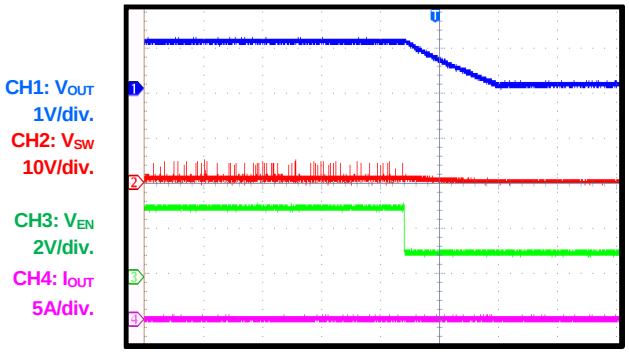
10ms/div.

EN On
I_{OUT} = 6A



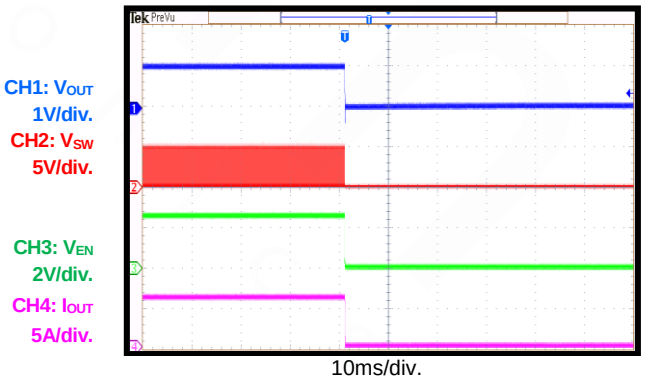
10ms/div.

EN Off
I_{OUT} = 0A



10ms/div.

EN Off
I_{OUT} = 6A

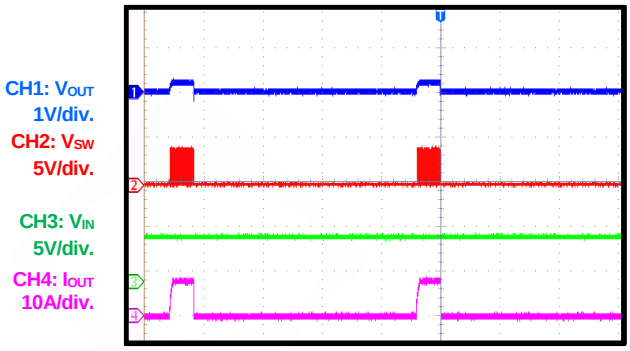


10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

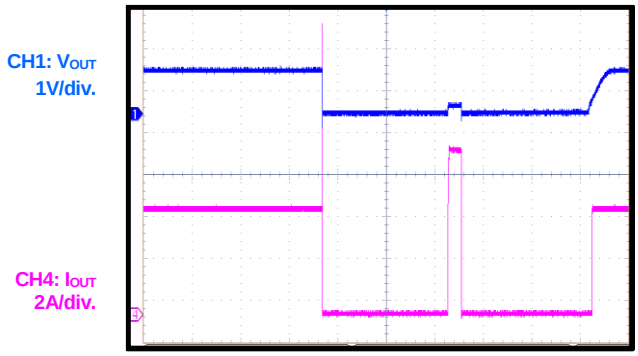
V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4 x 22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

SCP Steady State



20ms/div.

SCP Entry and Recovery



200ms/div.

FUNCTIONAL BLOCK DIAGRAM

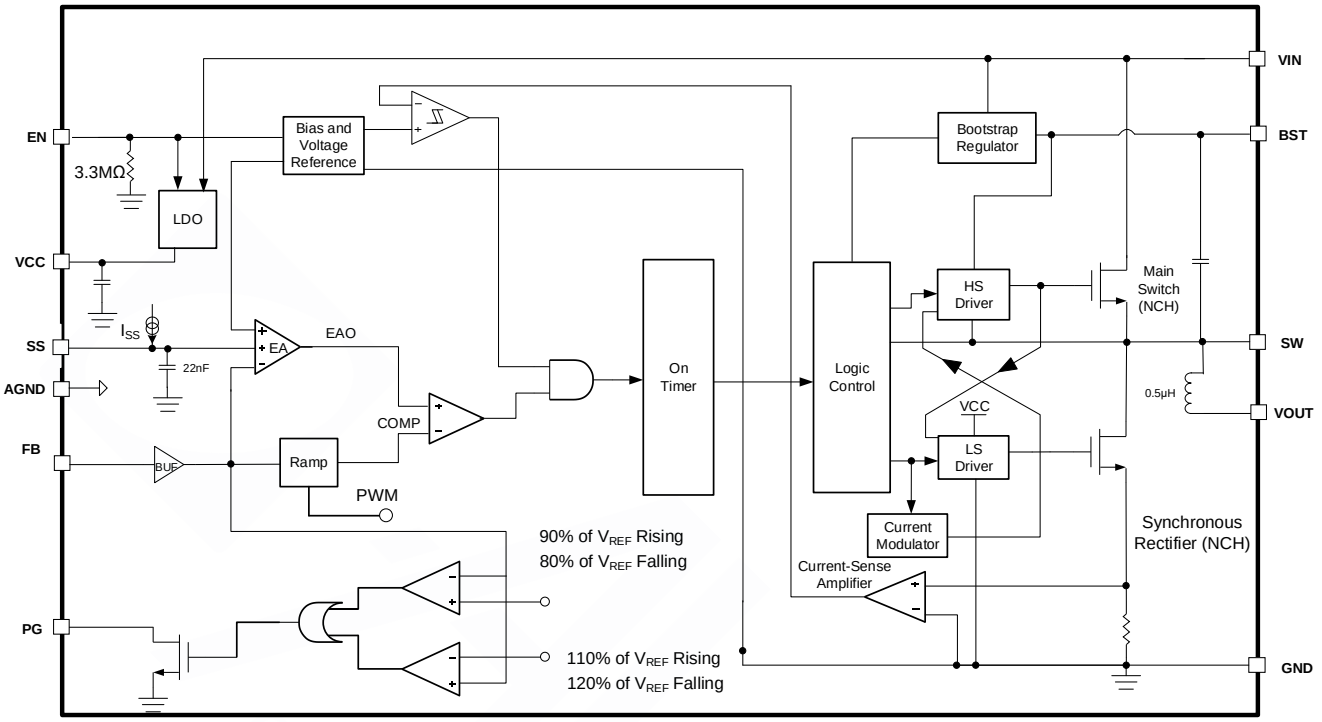


Figure 1: Functional Block Diagram

OPERATION

The MPM3650 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization.

Figure 2 shows the simplified ramp compensation block in the MPM3650.

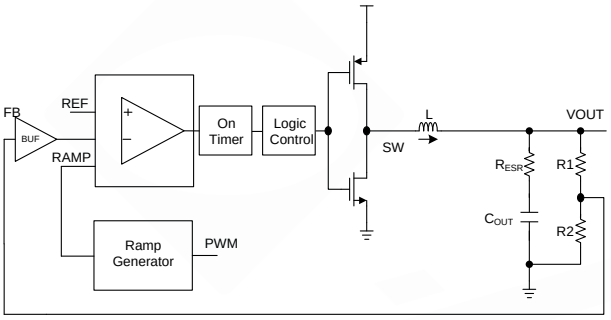


Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), and indicates there is an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant across the input voltage range.

After the on period elapses, the HS-FET turns on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called shoot-through. To avoid shoot-through, a dead-time (DT) is internally generated between the HS-FET off period and LS-FET on period, and vice versa.

Internal compensation is applied for COT control to stabilize operation. Internal compensation improves the jitter performance without affecting the line or load regulation, even if ceramic capacitors are used.

CCM Operation

When the output current is high and the inductor current is always above 0A, the device operates in continuous conduction mode (CCM). Figure 3 shows CCM operation. When V_{FB} is below V_{EAO}, the HS-FET turns on for a fixed interval, which is determined by a one-shot on-timer. When the HS-SFET turns off, the LS-FET turns on until the next period.

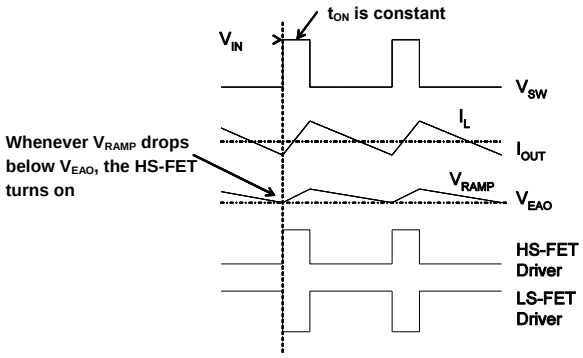


Figure 3: Heavy Load Operation

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

VCC Regulator

The 3.5V internal regulator powers most of the internal circuitries. This regulator takes the VIN input and operates in the full V_{IN} range. If V_{IN} exceeds 3.5V, the output of the regulator is in full regulation. If V_{IN} falls below 3.5V, the output of the regulator decreases following the changes in V_{IN}. There is an internal 1μF decoupling ceramic capacitor within the module.

Enable

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.23V to turn the regulator on; drive EN below 1V to turn it off.

When floating EN, pull it down to GND using an internal 3.3MΩ resistor. EN can be connected directly to VIN, and supports a 17V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3650 UVLO comparator monitors the output voltage of the internal regulator (VCC). The VCC UVLO rising threshold is about 2.5V. and its falling threshold is 2.3V.

If the input voltage exceeds the UVLO rising threshold voltage, the MPM3650 powers up. The

device shuts off when the input voltage drops below the UVLO falling threshold. This is a non-latch protection.

Soft Start

The MPM3650 employs a soft start (SS) mechanism to ensure the output smoothly ramps up during power-up. When the EN pin goes high, an internal current source (6μA) charges up the SS capacitor. The SS capacitor voltage takes over V_{REF} to the PWM comparator when the device is powering on. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage exceeds V_{REF}, it continues to ramp up until V_{REF} takes over. Then soft start finishes, and the device enters steady state operation.

The SS capacitor value can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

An internal 22nF SS capacitor is recommended.

If the output capacitor has a large capacitance, do not set the SS time too short. Otherwise, the device easily reaches the current limit during soft start.

Power Good Indicator

The PG pin is the open drain of a MOSFET that connects to VCC or a voltage source through a resistor (e.g. 100kΩ). The MOSFET turns on when an input voltage is applied, and the PG pin is pulled to GND before soft start completes. After the feedback voltage (V_{FB}) reaches 90% of V_{REF}, the PG pin is pulled high after a 50μs delay. When V_{FB} drops below 80% of V_{REF}, the PG pin is pulled low.

If under-voltage lockout (UVLO) or over-temperature protection (OTP) occurs, the PG pin is immediately pulled low. If an over-current (OC) condition occurs, the PG pin is pulled low when V_{FB} drops below 80% of V_{REF} after a 0.05ms delay. If an over-voltage (OV) condition occurs, the PG pin pulls low when V_{FB} rises above 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls below 110% of V_{REF}, the PG pin is pulled high after a 0.05ms delay.

If the input supply fails to power the MPM3650, PG is clamped low, even if PG is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

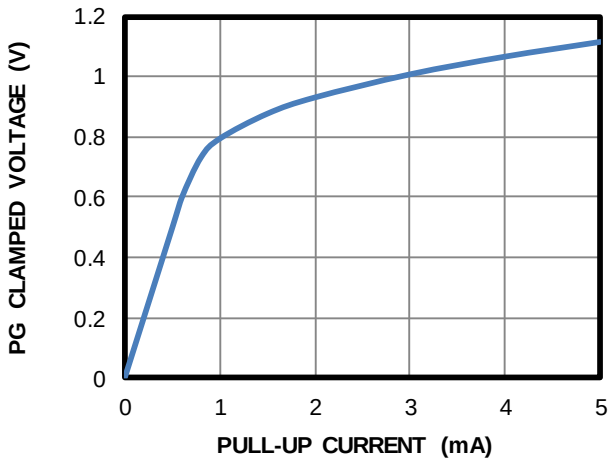


Figure 4: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3650 has valley limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET does not turn on again until the valley current limit disappears. Meanwhile, the output voltage drops until V_{FB} falls below the under-voltage (UV) threshold (typically 50% below V_{REF}). Once a UV condition is triggered, the MPM3650 enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from the OC fault with hiccup mode. This means that the chip disables the output power stage, discharges the soft-start capacitor, then automatically tries to reinitiate soft start. If the OC condition remains after soft start ends, the device repeats this operation until the OC condition disappears, and the output rises back to its regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM3650 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor also charges. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part begins operating normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage. First, choose a value for R2. Choose a reasonable R2, since a small R2 leads to considerable quiescent current loss, and a large R2 makes the FB noise sensitive. It is recommended to choose a value between 2kΩ and 100kΩ for R2. Set the current through R2 below 250μA to balance between system stability and no-load loss. Then R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

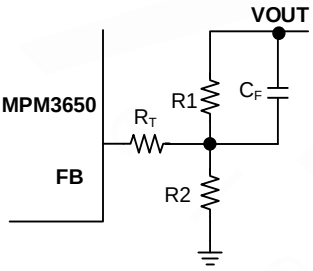


Figure 5: Feedback Network

Table 1 lists recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	CF (pF)	RT (Ω)
1.0	20	30	39	0
1.2	20	20	39	0
1.5	20	13	39	0
1.8	20	10	39	0
2.5	20	6.34	39	0
3.3	20	4.42	39	0

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must have a ripple current rating that exceeds the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

In the case of ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The output voltage ripple is mainly caused by the capacitance.

For simplification, the output voltage ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to consideration regarding the output ripple, a larger output capacitor also offers better load transient response. However, maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, and the device will fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be limited using Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during soft start, and t_{SS} is the soft-start time.

PCB Layout Guidelines [8]

PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor as close to the VIN and PGND pins as possible to minimize high-frequency noise. Keep the input capacitor and VIN pin traces as short and wide as possible.
5. Place the VCC capacitor as close to the VCC pin and GND as possible.
6. Connect VIN, VOUT, and GND to a large copper area to cool the chip, and to improve thermal performance and long-term reliability.
7. Separate input GNDs from the other GND areas at the top layer. Connect them at the internal layers and the bottom layer through multiple vias.
8. Ensure an integrated GND is used at the internal layer or bottom layer.
9. Use multiple vias to connect the power planes to internal layers.

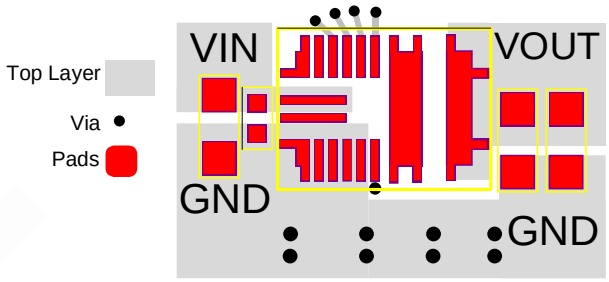


Figure 6: Recommended PCB Layout

Note:

8) The recommended layout is based on the Typical Application Circuits section on page 18.

TYPICAL APPLICATION CIRCUITS

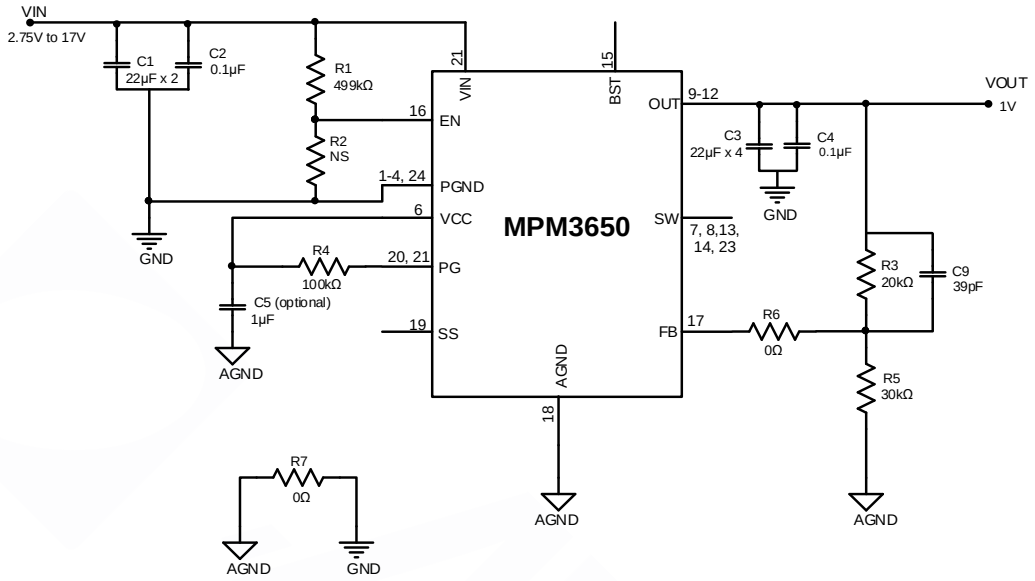


Figure 7: Typical Application Circuits with 1V Output

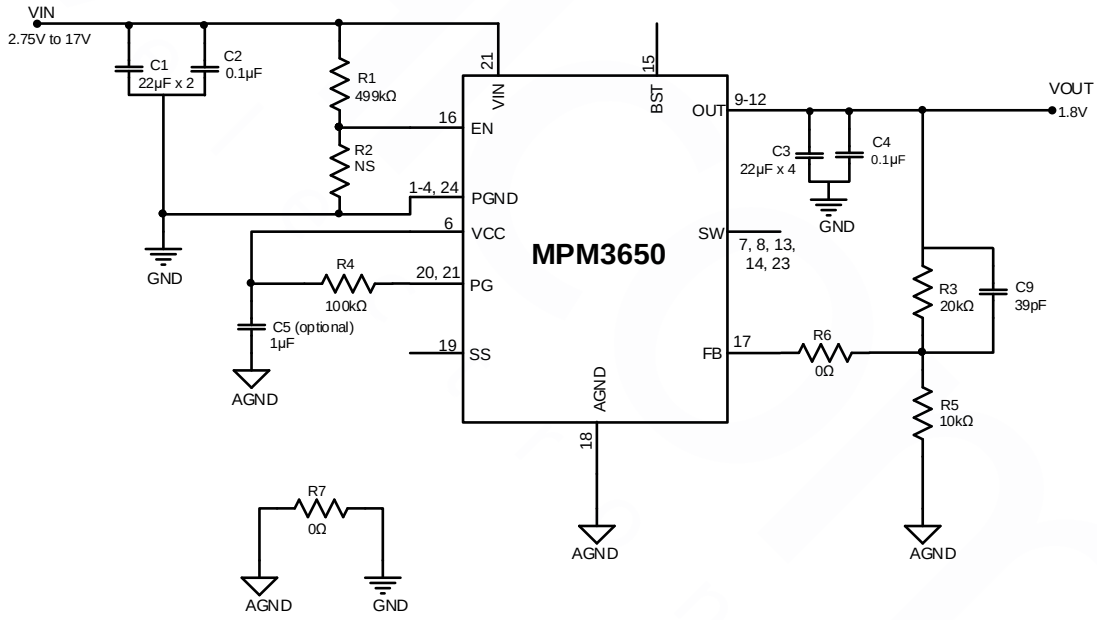


Figure 8: Typical Application Circuits with 1.8V Output

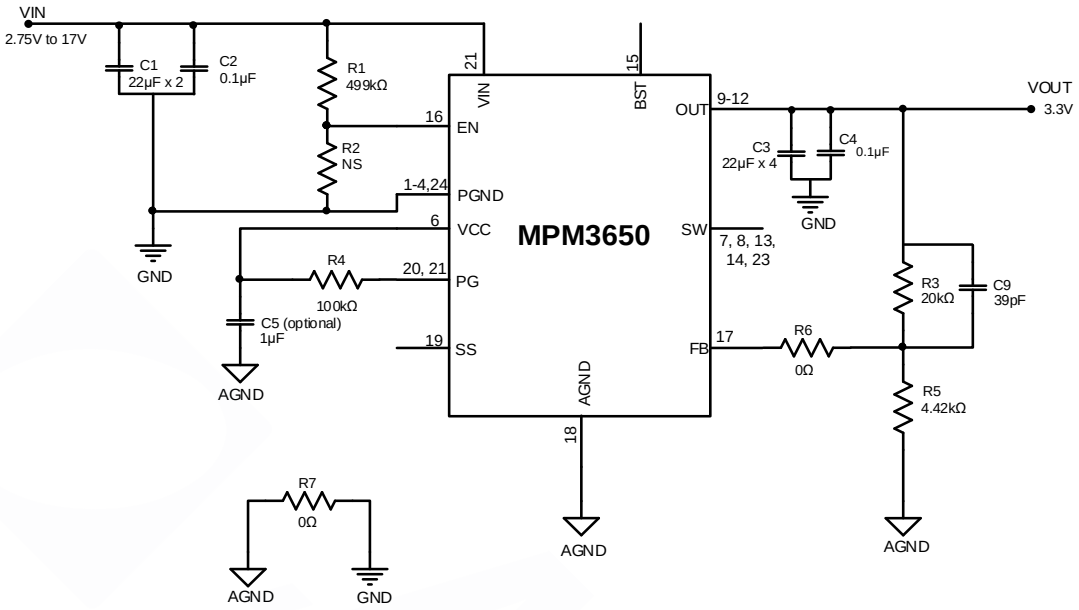
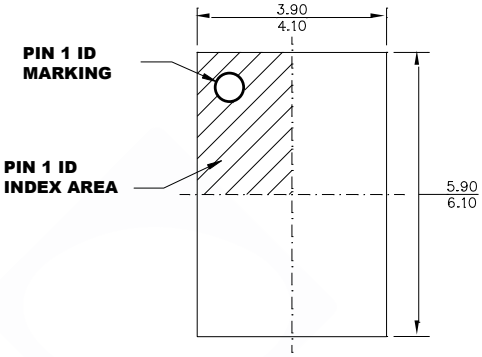


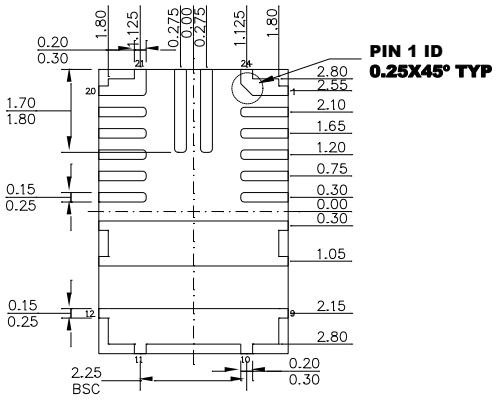
Figure 9: Typical Application Circuits with 3.3V Output

PACKAGE INFORMATION

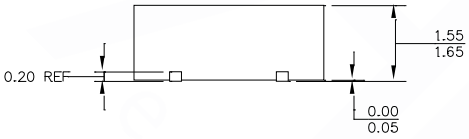
QFN-24 (4mmx6mmx1.6mm)



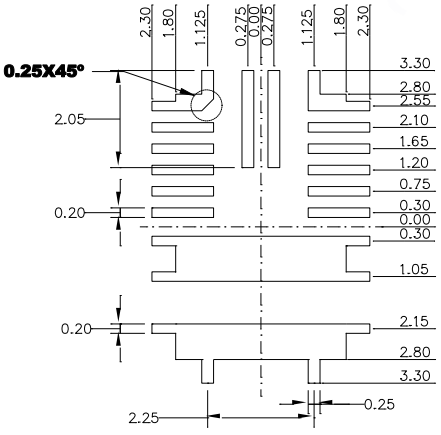
TOP VIEW



BOTTOM VIEW



SIDE VIEW

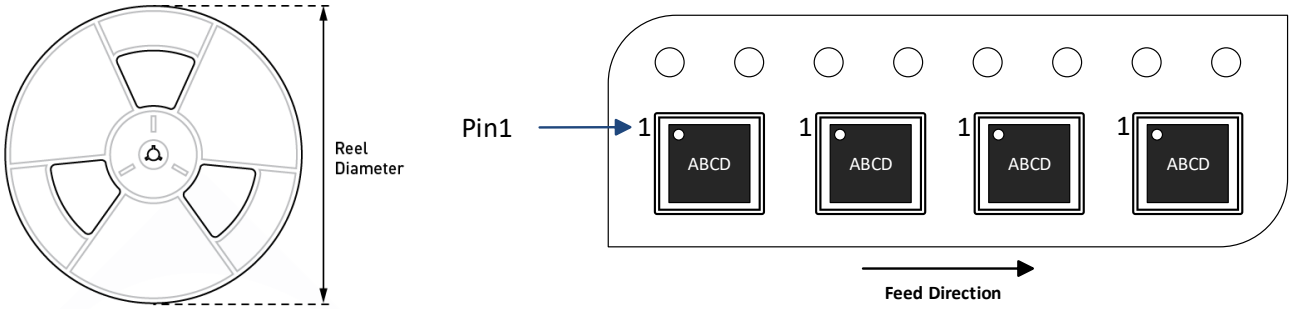


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3650GQW–Z	QFN-24 (4mmx6mmx1.6mm)	2500	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	6/3/2020	Initial Release	-