MPM54304

4V to 16V Input, Quad-Output Power Module with I²C and MTP in Ultra-Thin Package

DESCRIPTION

The MPM54304 is a quad-output, DC/DC step-down power module with up to 3A per output (channel 1 and 2) and 2A per output (channel 3 and 4). Channels 1 and 2 can be paralleled to provide up to 6A of current, and channels 3 and 4 can be paralleled to provide up to 4A of current.

Operating over a 4V to 16V input voltage range, the MPM54304 can support an output voltage range of 0.55V to 7V. The output voltage can be set via the I²C or external resistor divider. The module has internal auto-compensation, which eliminates the need for an external compensation network. The MPM54304 employs a constant-on-time (COT) control scheme to provide ultra-fast load transient responses. This minimizes the required output capacitance.

The MPM54304 features a two-time, non-volatile programmable memory. Its operating parameters are programmable via the I²C.

The MPM54304 requires a minimal number of external components, and is available in ultra-thin LGA-33 (7mmx7mmx2mm) package.

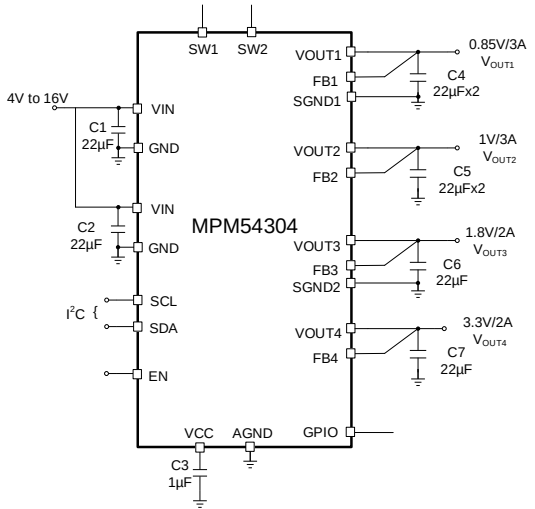
FEATURES

- 4V to 16V Operating Input Range
- Wide Output Voltage:
  - I²C Programmable: 0.55V to 5.4V
  - External Resistor Divider: 0.6V to 7V or V_{IN} * D_{MAX} if V_{IN} < 7V
- Channel 1 and 2: 3A Continuous Current
  Channel 3 and 4: 2A Continuous Current
- Interleaved Operation
- Configurable, Multi-Functional GPIO Pin
- I²C and Configurable Parameters:
  - Paralleling Channel 1 and 2
  - Paralleling Channel 3 and 4
  - Switching Frequency
  - Output Voltage
  - Over-Current and Over-Voltage Protection Threshold
  - Power-On and Power-Off Sequencing
  - Forced PWM or Auto-PWM/PFM

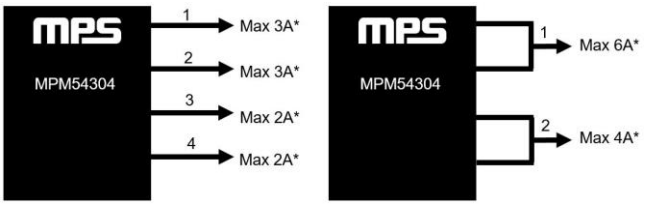
APPLICATIONS

- FPGA Power Supplies
- Multi-Rail Power Systems
- MCU/DSP Power Supplies

TYPICAL APPLICATION



4V to 16V Input and Quad Output



Note:

1) Maximum current per rail is subject to total package power loss derating. See the Max P_{LOSS} vs. Temperature Curve on page 11 for the maximum allowed package power loss rating. The total package power loss is determined as the sum of power loss of all rails: P_{LOSS} = (P_{LOSS}1 + P_{LOSS}2 + … + P_{LOSS}n), where n represents the utilized number of rails.

ORDERING INFORMATION

Part Number*	Package	Top Marking	Note	MSL Rating
MPM54304GMN-XXXX	LGA-33 (7mmx7mm)	*See Below*		3
MPM54304GMN-0000	LGA-33 (7mmx7mm)	*See Below*	Pre-programmed output voltage or I²C adjustable	
MPM54304GMN-0001	LGA-33 (7mmx7mm)	*See Below*	Set output voltage with resistor divider	
MPM54304GMN-0002	LGA-33 (7mmx7mm)	*See Below*	Set output voltage with resistor divider; buck 1 & 2 in parallel	
MPM54304GMN-0003	LGA-33 (7mmx7mm)	*See Below*	Set output voltage with resistor divider; buck 3 & 4 parallel	
MPM54304GMN-0004	LGA-33 (7mmx7mm)	*See Below*	Set output voltage with resistor divider; buck 1 & 2, buck 3 & 4 in parallel	

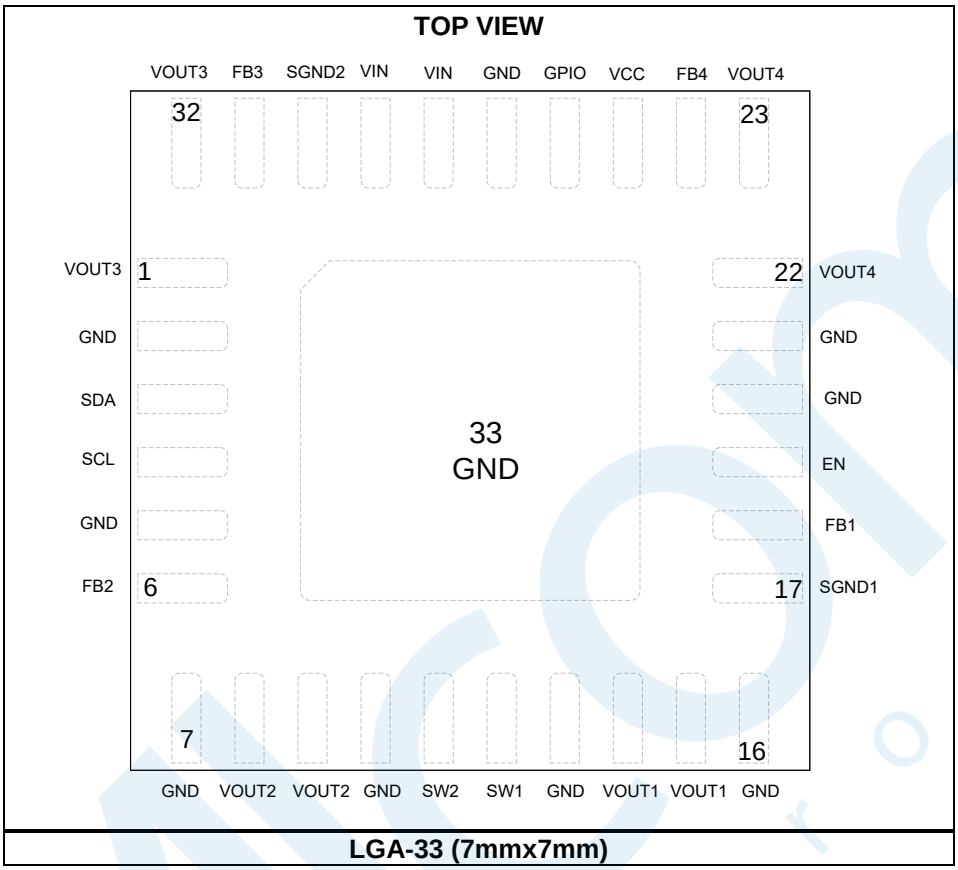
***** -XXXX is the configuration code identifier for register settings stored in the MTP memory. For default configuration with an I²C programmed output voltage, the code is “0000”. See Tables 3 to 12 on page 42 for the detailed configuration information and the register map of codes “0001” to “0004”.

TOP MARKING

MPSYYWW
MP54304
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54304: Part number
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE



LGA-33 (7mmx7mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 32	VOUT3	**Channel 3 output.**
2, 5, 7, 10, 13, 16, 20, 21, 27, 33	GND	**Power ground.** Connect to GND with wide copper plane and sufficient vias.
3	SDA	**I²C data signal pin.**
4	SCL	**I²C clock signal pin.**
6	FB2	**Feedback of buck 2.** Connect buck 2's output directly to this pin or through a feedback resistor divider.
8, 9	VOUT2	**Channel 2 output.**
11	SW2	**Buck 2 switching node.** Connect to SW1 in parallel mode.
12	SW1	**Buck 1 switching node.** Connect to SW2 in parallel mode.
14, 15	VOUT1	**Channel 1 output.**
17	SGND1	**Signal ground 1.** Channel 1 and 2 output voltage feedback sense ground.
18	FB1	**Feedback of buck 1.** Connect buck 1's output directly to this pin or through a feedback resistor divider.
19	EN/SYNCI	**Enable control.** Apply a logic high voltage on this pin to enable the IC; pull EN/SYNCI to logic low to disable the IC. The EN pin has a 2MΩ internal pull-down resistor. Apply a clock on EN/SYNCI to synchronize the switching frequency to the external clock.
22, 23	VOUT4	**Channel 4 output.**
24	FB4	**Feedback of buck 4.** Connect buck 4's output directly to this pin or through a feedback resistor divider.
25	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered from this voltage. Connect a 1µF decoupling capacitor to this pin.
26	GPIO	**General purpose input/output (GPIO) pin – ADD mode.** When the MTP/I²C configure this pin as "ADD," the pin can program four different I²C slave addresses.
		General purpose input/output (GPIO) pin – PG mode. When the MTP/I²C configure this pin as "PG," it is the open-drain power good output. Pull low when any enabled regulator falls below the UV threshold or when all regulators are disabled.
		General purpose input/output (GPIO) pin – Output Port mode. When the MTP/I²C configure this pin as "Output Port," it outputs high/low logics determined by the related register. Open-drain structure.
		General purpose input/output (GPIO) pin – SYNCO mode. When the MTP/I²C configure this pin as "SYNCO," it is the sync output. Phase-shift the clock output to sync another device's switching frequency.
28, 29	VIN	**Supply voltage input.** Requires a ceramic capacitor to decouple the input rail.
30	SGND2	**Signal ground 2.** Channel 3 and 4 output voltage feedback sense ground.
31	FB3	**Feedback of buck 3.** Connect buck 3's output directly to this pin or through a feedback resistor divider.

ABSOLUTE MAXIMUM RATINGS (2)

V_{IN} ..... -0.3V to +18V
V_{SWx} .....
-0.6V (-7V for <10ns) to V_{INx} + 0.3V (22V for <10ns)
EN, FBx ..... -0.3V to +6V (3)
GPIO, VCC, SCL, SDA ..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (4)
.....3.93W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (5)

Input voltage (V_{IN}) ..... 4V to 16V
I²C-set V_{OUT} ..... 0.55V to 5.4V
External divider set V_{OUT}
.....0.6V to 7V or V_{IN} * D_{MAX} if V_{IN} < 7V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

JESD51-7	31.8	23 °C/W
EVM54304-MN-00A	31.8	14.4 °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) For the EN/SYNCI pin's rating, see the Enable (EN/SYNCI) description section on page 17.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, FB high, PFM		1500	2500	μA
Shutdown current	I_{IN_STD}	I²C and MTP alive		40	80	μA
EN rising threshold	V_{EN_R}		-2.5%	1.21	+2.5%	V
EN hysteresis	V_{EN_F}			150		mV
EN input current	I_{EN}	V_{EN} = 2V		1		μA
Frequency SYNC input range[8]	f_{SYNCI}		500		1600	kHz
Default frequency	f_{SW}	Adjustable by MTP, register value: 0x0d D[7:6] = 01	-15%	800	+15%	kHz
PG UV rising	$V_{PG\_UV\_R}$		88%	92%	97%	V_{REF}
PG UV falling	$V_{PG\_UV\_F}$			87%		V_{REF}
PG rising delay [9]	$t_{PG\_R\_DLY}$	MTP adjustable, register value: 0x0e D[4:2] = 000		200		μs
PG falling delay [9]	$t_{PG\_F\_DLY}$			50		μs
Power good, output port sink current capability	V_{PG_Sink}	Sink 1mA			0.4	V
ADD pin voltage threshold 1	V_{ADD_1}	To set I²C address 1, register value: 0x0e D[7:6] = 00			18%	V_{CC}
ADD pin voltage threshold 2	V_{ADD_2}	To set I²C address 2, register value: 0x0e D[7:6] = 00	33%		45%	V_{CC}
ADD pin voltage threshold 3	V_{ADD_3}	To set I²C address 3, register value: 0x0e D[7:6] = 00	56%		71%	V_{CC}
ADD pin voltage threshold 4	V_{ADD_4}	To set I²C address 4, register value: 0x0e D[7:6] = 00	82%			V_{CC}
ADD pin input current	I_{ADD}	V_{ADD} = 2V		0		μA
Frequency sync out range	f_{SYNCO}	Open-drain	500		1600	kHz
Frequency sync out duty	D_{SYNCO}	Phase shift 180° from buck 1		50		%
VCC UVLO rising	V_{CC_R}		2.8	3	3.2	V
VCC UVLO hysteresis	V_{CC_HYS}			100		mV
VCC voltage	V_{CC}	I_{CC} = 0mA	3.1	3.3	3.5	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Thermal shutdown [9]	T_{OTP_R}			160		°C
Thermal hysteresis [9]	T_{HYS}			20		°C
Step-Down Regulator						
VIN UVLO rising	V_{IN_R}	Adjustable by MTP, register value: 0x0c D[2:1] = 01		4.5		V
VIN UVLO hysteresis	V_{IN_HYS}			600		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C [7], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage accuracy	V_{FB1}	Default output of buck 1, register value: 0x02 D[7:0] = 00101101	-1.5%	1	+1.5%	V
	V_{FB2}	Default output of buck 2, register value: 0x05 D[7:0] = 10110111	-1.5%	3.3	+1.5%	V
	V_{FB3}	Default output of buck 3, register value: 0x08 D[7:0] = 01111101	-1.5%	1.8	+1.5%	V
	V_{FB4}	Default output of buck 4, register value: 0x0b D[7:0] = 01011111	-1.5%	1.5	+1.5%	V
Buck 1, Buck 2						
Low-side current limit (source)	$I_{LS\_Valley1}$	Adjustable by MTP, register value: 0x01 D[4:3] = 10	3.2	4.2	5.2	A
	$I_{LS\_Valley2}$	Adjustable by MTP, register value: 0x04 D[4:3] = 01	2	3	4	
Low-side current limit (sink)	I_{CL_PWM1}			-2		A
Minimum on time [9]	t_{ON_MIN1}			33		ns
Minimum off time [9]	t_{OFF_MIN1}			113		ns
Output OVP rising threshold	V_{OVP1_H}		115%	120%	125%	V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			114%		V_{REF}
Output to discharge resistor [9]	R_{SW1}/R_{SW2}			45		Ω
Soft-start time of buck 1	t_{SS_B1}	V_{OUT} = 10 to 90%		0.8		ms
Soft-start time of buck 2	t_{SS_B2}	V_{OUT} = 10 to 90%		1.2		ms
Buck 3, Buck 4						
Low-side current limit (source)	$I_{LS\_Valley3}$	Adjustable by MTP, register value: 0x07 D[4:3] = 00	1.2	2	3	A
	$I_{LS\_Valley4}$	Adjustable by MTP, register value: 0x0a D[4:3] = 01	2	3	4	
Low-side current limit (sink)	I_{CL_PWM2}	Forced PWM mode, OVP, discharge		-1.5		A
Minimum on time [9]	t_{ON_MIN2}			31		ns
Minimum off time [9]	t_{OFF_MIN2}			133		ns
Output OVP rising threshold	V_{OVP2_H}		115%	120%	125%	V_{REF}
Output OVP recovery threshold	V_{OVP2_L}			114%		V_{REF}
Output to discharge resistor [9]	R_{SW3}/R_{SW4}			45		Ω
Soft-start time of buck 3	t_{SS_B3}	V_{OUT} = 10 to 90%		0.8		ms
Soft-start time of buck 4	t_{SS_B4}	V_{OUT} = 10 to 90%		0.7		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications (10)						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}	Sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$			70		ns
Set-up time for repeated start	$t_{SU.STA}$		160			ns
Hold time for repeated start	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	$t_{SU.STO}$		160			ns
Rise time of SCL and SDA	t_R		10		300	ns
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF
SCL low time	t_{LOW}		200			ns

Notes:

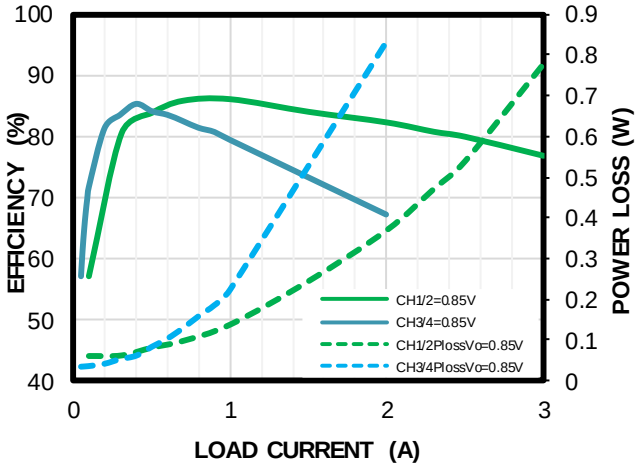
7) Not tested in production. Guaranteed by over-temperature correlation.
8) This function has limitations-only a SYNC IN close to the current system switching frequency can be used.
9) Guaranteed by engineering sample characterization.
10) Maximum I²C bus voltage should be lower than 4V. A 1.8V or 3.3V typical bus voltage is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V , f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

V_{IN} = 5V



Efficiency vs. Load Current

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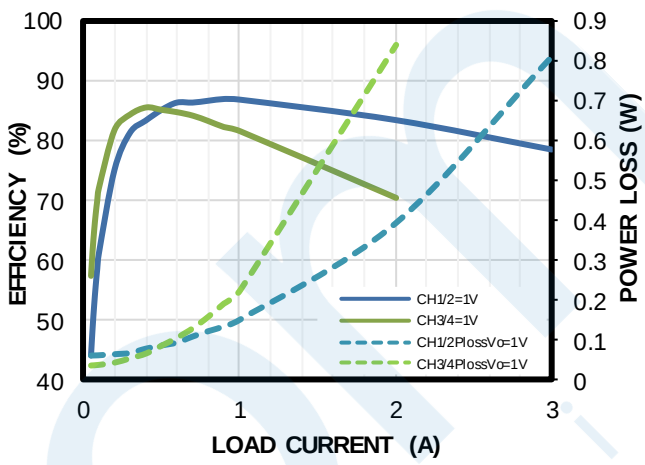

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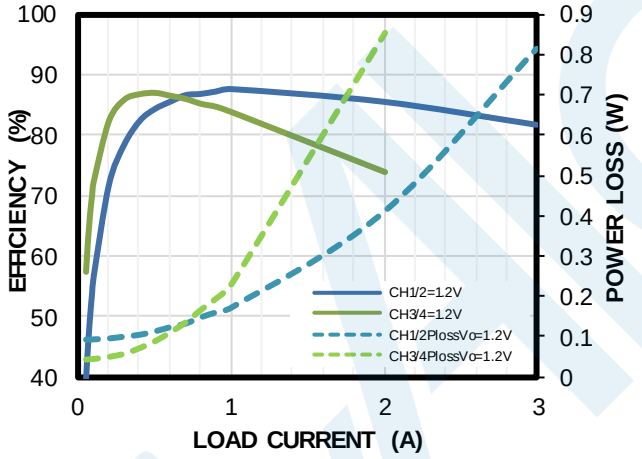
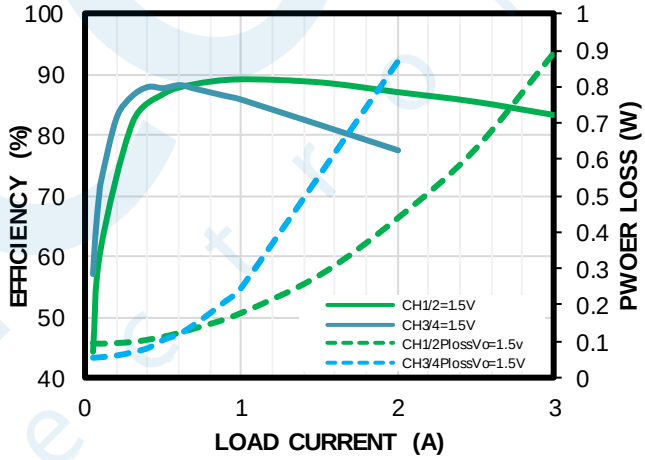
V_{IN} = 5V



Efficiency vs. Load Current

V_{IN} = 5V



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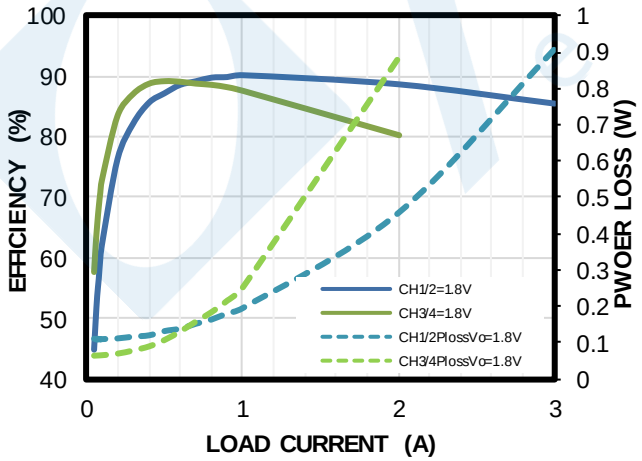

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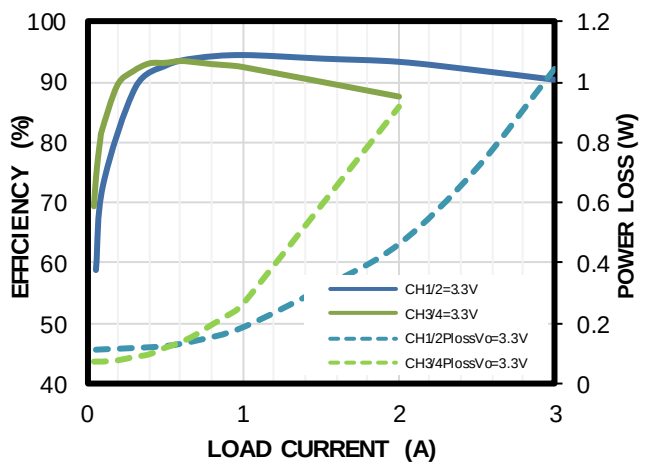

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V , f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current
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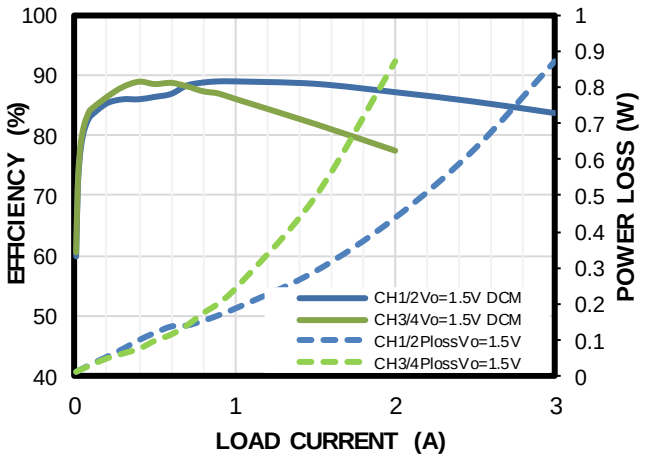

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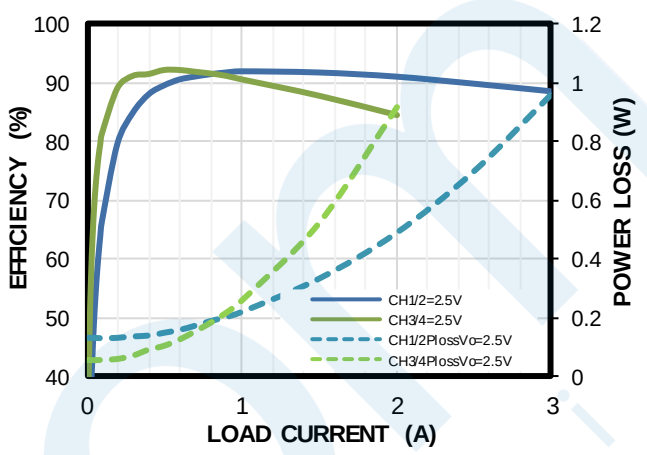
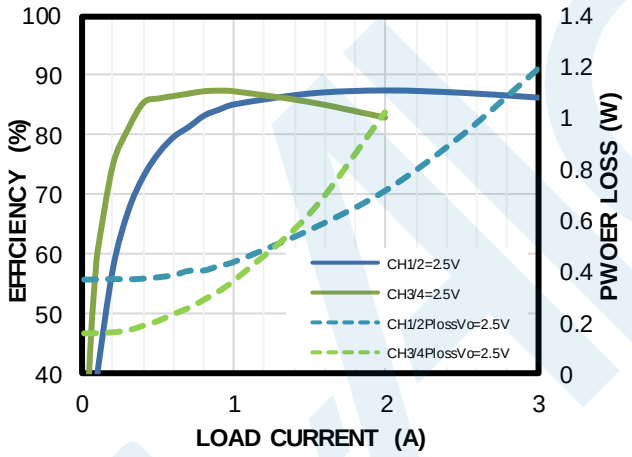


Efficiency vs. Load Current
V_{IN} = 12V



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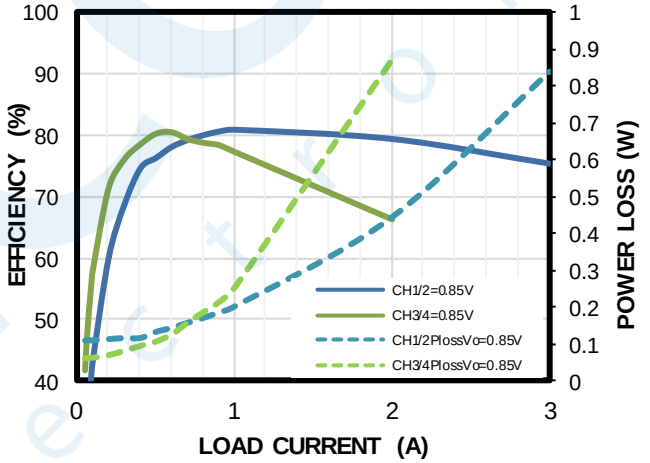

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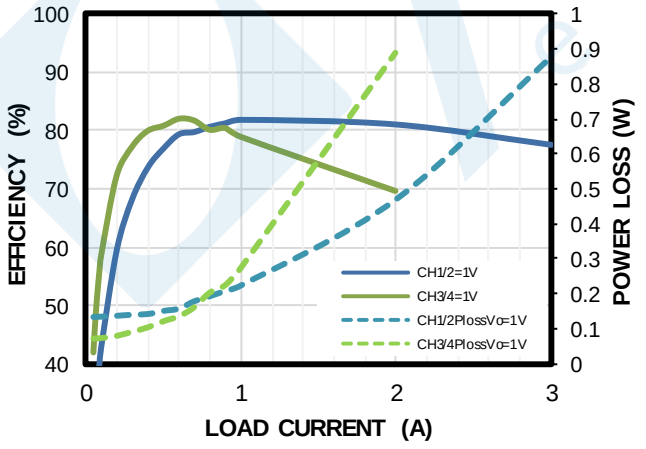

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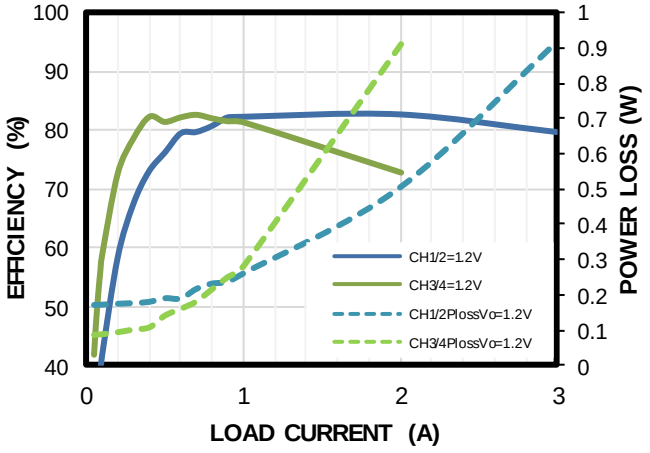

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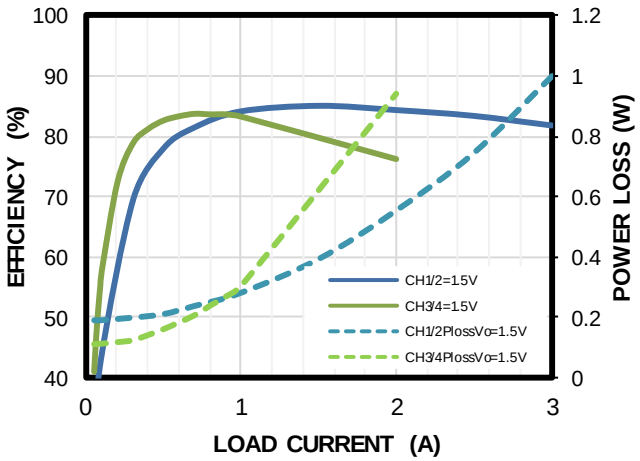

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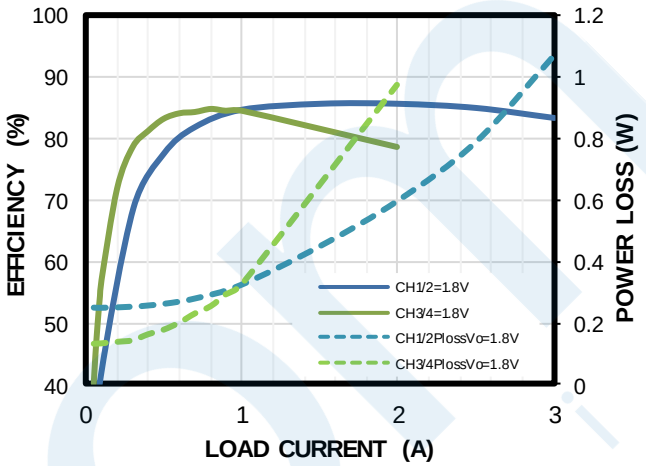

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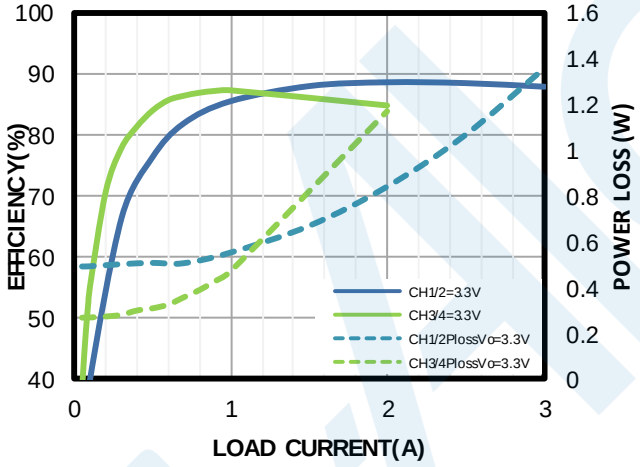

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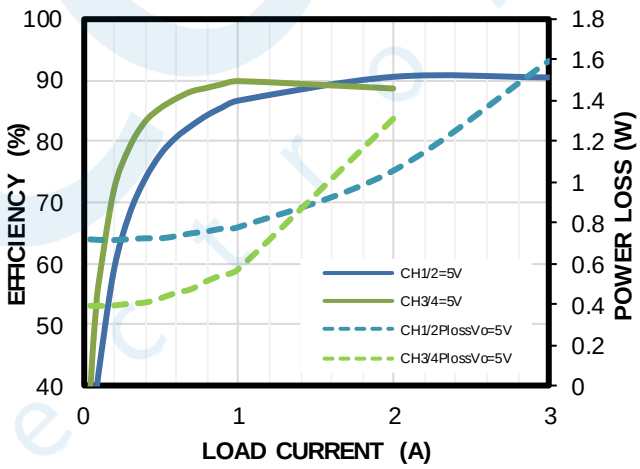

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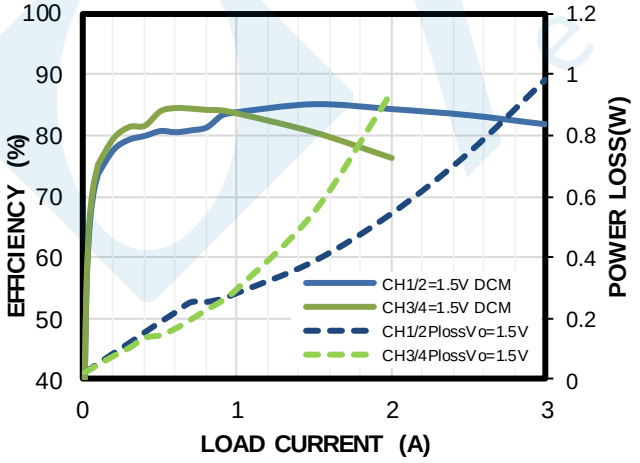
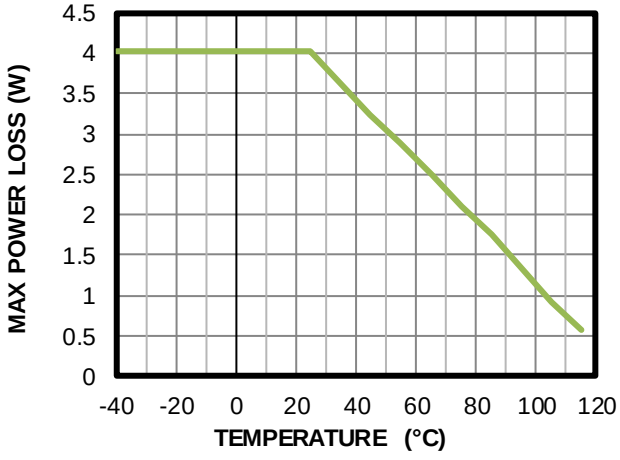


Max Power Loss vs. Temperature

Air flow

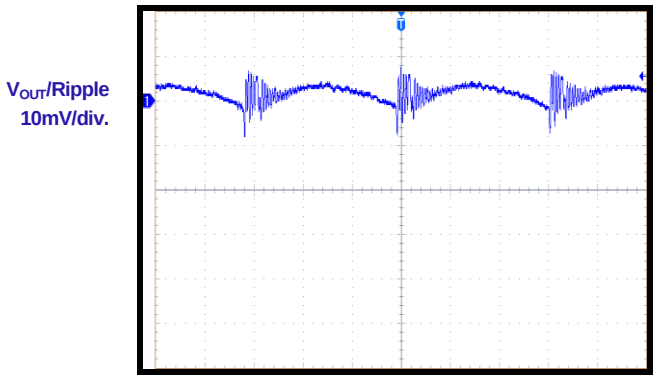


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

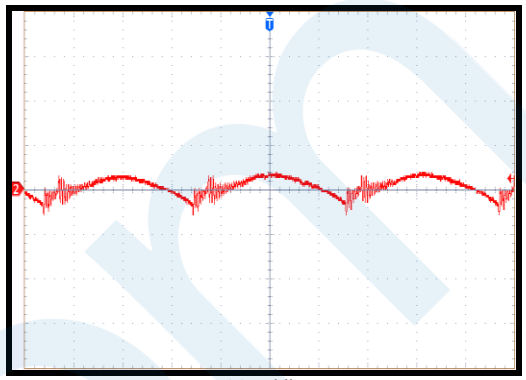
VOUT1 Ripple

I_{OUT} = 3A, V_{OUT} = 1V, CCM



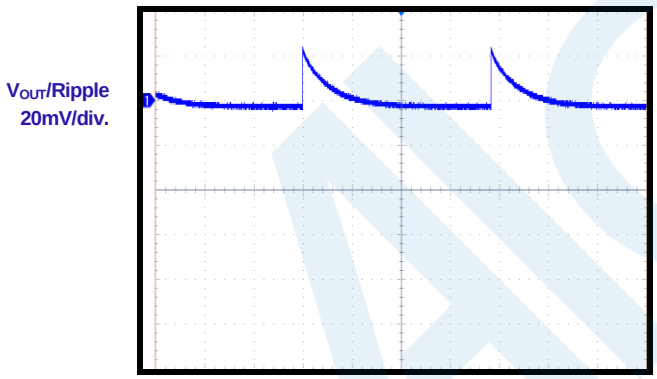
VOUT2 Ripple

I_{OUT} = 3A, V_{OUT} = 1V, CCM



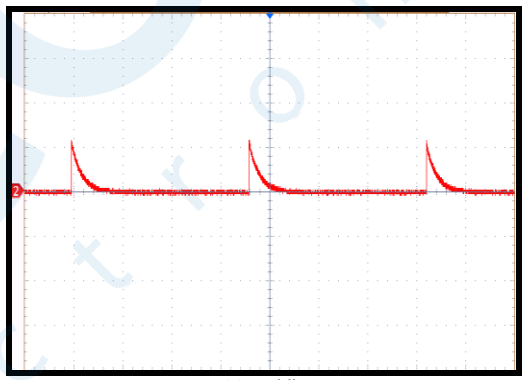
VOUT1 Ripple

I_{OUT} = 0A, V_{OUT} = 1V, DCM



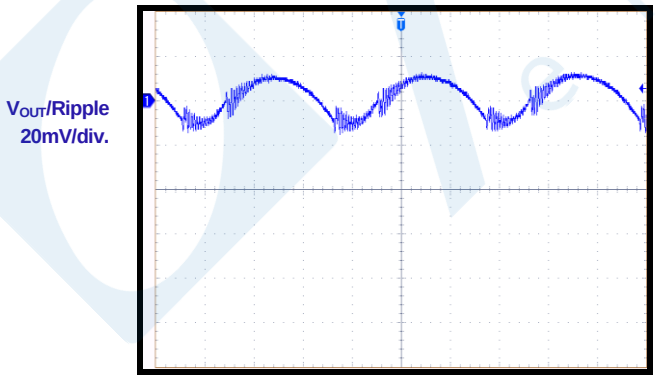
VOUT2 Ripple

I_{OUT} = 0A, V_{OUT} = 1V, DCM



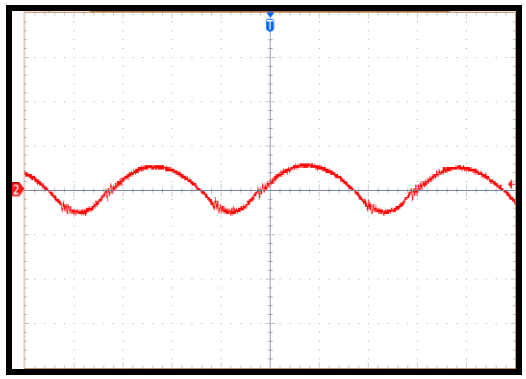
VOUT1 Ripple

I_{OUT} = 3A, V_{OUT} = 3.3V, CCM



VOUT2 Ripple

I_{OUT} = 3A, V_{OUT} = 3.3V, CCM

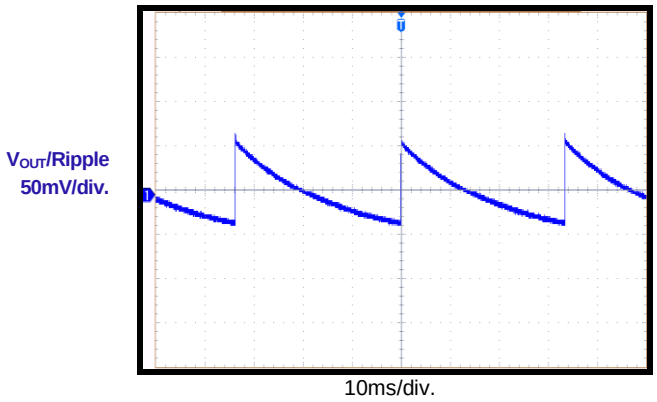


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V , f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

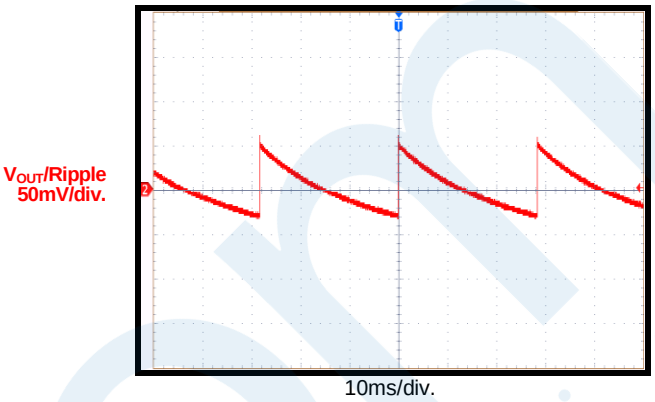
VOUT1 Ripple

I_{OUT} = 0A, V_{OUT} = 3.3V, C_{OUT} = 47µF, DCM



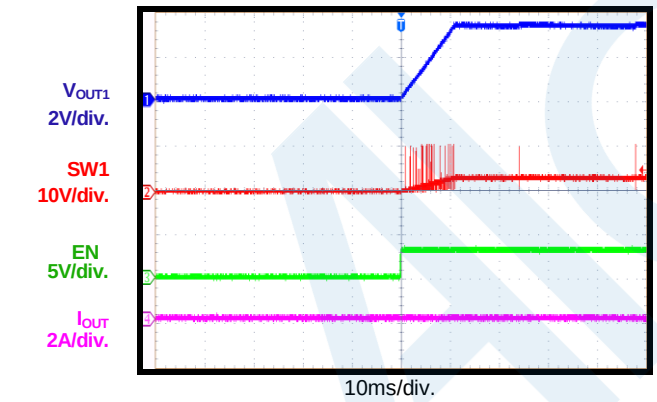
VOUT2 Ripple

I_{OUT} = 0A, V_{OUT} = 3.3V, C_{OUT} = 47µF, DCM



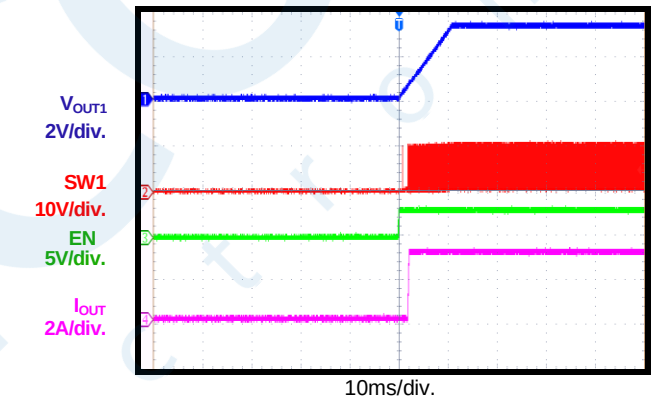
EN On

V_{OUT1} = 3.3V



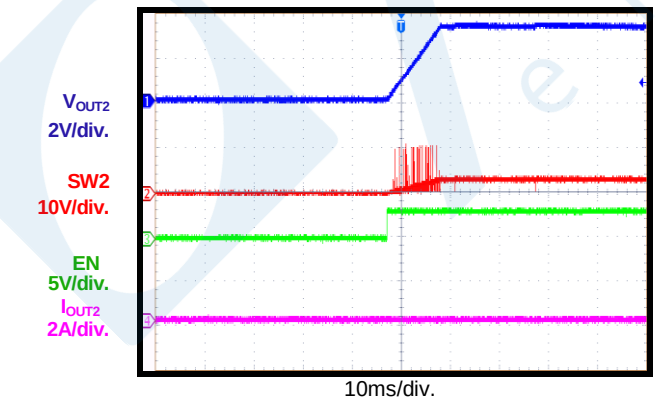
EN On I_{OUT1} = 3A

V_{OUT1} = 3.3V



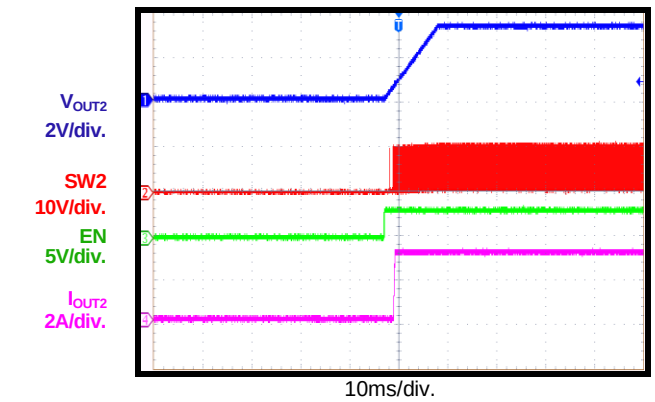
EN On

V_{OUT2} = 3.3V



EN On I_{OUT2} = 3A

V_{OUT2} = 3.3V

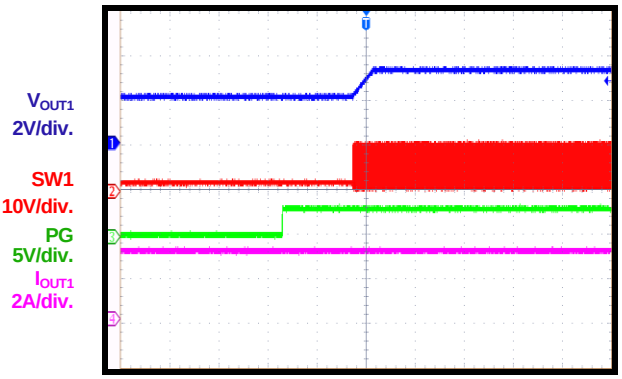


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

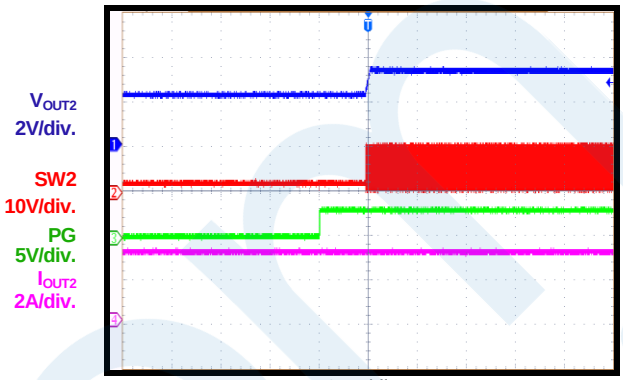
Pre-Bias Start-Up

V_{OUT1} = 3.3V

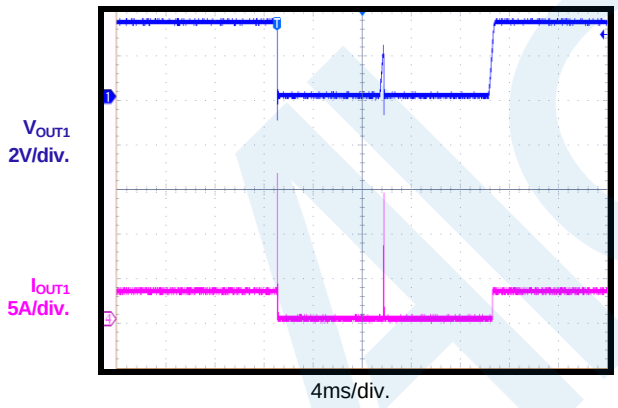


Pre-Bias Start-Up

V_{OUT2} = 3.3V

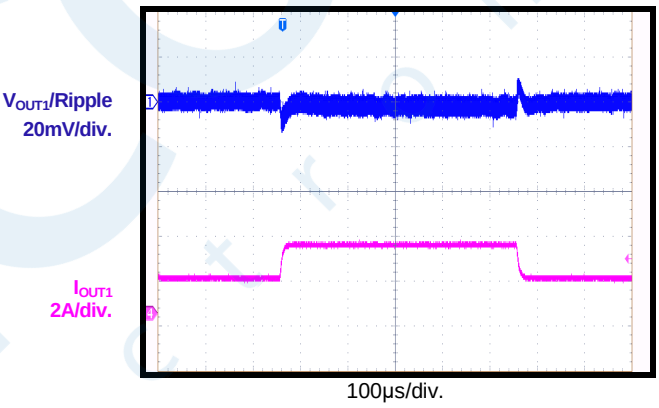


SCP Entry and Recovery



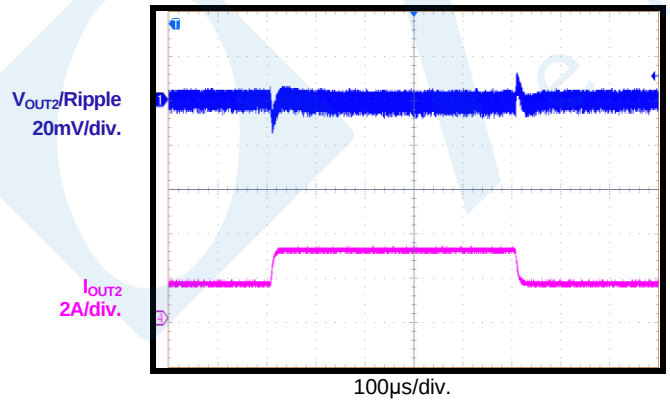
Load Transient

I_{OUT1} = 1.5A to 3A, V_{OUT1} = 1V



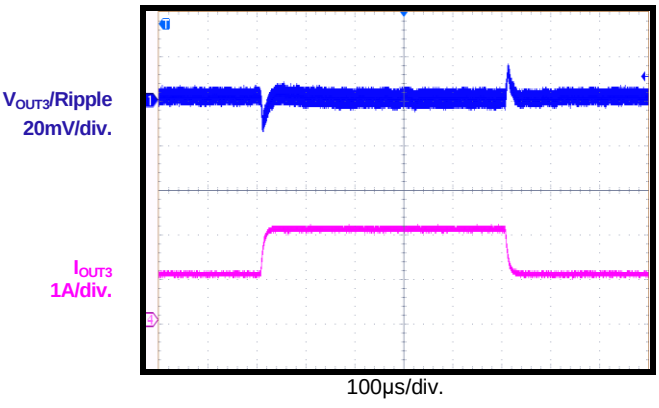
Load Transient

I_{OUT2} = 1.5A to 3A, V_{OUT2} = 1V



Load Transient

I_{OUT3} = 1A to 2A, V_{OUT3} = 1V

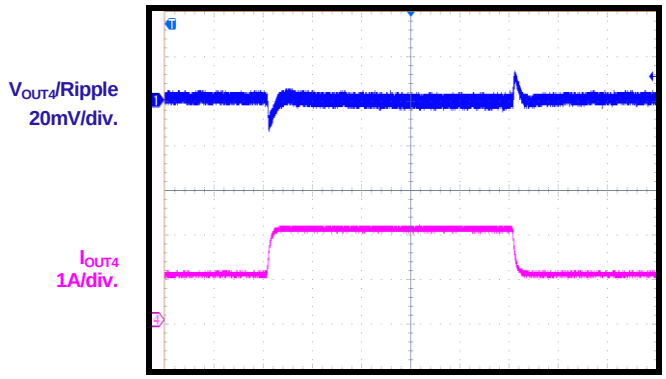


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1/3.3/1.8/1.5V, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

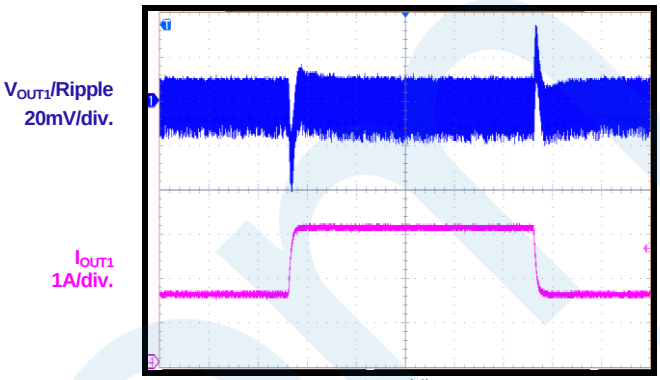
Load Transient

I_{OUT4} = 1A to 2A, V_{OUT4} = 1V



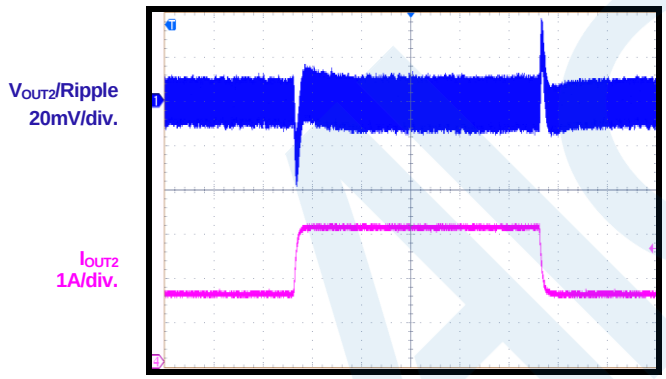
Load Transient

I_{OUT1} = 1.5A to 3A, V_{OUT1} = 3.3V



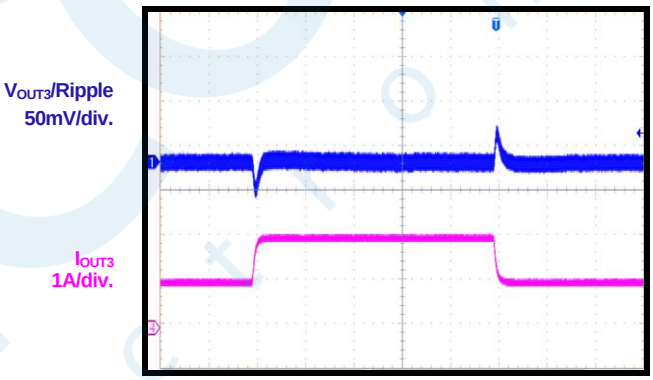
Load Transient

I_{OUT2} = 1.5A to 3A, V_{OUT2} = 3.3V



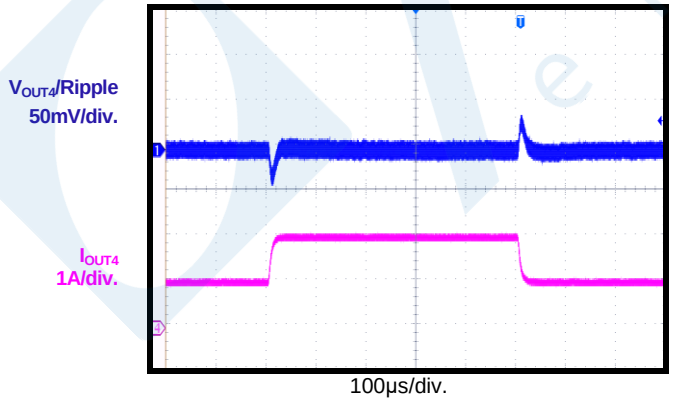
Load Transient

I_{OUT3} = 1A to 2A, V_{OUT3} = 3.3V



Load Transient

I_{OUT4} = 1A to 2A, V_{OU44} = 3.3V



FUNCTIONAL BLOCK DIAGRAM

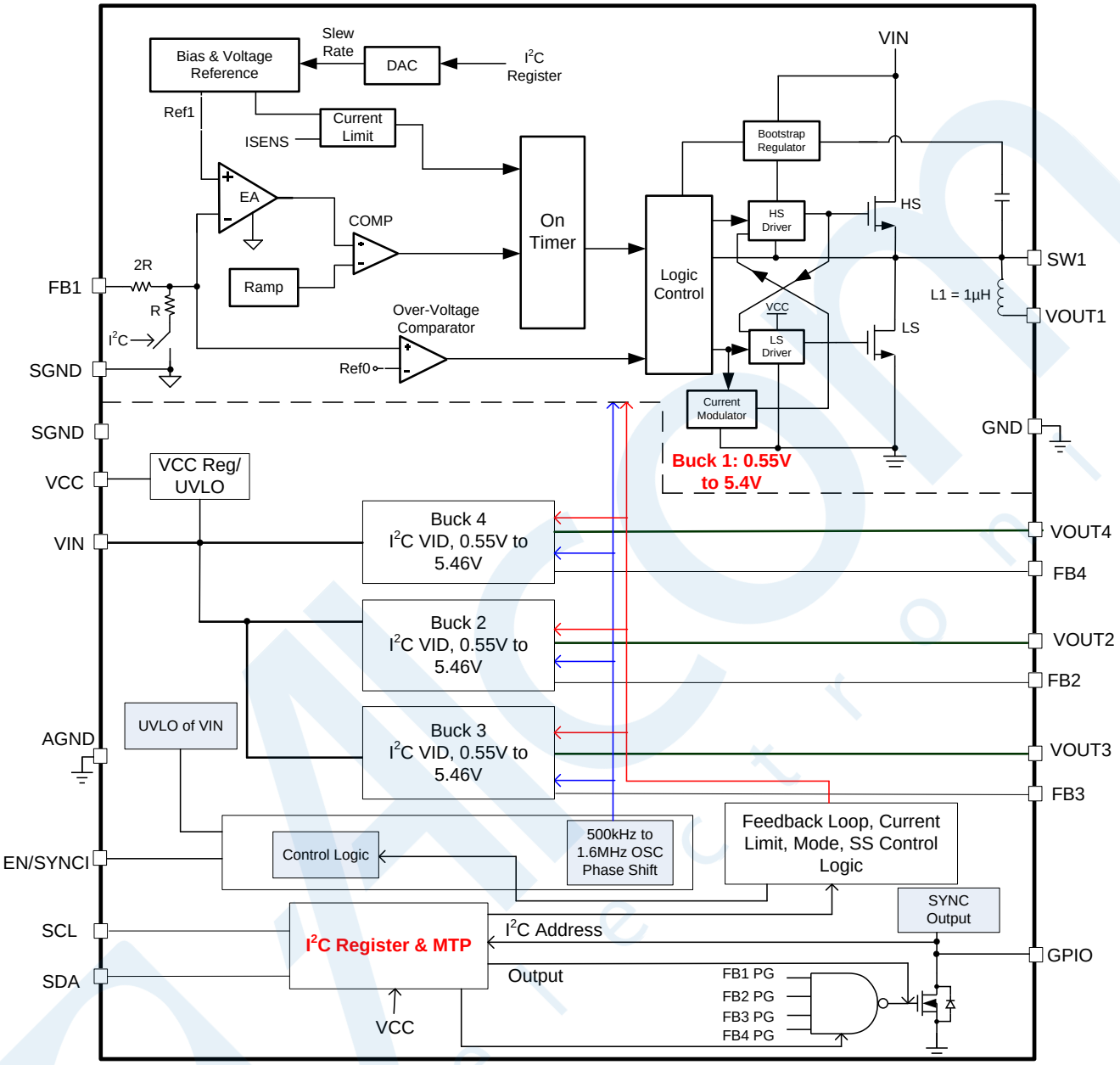


Figure 1: Functional Block Diagram

ANALOG OPERATION

High-Efficiency Buck Regulators

The MPM54304 integrates four synchronous, step-down DC/DC regulators that have built-in soft start, compensation, and hiccup current limit protection. Fixed-frequency, constant-on-time (COT) control provides fast transient response. The switching clock is locked and phase-shifted from buck 1 to buck 4 during CCM operation.

Power Supply and UVLO

When the input voltage exceeds the UVLO rising threshold voltage, the corresponding buck regulators powers up. It shuts down when the input voltage is below the UVLO falling threshold voltage. See the State Machine Description section on page 32 for more details about power-up.

Enable and Switching Frequency SYNC Input (EN/SYNCI)

Frequency SYNC input (EN/SYNCI) is a digital control pin that turns the regulator on and off. Drive EN/SYNCI high to turn the regulator on; drive it low to turn the regulator off. When flaoted, EN/SYNCI is pulled low automatically by an internal resistor.

Connecting EN/SYNCI directly to a voltage source requires limiting the amplitude of the voltage source to ≤6V to prevent damage. A resistor divider is required when pulling EN/SYNCI up to a $12V_{IN}$ supply.

For external clock synchronization, connect a clock with a frequency range between 500kHz and 1.6MHz to EN/SYNCI. Buck 1's SW rising edge will synchronize with the external clock rising edge. Select an external clock signal with a pulse width less than 1.7µs. After synchronization, the buck 1 to buck 4 phase shift continues to follow the MTP definition. The MPM54304's default switching frequency should be set close to the sync input's frequency. For example, when the external SYNCI clock is 500kHz, the internal switching frequency should be set at 533kHz via the I²C or MTP. The I²C and MTP function, including the ADD pin function, is kept active when EN/SYNCI is pulled low.

Thermal Shutdown

The MPM54304 features thermal shutdown by internally monitoring the junction temperature of the power module. If the junction temperature exceeds the 160°C threshold, the power modules shuts off. This is a non-latch protection. There is a 20°C hysteresis. Once the junction temperature drops below 140°C, the device initiates a soft start.

Pre-Bias Start-Up

The MPM54304 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the internal BST voltage is refreshed and charged. The voltage on the internal soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part begins normal operation.

Power Good (PG)

The MPM54304 has power good (PG) register bits (bits D4~D7 of the status register), which indicate whether the enabled buck's output voltage is ready or not. When a buck's feedback voltage (V_{FB}) is above 92% of the reference voltage (V_{REF}), the corresponding PGx bit in the status register is set to from 0 to 1 following a 200µs default or other MTP-programmed delay time. During normal operation, the PGx bit is set to 0 when the corresponding buck regulator falls below the UV threshold with a 50µs delay.

The MPM54304's GPIO pin can be configured as a dedicated PG pin output, as the wire and output of the PG1 to PG4 signals (see Figure 2).

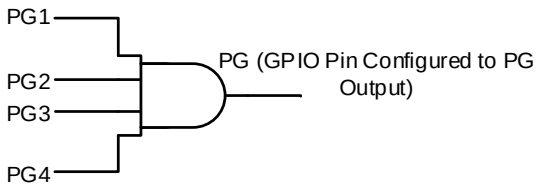


Figure 2: GPIO Pin Configured to PG Output Logic

If UVLO, EN/SYNCI = low, or over-temperature protection (OTP) occurs, the PG pin is pulled

low immediately. If an over-current (OC) condition occurs, the PG pin is pulled low when V_{FB} drops below 87% of V_{REF} after a 50µs delay. The PG function does not indicate an output over-voltage condition.

Output Over-Voltage Protection (OVP)

The MPM54304 monitors the output voltage. If the output voltage exceeds 120% of the regulation voltage for more than 2.5µs, it enters OVP discharge mode. In OVP discharge mode, the low-side MOSFET (LS-FET) turns on and remains on until the low-side current reaches the negative current limit. This discharges the output and tries to keep the output voltage within the normal range. If the OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior. The part exits this discharge mode when V_{FB} falls below 114% of V_{REF}.

If the input voltage exceeds 18V (the input OVP threshold) during OVP discharge mode, the MPM54304 stops switching until the input voltage falls below 16V. Then the MPM54304 enters discharge mode again. This input OVP function is only active during an output OV condition.

The OVP function can be enabled or disabled through the I^2C and MTP interface.

Output Discharge

In order to discharge the energy of the output capacitor during the shutdown sequence, there are discharge resistors (typically 45Ω) from the SWx pin to ground. The discharge function can be enabled or disabled through the I^2C and MTP interface.

Soft Start

The MPM54304 features a soft start (SS) mechanism to ensure smooth output ramp-up during power-up. When the part is enabled and the BST voltage reaches its rising threshold, the internal DAC outputs a ramp voltage (reference voltage). The output voltage smoothly ramps up with the reference voltage. When the DAC output reaches the final voltage, it stops at that level. At this point, soft start finishes and the device enters steady state operation.

The start-up delay and soft-start slew rate are both programmable via the MTP.

Out-of-Phase Operation and Clock SYNC Out

Buck 1 to buck 4 are frequency-locked and capable of phase shift. Phase shift is set to a default (described below), but can also be changed by the MTP. When the GPIO pin is configured to “SYNC Out” mode, the MPM54304 outputs a 180° phase shift from the internal clock’s rising edge with a 50% duty pulse (see Figure 3). This is an open-drain output; an external 1kΩ pull-up resistor should be added. The SYNC Out signal disappears if buck 1 to buck 4 all enter light-load sleep mode. The SYNC Out signal is enabled after the power-on sequence has completed.

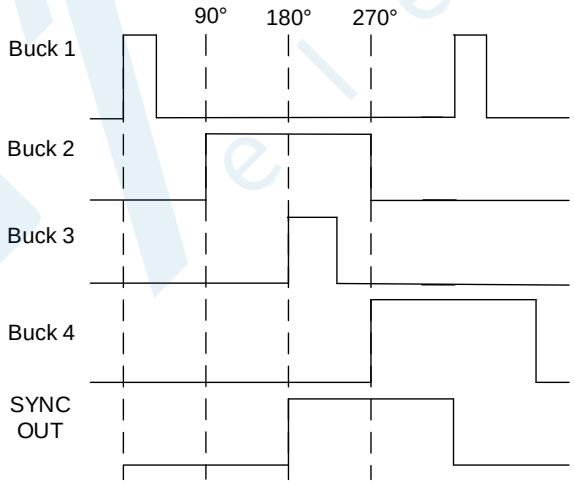


Figure 3: Phase Shift Example

VCC Regulator

A 3.3V internal regulator powers most of the internal circuitries. A decoupling capacitor is needed to stabilize the regulator and reduce the ripple. This regulator takes the V_{IN} input and operates in the full V_{IN} range.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM54304 has valley current limit control. The inductor current is monitored during the LS-FET on state. When the sensed inductor current exceeds the valley current limit threshold, the device enters over-current protection (OCP) mode. The HS-FET cannot turn on until the current falls below the valley current limit. Meanwhile, the output voltage drops until it is below the under-voltage (UV) threshold, which is typically 45% below the reference.

If UV and OCP are both triggered, the MPM54304 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce power dissipation during a short-circuit condition. During OCP, the device tries to recover from the over-current fault with hiccup mode. To do this, the chip disables the output power stage, discharges the soft-start capacitor, then automatically tries to soft start again. If the over-current condition still exists when soft start finishes, the device repeats this operation. OCP a is non-latch protection.

Parallel Output Mode

The outputs of the MPM54304 can be connected in parallel to provide higher current. Output 1 and output 2 can be paralleled to provide up to 6A of current. Output 3 and output 4 can be paralleled to provide up to 4A of current. It should be noted that the maximum output current in parallel mode is also limited by the total power dissipation.

Figure 18 shows the connections for parallel mode operation (see page 41). To operate output 1 and output 2 in parallel mode, connect VOUT1 to VOUT2, and FB1 to FB2. To operate output 3 and output 4 in parallel mode, connect VOUT3 to VOUT4, and FB3 to FB4.

All buck function commands follow buck 1 and buck 3 in parallel mode. The phase delay should be the same for buck 3 and buck 4 when in parallel mode.

DIGITAL INTERFACE

MTP Program

The I²C and MTP blocks become active once the VCC pin's voltage exceeds its 2V rising threshold, no matter whether the EN pin's voltage is high or low. Figure 4 shows a system-level application example.

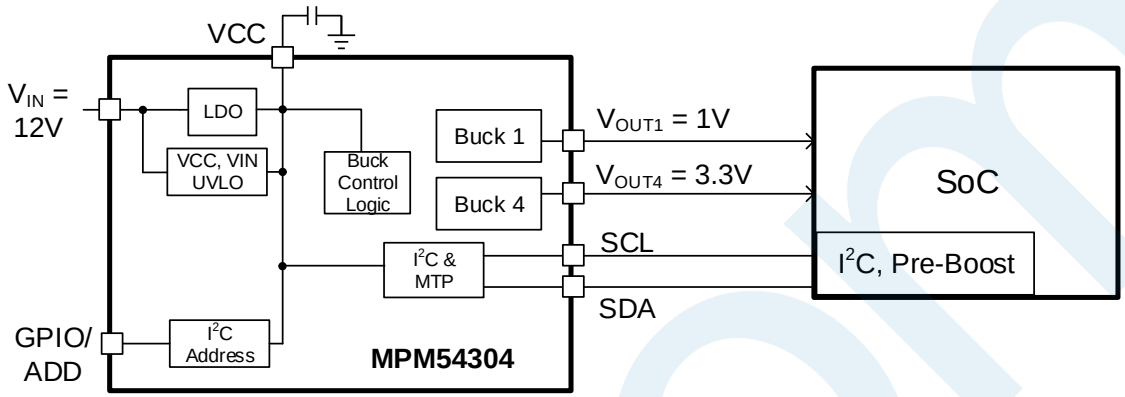


Figure 4: I²C Start-Up Block

When VIN powers up and EN/SYNCI is pulled high, the MPM54304 starts up with a "safe mode" that allows the SoC to start up without damage. In safe mode, only one or two power rails will turn on. For example, V_{OUT1} = 1V, V_{OUT4} = 3.3V, other power rails are off. The default buck 1 to buck 4 configuration is determined by the MTP e-fuse.

The MTP data is loaded into the corresponding I²C registers during the first power-up. The I²C registers directly control the parameters of buck 1 to buck 4. The MTP load to I²C register conditions are described below:

- V_{CC} > 2V, first power-up.
- MTP programming has been completed.

Toggling EN/SYNCI on and off will not reload the MTP registers into the I²C registers again.

The I²C register and MTP table are correlated to each other. The MTP table can be accessed and programmed through the I²C interface. It can be programmed two times.

After buck 1 and buck 4 power up, the SoC programs the MPM54304 I²C register and MTP. For details on how to identify a valid slave address, see the I²C Bus Slave Address section on page 30. When the SoC writes to the I²C register, the I²C register takes effect immediately. It can also be burned into the MTP. The VCC voltage (V_{CC}) rises up to 5.2V when the MTP is programmed. In order to protect the device, buck regulators are shut down when burning the MTP e-fuse. After MTP programming is done, the buck regulators start up sequentially. During normal buck operation, the I²C master can read and write the register's data.

Safety Considerations for Writing MTP

Several protection items can reduce the failure rate of MTP writing. Take the following steps before writing the MTP registers:

Step 1: Set the MTP_Program bit to 1. The I²C register will be locked to prevent write operation until MTP programming finishes; the SoC can read the I²C register during this period.

Step 2: Check the MTP burning power supply. If it is above 5.1V, continue the MTP write; otherwise, abort and unlock the I²C write protection.

Step 3: The MPM54304 can calculate the sum of all related I²C registers to be burned in the MTP register, then generate a 16-bit checksum. This is not a truly sum of all I²C registers, but an arithmetic to combine all data. The checksum result is also written to the MTP register.

After the MTP write operation finishes, there is typically a 100ms delay. The MPM54304 then sets the MTP_Program bit to 0, and the I²C register write protection is unlocked. The SoC

can read the I²C register; if the MTP_Program bit goes to 0, it indicates that MTP programming is done.

After the MTP write operation finishes, the SoC can read the MTP register data to confirm that the correct value is saved into the MTP registers. If anything is wrong, the SoC will write the MTP again.

During VIN power-up, before loading the MTP data into the I²C register, the MPM54304 does a checksum calculation for all related MTP registers, then compares it with the checksum byte. If they match, the MTP data is loaded into the I²C register. Otherwise, the I²C register uses the hard-coded default value. There is an I²C register flag bit to indicate whether there is a checksum error.

MTP Table

	REG (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck 1	40			Soft Start Delay1		Additional Phase Delay1	Soft Start Time1		
	41	Vout_Limit_EN1	Mode1	Current Limit1		VOUT_OVP_EN1	Phase Delay Select1		VOUT_DIS_EN1
	42	Vout_Select1	V_Ref1						
Buck 2	43			Soft Start Delay2		Additional Phase Delay2	Soft Start Time2		
	44	Vout_Limit_EN2	Mode2	Current Limit2		VOUT_OVP_EN2	Phase Delay Select2		VOUT_DIS_EN2
	45	Vout_Select2	V_Ref2						
Buck 3	46			Soft Start Delay3		Additional Phase Delay3	Soft Start Time3		
	47	Vout_Limit_EN3	Mode3	Current Limit3		VOUT_OVP_EN3	Phase Delay Select3		VOUT_DIS_EN3
	48	Vout_Select3	V_Ref3						
Buck 4	49			Soft Start Delay4		Additional Phase Delay4	Soft Start Time4		
	4A	Vout_Limit_EN4	Mode4	Current Limit4		VOUT_OVP_EN4	Phase Delay Select4		VOUT_DIS_EN4
	4B	Vout_Select4	V_Ref4						
System	4C	EN1	EN2	EN3	EN4		UVLO		OP_BIT
System	4D	FREQ		Shutdown_Delay_EN	I²C Slave Address				
System	4E	ADD_PG_OP_SYNCOUT			PG_Delay			Parallel_2	Parallel_1
System	4F	MTP configure code. “0x00” means standard MPM54304; “0x01” means MPM54304-0001 part number.							
System	50	MTP revision number. The customer may need to update the MTP value from time to time, so the revision number is stored here.							
System	51	Checksum1 of MTP register 0x40 to 0x50: • When writing the I²C register data into the MTP, the MPM54304 does a checksum of all related I²C registers, and writes the result in this and the next byte. • During power-up, the MPM54304 calculates and compares the MTP cell’s data with the 0x51~0x52 registers’ content. If they match, MTP data is loaded into the I²C register; otherwise, the I²C register ignores the MTP data and uses the default setting.							
System	52	Checksum2 of MTP register 0x40~0x50.							

MTP Table Description

<table>
<tr><th>Name</th><th>Bit</th><th>Default</th><th>Description</th></tr>
<tr><td>Soft-Start Delay</td><td>D[5:4]</td><td>Soft Start Delay1 = 01
Soft Start Delay2 = 11
Soft Start Delay3 = 01
Soft Start Delay4 = 10</td><td>The delay time between EN = high and the system being ready to buck V_{OUT} starting to ramp up. Two bits can set four different values:
D[5:4] = 00: 0ms, time slot 0
D[5:4] = 01: 1ms, time slot 1
D[5:4] = 10: 2ms, time slot 2
D[5:4] = 11: 3ms, time slot 3
See the Power-On Sequence section on page 33 for the time slot definition.</td></tr>
<tr><td>Additional Phase Delay</td><td>D[3]</td><td>Delay1 = 0
Delay2 = 0
Delay3 = 0
Delay4 = 0</td><td>Set to 1 to add a 100ns phase delay for the buck high-side switch turn-on edge.</td></tr>
<tr><td>Soft-Start Time</td><td>D[2:0]</td><td>Soft Start Time1 = 010
Soft Start Time2 = 011
Soft Start Time3 = 001
Soft Start Time4 = 001</td><td>Soft-start slew rate setting bit of each buck regulator. The slew rate below is the internal reference voltage slew rate. If the Vout_Select bit is set to 1, the V_{OUT} slew rate is 2 times the value.
D[3:0] = 000: 2.67mV/µs soft-start slew rate
D[3:0] = 001: 1.6mV/µs soft-start slew rate
D[3:0] = 010: 1mV/µs soft-start slew rate
D[3:0] = 011: 0.67mV/µs soft-start slew rate
D[3:0] = 101: 0.25mV/µs soft-start slew rate
D[3:0] = 110: 0.167mV/µs soft-start slew rate
D[3:0] = 111: 0.1mV/µs soft-start slew rate
Available soft-start time vs. the V_{OUT} voltage:
Soft-start time (ms):
<table>
<tr><th>3 Bits</th><th>Slew Rate (mV/µs)</th><th>V_{OUT} = 5V</th><th>V_{OUT} = 3.3V</th><th>V_{OUT} = 2.5V</th><th>V_{OUT} = 1.8V</th><th>V_{OUT} = 1V</th><th>V_{OUT} = 0.6V</th></tr>
<tr><td>000</td><td>2.67</td><td>0.6</td><td>0.4</td><td>0.3</td><td>0.7</td><td>0.4</td><td>0.2</td></tr>
<tr><td>001</td><td>1.6</td><td>1.0</td><td>0.7</td><td>0.5</td><td>1.1</td><td>0.6</td><td>0.4</td></tr>
<tr><td>010</td><td>1</td><td>1.7</td><td>1.1</td><td>0.8</td><td>1.8</td><td>1.0</td><td>0.6</td></tr>
<tr><td>011</td><td>0.67</td><td>2.5</td><td>1.6</td><td>1.2</td><td>2.7</td><td>1.5</td><td>0.9</td></tr>
<tr><td>100</td><td>0.4</td><td>4.2</td><td>2.8</td><td>2.1</td><td>4.5</td><td>2.5</td><td>1.5</td></tr>
<tr><td>101</td><td>0.25</td><td>6.7</td><td>4.4</td><td>3.3</td><td>7.2</td><td>4.0</td><td>2.4</td></tr>
<tr><td>110</td><td>0.167</td><td>10.0</td><td>6.6</td><td>5.0</td><td>10.8</td><td>6.0</td><td>3.6</td></tr>
<tr><td>111</td><td>0.1</td><td>16.7</td><td>11.0</td><td>8.3</td><td>18.0</td><td>10.0</td><td>6.0</td></tr>
</table></td></tr>
<tr><td>Vout_Limit_EN</td><td>D[7]</td><td>Vout_Limit_EN1 = 1
Vout_Limit_EN2 = 0
Vout_Limit_EN3 = 0
Vout_Limit_EN4 = 0</td><td>This bit limits the maximum output voltage of each power rail.
D[7] = 0: The maximum output voltage has no limit. It depends on the I²C V_{OUT} setting, maximum duty cycle, or absolute voltage limit.
D[7] = 1: The maximum output voltage is limited to 1.830V (FB pin voltage).</td></tr>
</table>

Mode	D[6]	Mode1 = 1 Mode2 = 1 Mode3 = 1 Mode4 = 1	Selects the mode (auto-PFM/PWM mode or forced PWM mode). D[6] = 0: Auto-PFM/PWM mode D[6] = 1: Forced PWM mode
Current Limit	D[5:4]	Current Limit1 = 10 Current Limit2 = 10 Current Limit3 = 01 Current Limit4 = 01	Sets the current limit of buck 1 to buck 4. D[5:4] = 00: 2A valley current limit for 1A output current application D[5:4] = 01: 3A valley current limit for 2A output current application D[5:4] = 10: 4.2A valley current limit for 3A output current application D[5:4] = 11: 5A valley current limit for 4A peak output current application Note: For buck 3 and buck 4, a 4.2A or 5A valley current limit is not available; D[5:4] = 10 or 11 are both invalid.
Phase Delay Select	D[2:1]	Phase Delay Select1 = 01 Phase Delay Select2 = 10 Phase Delay Select3 = 11 Phase Delay Select4 = 00	Sets the phase delay. 00: 0° delay 01: 90° delay 10: 180° delay 11: 270° delay
VOUT_ OVP_EN	D[3]	VOUT_OVP_ EN1 = 1 VOUT_OVP_ EN2 = 1 VOUT_OVP_ EN3 = 1 VOUT_OVP_ EN4 = 1	Enable bit of buck 1 to buck 4's output over-voltage protection (OVP) function. D[3] = 0: Disable OVP function D[3] = 1: Enable OVP function
VOUT_ DIS_EN	D[0]	VOUT_DIS_ EN1 = 1 VOUT_DIS_ EN2 = 1 VOUT_DIS_ EN3 = 1 VOUT_DIS_ EN4 = 1	Enable bit of buck 1 to buck 4's output discharge function. D[3] = 0: Disable discharge function D[3] = 1: Enable discharge function
Vout_ Select	D[7]	Vout_Select1 = 0 Vout_Select2 = 1 Vout_Select3 = 1 Vout_Select4 = 1	Selects the internal feedback divider ratio. D[7] = 0: The FB voltage is fed directly to the error amplifier. The FB voltage is equal to the reference voltage D[7] = 1: The FB voltage is divided by 1/3, then compared with the reference voltage. The FB voltage is equal to 2 times the reference voltage Note: If the AVS function is used, the D[7] bit will be set at 0.

V_Ref	D[6:0]	V_Ref1 = 1.V V_Ref2 = 3.3V V_Ref3 = 1.800V V_Ref4 = 2.5V	Sets the internal reference voltage, from 550mV to 1.82V, 10mV per step. The voltage slew rate is fixed at 2mV/µs. D[6:0] = 000 0000: 550mV D[6:0] = 000 0001: 560mV ... D[6:0] = 111 1111: 1.82V
EN1, EN2, EN3, EN4	D[7:4]	EN1 = 1 EN2 = 1 EN3 = 1 EN4 = 1	Enable bit of each buck regulator. 1: Enabled 0: Disabled
UVLO	D[2:1]	D[2:1] = 01	Sets the input UVLO threshold of VIN. 00: UVLO rising threshold is 3.5V 01: UVLO rising threshold is 4.5V 10: UVLO rising threshold is 5.8V 11: UVLO rising threshold is 8.5V
OP_BIT	D[0]	D[0] = 0	When the ADD_PG_OP_SYNCOUT bit is set to 10, pin 20 is configured as a GPIO output port. OP_BIT sets the output port as logic high or low. This bit is only valid when ADD_PG_OP_SYNCOUT = 10. 0: Pin 20 pulls low, with certain resistance 1: Pin 20 is an open drain
FREQ	D[7:6]	D[7:6] = 01: 800kHz	Frequency of the buck regulator. The buck 1 to buck 4 switching frequency is always the same; the device cannot support a different frequency from buck 1 to buck 4. D[7:6] = 00: 533kHz D[7:6] = 01: 800kHz D[7:6] = 10: 1060kHz D[7:6] = 11: 1600kHz
Shutdown_ Delay_EN	D[5]	D[5] = 1	The MPM54304 offers two kinds of shutdown sequence when EN goes low. In the first sequence, buck 1 to buck 4 shut down at the same time. In the second sequence, buck 1 to buck 4 shutdown follows the reverse of the power-on sequence. See the Shutdown Sequence section on page 35 for more details. D[5] = 0: Shutdown at the same time D[5] = 1: Shutdown sequence is the reverse of the power-on sequence
I²C SLAVE ADDRESS	D[4:0]	D[4:0] = 01000	Sets the A5 to A1 bits of the slave I²C address. See the I²C Bus Slave Address section on page 30 for more details.
ADD_PG_OP _SYNCOUT	D[7:6]	D[7:6] = 01	Sets pin 20's function. D[7:6] = 00: Pin 20 is configured as an ADD pin, which can set the I²C slave address D[7:6] = 01: Pin 20 is configured as a PG pin, which indicates the buck regulator's power status D[7:6] = 10: Pin 20 is an OP pin (GPIO output port), and works in output mode. This mode is an open-drain structure with logic controlled by the I²C register bit. OP_BIT sets the default status D[7:6] = 11: Pin 20 is configured as SYNC Output. It outputs a clock signal to sync with the downstream device's switching frequency. Open-drain structure

PG_Delay	D[4:2]	D[4:2] = 000	Sets the PG delay timer: 000: 0.2ms 001: 5ms 010: 25ms 011: 75ms 100: 200ms
Parallel_2 (10)	D[1]	0	Sets buck 3 and buck 4 to work in parallel mode. Use FB3 as the feedback pin. Default value is 0. After entering parallel mode, buck 4's I²C/MTP register is invalid. The current limit is double buck 3's register setting. 0: Non-parallel mode 1: Parallel mode
Parallel_1 (10)	D[0]	0	Sets buck 1 and buck 2 to work in parallel mode. Use FB1 as the feedback pin. Default value is 0. After entering parallel mode, Buck 2's I²C/MTP register is invalid. The current limit is double buck 1's register setting. 0: Non-parallel mode 1: Parallel mode

Note:

11) The parallel mode must be programmed before pulling the EN/SYNCI pin to logic high.

V_{REF1} to V_{REF4}, Reference Voltage Truth Table

D[6:0]	V_{REF} (mV)	D[6:0]	V_{REF} (mV)	D[6:0]	V_{REF} (mV)
0000000	550	0101011	980	1010110	1410
0000001	560	0101100	990	1010111	1420
0000010	570	0101101	1000	1011000	1430
0000011	580	0101110	1010	1011001	1440
0000100	590	0101111	1020	1011010	1450
0000101	600	0110000	1030	1011011	1460
0000110	610	0110001	1040	1011100	1470
0000111	620	0110010	1050	1011101	1480
0001000	630	0110011	1060	1011110	1490
0001001	640	0110100	1070	1011111	1500
0001010	650	0110101	1080	1100000	1510
0001011	660	0110110	1090	1100001	1520
0001100	670	0110111	1100	1100010	1530
0001101	680	0111000	1110	1100011	1540
0001110	690	0111001	1120	1100100	1550
0001111	700	0111010	1130	1100101	1560
0010000	710	0111011	1140	1100110	1570
0010001	720	0111100	1150	1100111	1580
0010010	730	0111101	1160	1101000	1590
0010011	740	0111110	1170	1101001	1600
0010100	750	0111111	1180	1101010	1610
0010101	760	1000000	1190	1101011	1620
0010110	770	1000001	1200	1101100	1630
0010111	780	1000010	1210	1101101	1640
0011000	790	1000011	1220	1101110	1650
0011001	800	1000100	1230	1101111	1660
0011010	810	1000101	1240	1110000	1670
0011011	820	1000110	1250	1110001	1680
0011100	830	1000111	1260	1110010	1690
0011101	840	1001000	1270	1110011	1700
0011110	850	1001001	1280	1110100	1710
0011111	860	1001010	1290	1110101	1720
0100000	870	1001011	1300	1110110	1730
0100001	880	1001100	1310	1110111	1740
0100010	890	1001101	1320	1111000	1750
0100011	900	1001110	1330	1111001	1760
0100100	910	1001111	1340	1111010	1770
0100101	920	1010000	1350	1111011	1780
0100110	930	1010001	1360	1111100	1790

0100111	940	1010010	1370	1111101	1800
0101000	950	1010011	1380	1111110	1810
0101001	960	1010100	1390	1111111	1820
0101010	970	1010101	1400		

Output Voltage Setting

FB1 to FB4 are the output voltage feedback pins. The FB pin can be directly connected to the buck output or the resistor divider network to get a higher output voltage.

If connecting FB directly to V_{OUT}, then for buck 1, the I²C bit Vout_Select1 can set FB1 = Ref1 or FB1 = 3 x Ref1. The Ref1 voltage range is 0.55V to 1.82V (see the Reference Voltage Truth Table above). After setting the Vout_Select1 bit to 1, the buck 1 output voltage range becomes 1.65V to 5.46V.

For better load transient response, set V_{REF} to a lower value and use a feedback resistor divider to set the final V_{OUT}. In this case, a feed-forward capacitor can be added to sense the V_{OUT} change more quickly. Figure 5 shows a similar feedback configuration to this operation, but without AVS.

If connecting FBx to the resistor divider network (using buck 1 as an example), the I²C bit Vout_Select1 = 0 can set FB1 to equal Ref1. The Ref1 voltage range is 0.55V to 1.82V (see the Reference Voltage Truth Table above). Calculate the buck 1 output voltage with Equation (1):

$$V_{O1} = \frac{R1+R2}{R2} \times V_{REF1} \quad (1)$$

If using a resistor divider, the AVS function is supported. The direct V_{OUT}-to-FB path should be cut off.

If the AVS function is chosen, set Vout_Select = 0.

During I²C DVS, the voltage change slew rate is 2.6mV/µs when Vout_Select = 0. The slew rate is 7.8mV/µs when Vout_Select = 1.

The Vout_Limit_EN bit can clamp the maximum output voltage to 1.830V (for the FB voltage, blank the Vout_Select bit). The absolute maximum output voltage is limited to 7V or the maximum duty cycle.

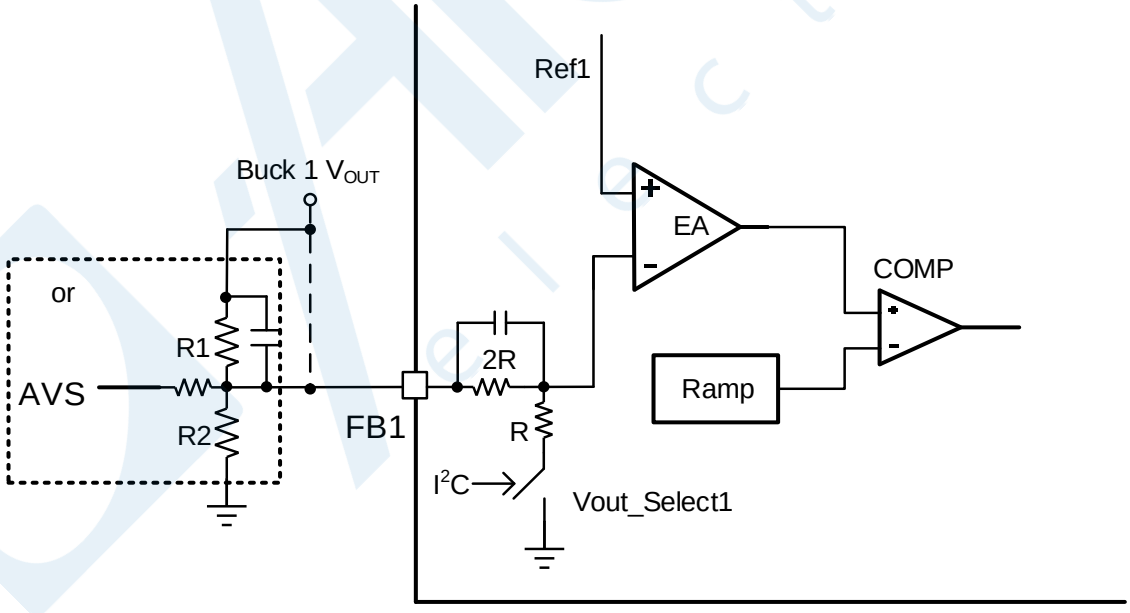


Figure 5: Output Voltage Setting

I²C Register Map

	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck 1	00	R/W			Soft Start Delay1		Additional Phase Delay1	Soft Start Time1		
	01	R/W	Vout_Limit_EN1	Mode1	Current Limit1		VOUT_OVP_EN1	Phase Delay Select1		VOUT_DIS_EN1
	02	R/W	Vout_Select 1	V_Ref1						
Buck 2	03	R/W			Soft Start Delay2		Additional Phase Delay2	Soft Start Time2		
	04	R/W	Vout_Limit_EN2	Mode2	Current Limit2		VOUT_OVP_EN2	Phase Delay Select2		VOUT_DIS_EN2
	05	R/W	Vout_Select 2	V_Ref2						
Buck 3	06	R/W			Soft Start Delay3		Additional Phase Delay3	Soft Start Time3		
	07	R/W	Vout_Limit_EN3	Mode3	Current Limit3		VOUT_OVP_EN3	Phase Delay Select3		VOUT_DIS_EN3
	08	R/W	Vout_Select 3	V_Ref3						
Buck 4	09	R/W			Soft Start Delay4		Additional Phase Delay4	Soft Start Time4		
	0A	R/W	Vout_Limit_EN4	Mode4	Current Limit4		VOUT_OVP_EN4	Phase Delay Select4		VOUT_DIS_EN4
	0B	R/W	Vout_Select 4	V_Ref4						
System	0C	R/W	EN1	EN2	EN3	EN4		UVLO		OP_BIT
System	0D	R/W	FREQ (533kHz/800kHz/ 1.06MHz/1.6MHz)		Shutdown_ Delay_EN	I2C Slave Address				
System	0E	R/W	ADD_PG_OP_SYNCOUT		MTP_ Program	PG_Delay			Parallel_2 (11)	Parallel_1 (11)
System	0F	R/W	MTP configure code. “0x00” means standard MPM54304; “0x01” means MPM54304-0001 part number.							
System	10	R/W	MTP revision number. The customer may need to update the MTP value from time to time, so the revision number is stored here.							
System	11	W	MTP Program Password							
Status	12	R	PG1	PG2	PG3	PG4	OT Warning	OTP		
System	13	R	Vendor ID (1000)				Checksum Flag	Current MTP Page Index		

Note:

12) The parallel_1 and parallel_2 bits only take effect during EN/SYNCI pin turn-on. After EN/SYNCI is turned on, change those bits will not change the parallel mode.

Description of Register Bits

Most of the register bits share the same MTP table description. The sections below only list the description of different register bits.

The I²C register’s default value is determined by the MTP table.

Reset condition of all registers: All I²C registers are reset by the VCC under-voltage lockout

(UVLO). The power-on sequence begins once VIN UVLO is released. An OTP (over-temperature protection) will not reset the I²C register.

1. REG "0x0E" System

Name	Bits	Description
MTP_Program	D[5]	The default value of this bit is 0. Once D[5] is set to 1, the I²C register's data burns to the MTP table. Once the system starts to burn the I²C register's data to the MTP table, the I²C register write operation is locked (NACK). The read operation is not locked until the MTP write operation finishes (typically 100ms). Then the system auto-sets D[5] = 0, and waits for the next MTP burn command. The Current MTP Page Index adds 1 after MTP programming is complete.

2. REG "0x11" System

Name	Bits	Description
MTP Program Password	D[7:0]	To access the MTP_Program bit, the correct password must be entered into this register.

3. REG "0x12" Status

Name	Bits	Description	
PG1	D[7]	Power good indicator for buck 1. 1: Power good 0: Power not good	These bits always reflect the current state of the device.
PG2	D[6]	Power good indicator for buck 2.	
PG3	D[5]	Power good indicator for buck 3.	
PG4	D[4]	Power good indicator for buck 4.	
OT Warning	D[3]	Die temperature early warning bit. When the bit is high, the die temperature is above 120°C.	
OT Protection	D[2]	Over-temperature indication. When this bit is high, the IC is in thermal shutdown.	

4. REG "0x13" System

Name	Bits	Description
Checksum Flag	D[3]	D[3] = 1: The current MTP page has a CRC or checksum error D[3] = 0: The MTP's data passes the CRC check The checksum flag only works after the IC has burned the MTP; otherwise, this bit is always high.
Current MTP Page Index	D[2:0]	D[2:0] stores the current MTP page index information. 000: Default page (there are three pages that can be used) 001: First page 011: Third page

I²C Bus Slave Address

The slave address is 7 bits, followed by an 8th data direction bit (read or write).

There are two ways to program the I²C slave address. The first is to use the external GPIO when it is configured as an ADD pin. The second is to use the I²C/MTP register.

The final slave address is determined by both the ADD pin and the I²C register setting. However, the ADD pin has higher priority, which means it can override the I²C register's setting.

Details on both methods of programming the I²C slave address are described below.

Use the ADD Pin to Set the I²C Slave Address

The GPIO pin is a multi-function pin. It can be configured as ADD, PG, OP, or SYNCOUT

through the I²C or MTP. If pin 26 is configured as an ADD pin, then this pin can be used to program four different slave addresses. A resistor divider from VCC to GND can get an accurate reference voltage. Connect the ADD pin to this reference voltage to set a different I²C address. The internal circuit changes the I²C address accordingly. Table 1 shows the four voltage thresholds for four I²C addresses, and the recommended setting resistor.

Table 1: I²C Slave Address Setting by ADD Voltage

ADD Voltage	ADD Upper Resistor R1 (kΩ)	ADD Lower Resistor R2 (kΩ)	I²C Address	
			Binary	Hex
<18% of V_{CC}	No connect	100	1101 000	68H
33% of V_{CC} to 45% of V_{CC}	500	300	1101 001	69H
56% of V_{CC} to 71% of V_{CC}	300	500	1101 010	6AH
>82% of V_{CC}	100	No connect	1101 011	6BH

Use I²C or MTP to Set the I²C Slave Address

The MPM54304 still offers a programmable I²C slave address via the I²C or MTP.

The I²C register REG0D D[4:0] or MTP REG4D D[4:0] can program A5, A4, A3, A2, and A1 bits (see Table 2).

Table 2: I²C Slave Address Setting by I²C or MTP

	A7	A6	A5	A4	A3	A2	A1
Setting Value	1	1	0 (12)	1 (12)	0 (12)	0 (12)	0 (12)

Note:

13) These bits are programmable by the MTP e-fuse or I²C register.

By default, the slave address is 0x68, A[7:1] = 1101 000.

When the I²C register's slave address bits are changed, the new address takes effect immediately. The I²C master should use the new slave address to continue communication.

POWER CONTROL

State Machine Diagram of Buck Switchers

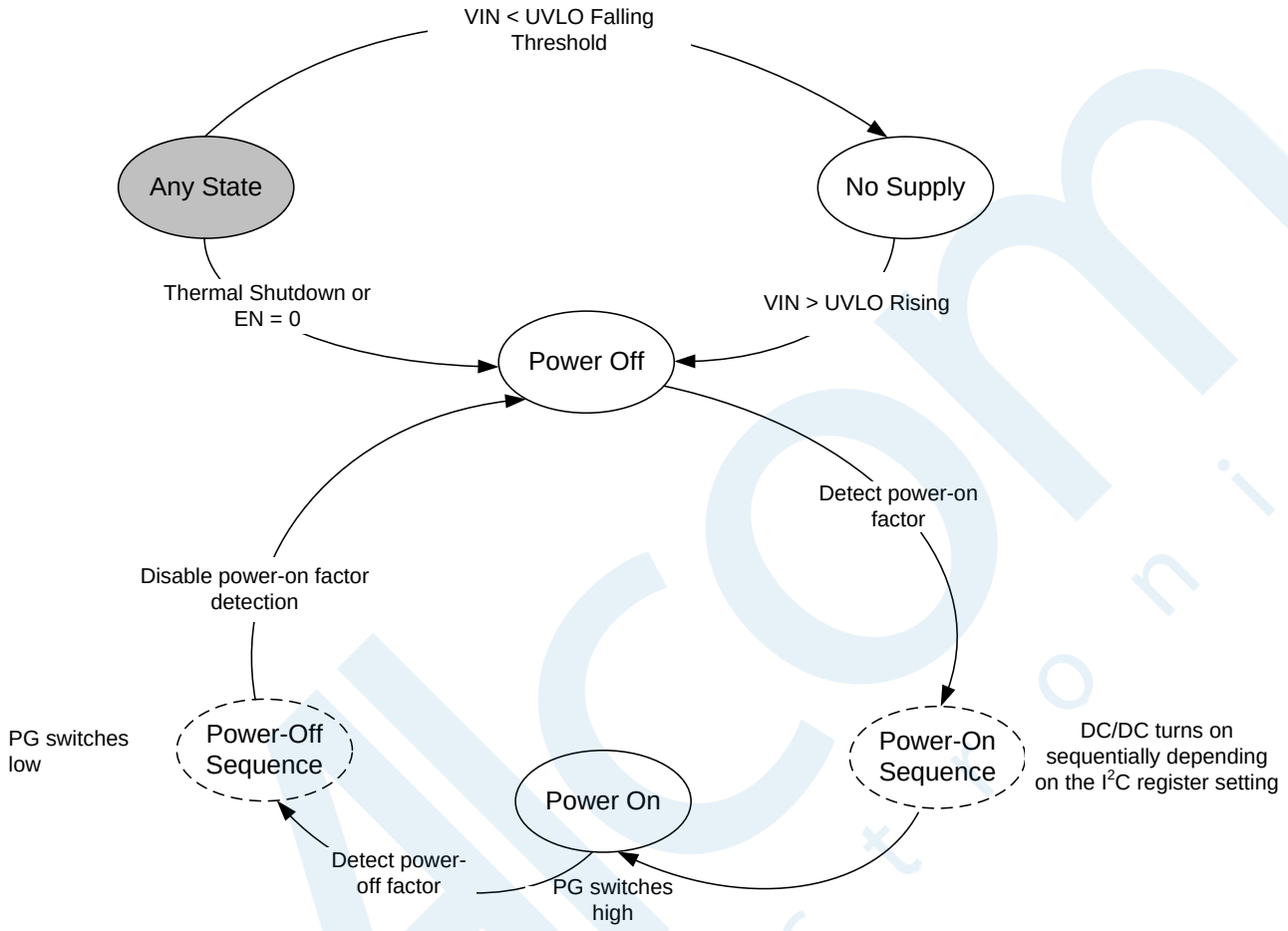


Figure 6: Power Control State Machine Diagram

State Machine Description

The state machine has the following statuses:

Shutdown

The PMIC's EN/SYNCI pin is pulled low. All of the PMIC's switcher functions are disabled, but the I²C and MTP are live as long as the input is above the UVLO threshold.

No Supply

The PMIC's input pin has a UVLO detection circuit. If input voltage VIN is below the UVLO rising threshold, all PMIC functions are disabled.

Power Off

All buck regulators are turned off. In this state, the PMIC is always monitoring the power-on factor. Once a power-on factor is detected, it changes to the power-on sequence state.

Power-On Sequence

Buck 1 to buck 4 turn on sequentially, according to the order programmed by the MTP e-fuse. If a power-off factor is detected during the power-on sequence, the PMIC returns to its power-off state.

Power On

Buck 1 to buck 4 are turned on. The PG output switches high. In this state, the PMIC is always monitoring the power-off factor.

Power-Off Sequence

The PMIC changes to this state when it detects a power-off factor in the power-on state. Buck 1 to buck 4 either turn off sequentially in the reverse order of the power-on sequence, or turn off at the same time, depending on the Shutdown_Delay_EN bit's setting.

Power-On Factors

The PMIC has the following power-on factors:

EN/SYNCI Pin

If the EN/SYNCI pin is pulled high, the system changes from its power-off state to the power-on sequence. The related EN bit determines each buck's on or off state.

Thermal Recovery

The part may be in its power-off state due to the die temperature exceeding the thermal protection threshold. Once the die's temperature decreases, the PMIC enters the power-on sequence again.

Power-On Sequence

There are four slots for power-on sequence timing. All buck regulators can be programmed with 0 to 2 time slots by the MTP e-fuse (see Figure 7).

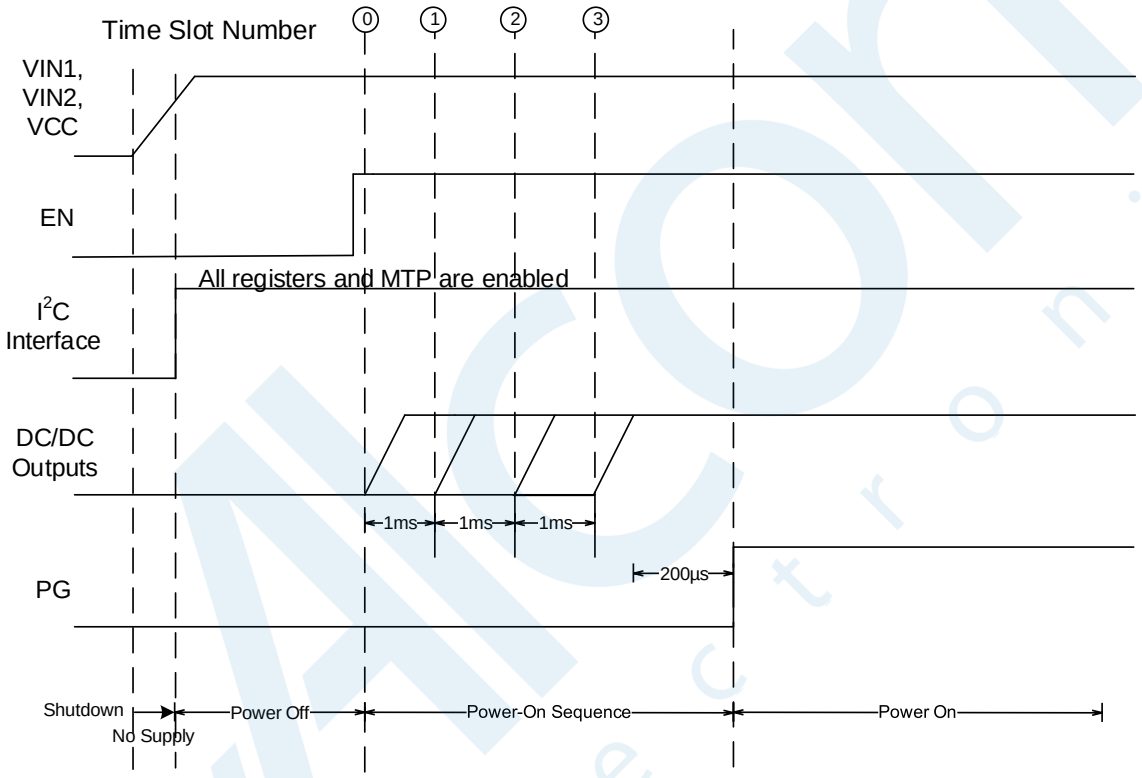


Figure 7: Power-On Sequence

Buck Regulators Turn On

The MPM54304 provides a programmable power-on sequence. The MTP configuration tables on page 42 have bits to set the time slot number (start-up delay timer) for each channel. The default power-on sequence is shown in the default MTP configuration table (see page 42).

Power-Off Factor

EN/SYNCI Pin Hardware-Initiated Power-Off

The MPM54304 supports controlled power-off the through the EN/SYNCI pin. When the EN/SYCNI pin is pulled low, the system enters the power-off sequence.

Power-Off Sequence

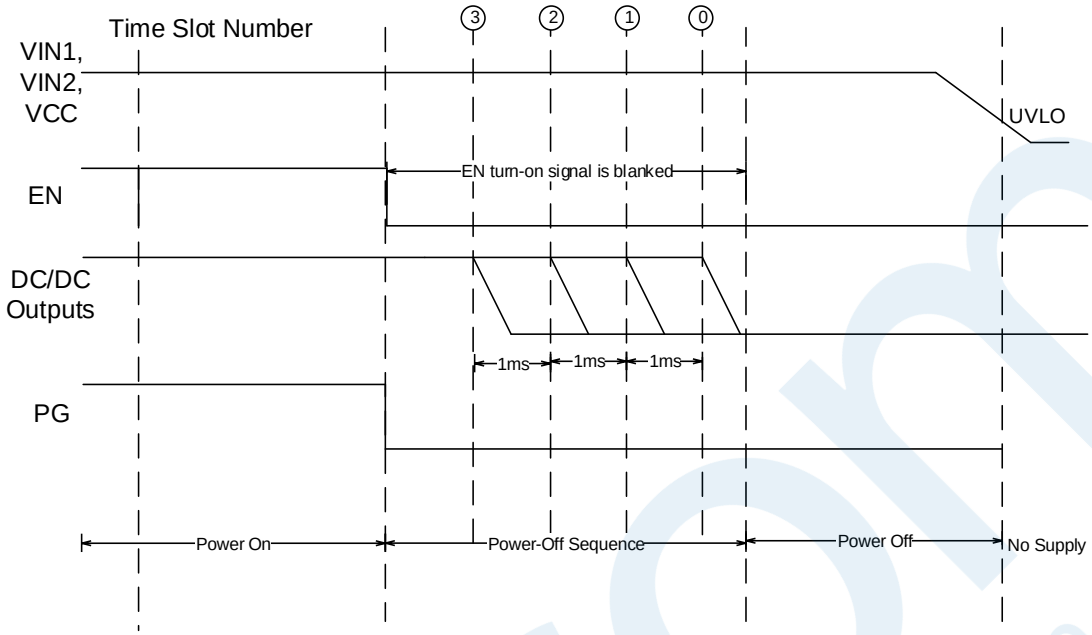


Figure 8: Power-Off Sequence when Shutdown_Delay_EN = 1

PG is pulled low before the device starts to turn off. The DC/DC power-off sequence is in the reverse order of the power-on sequence when Shutdown_Delay_EN is set to 1.

In order to fully discharge the output voltage, the EN signal is blanked during the power-off sequence period. Within this power-off sequence period, the MPM54304 continues working in output discharge mode regardless of whether the external EN/SYNCI pin is pulled high or low.

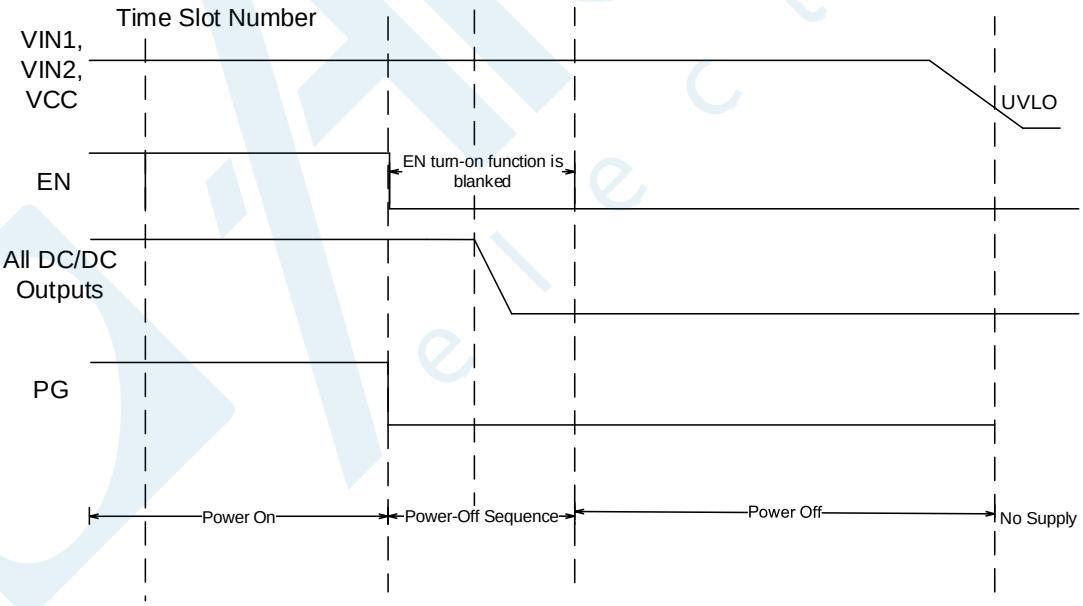


Figure 9: Power-Off Sequence when Shutdown_Delay_EN = 0

All the DC/DC outputs power off at the same time when Shutdown_Delay_EN is set to 0.

Shutdown Sequence

When the input voltage is below the UVLO falling threshold or the IC is over-temperature, the PMIC enters the shutdown sequence immediately. All the DC/DC regulators turn off at the same time (see Figure 10).

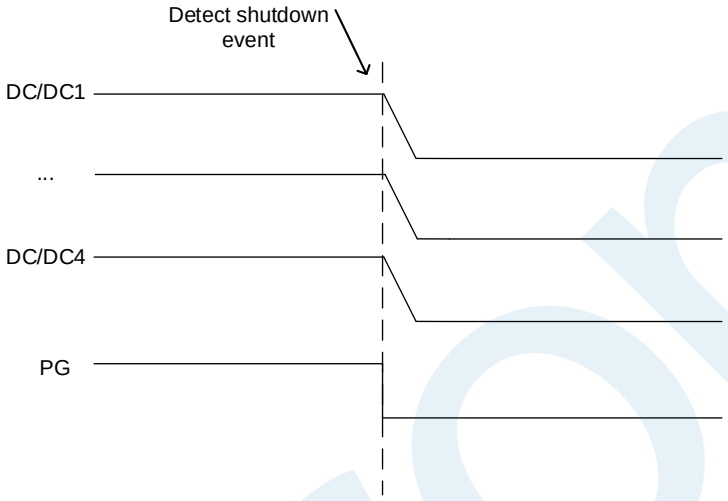


Figure 10: Shutdown Sequence

Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MPM54304 sets the OT WARNING bit to 1.

If the die temperature exceeds 160°C, the system begins the shutdown sequence. When the temperature recovers to 140°C, the regulator begins the power-on sequence again.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM54304 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be instantaneously controlled by the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 11).

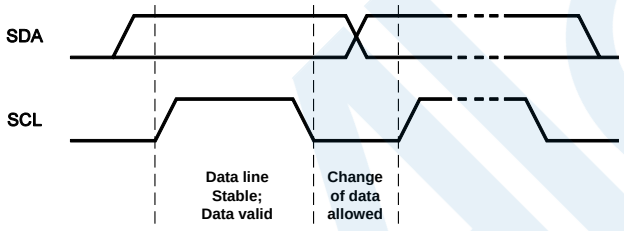


Figure 11: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start condition is defined as the SDA signal transitioning from high to low while the SCL is high. A stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 12).

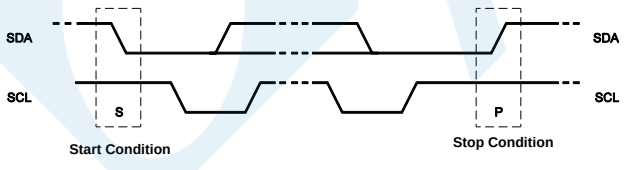


Figure 12: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after a start condition. The bus is considered to be free again a minimum of 4.7µs after a stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start and repeated start conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Figure 13 shows the format that data transfers follow. After the start condition, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.

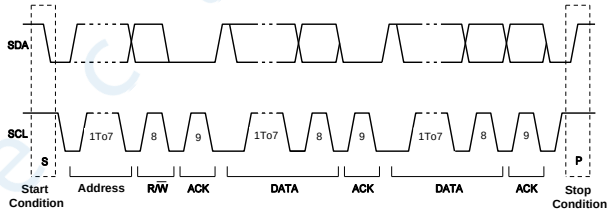


Figure 13: A Complete Data Transfer

The MPM54304 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receipt of each byte, the MPM54304 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPM54304. The MPM54304 then performs an update on the falling edge of the LSB byte.

Figure 14 shows examples of an I²C write and read sequence.

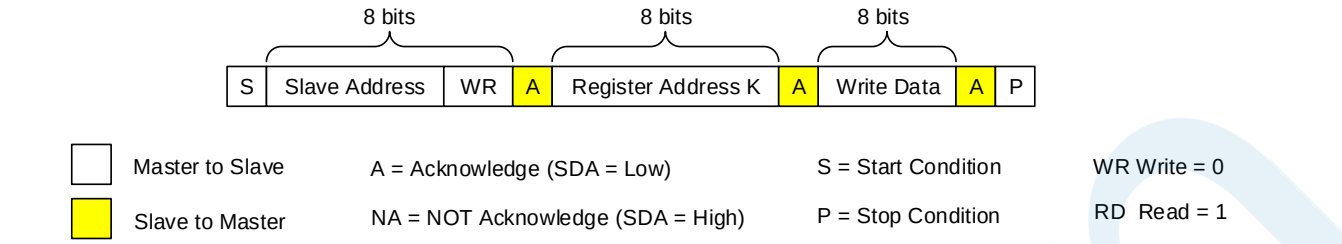


Figure 14a: I²C Write Example – Write Single Register

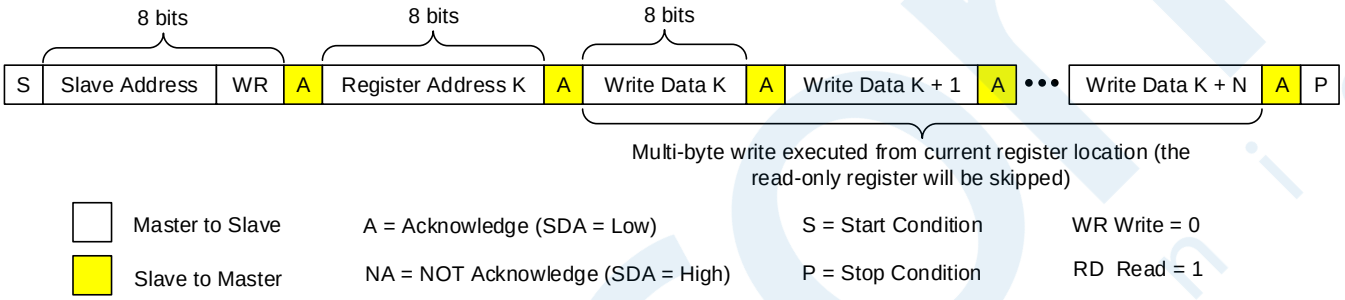


Figure 14b: I²C Write Example – Write Multi-Register

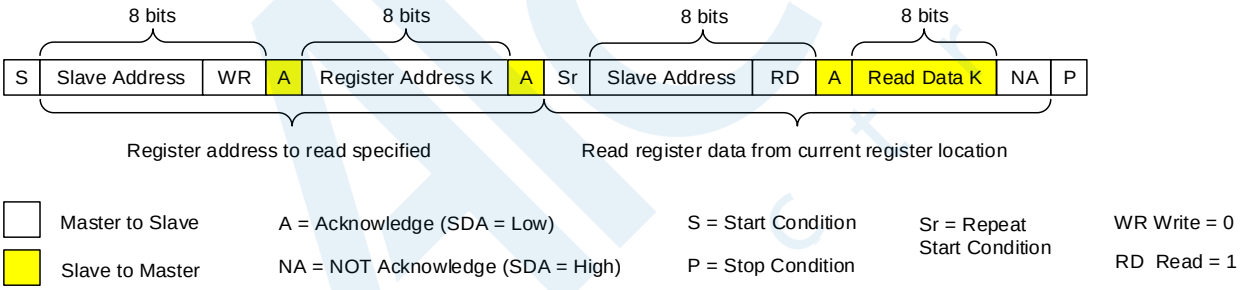


Figure 14c: I²C Read Example – Read Single Register

APPLICATION INFORMATION

Internal Inductor

Fixed inductors in the module are 1µH (channels 1 and 2) and 2.2µH (channels 3 and 4).

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (3):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Step-Down Regulator

Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic

capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation.

PCB Layout Guidelines (13)

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to achieve better thermal performance. For best results, refer to Figure 15 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor as close to the device as possible.
5. Keep the input capacitor and IN as short and wide as possible.
6. Place the VCC capacitor as close to the VCC and GND pins as possible.
7. Connect VIN, VOUT, and GND to a large copper area to improve thermal performance and long-term reliability.
8. Separate the input GND area from other GND areas on the top layer, and connect them together on the internal layers and bottom layer through multiple vias.
9. Ensure there is an integrated GND area on the internal layer or bottom layer.
10. Use multiple vias to connect the power planes to internal layers.

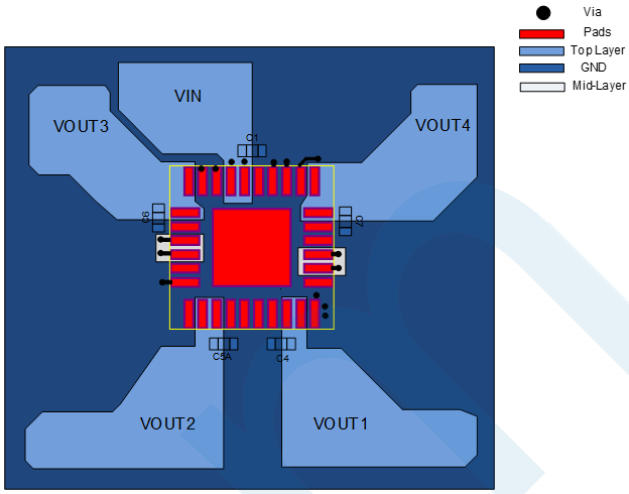


Figure 15: Recommended PCB Layout

Notes:

13) The recommended layout is based on the Typical Application Circuit section on page 40.

TYPICAL APPLICATION CIRCUITS

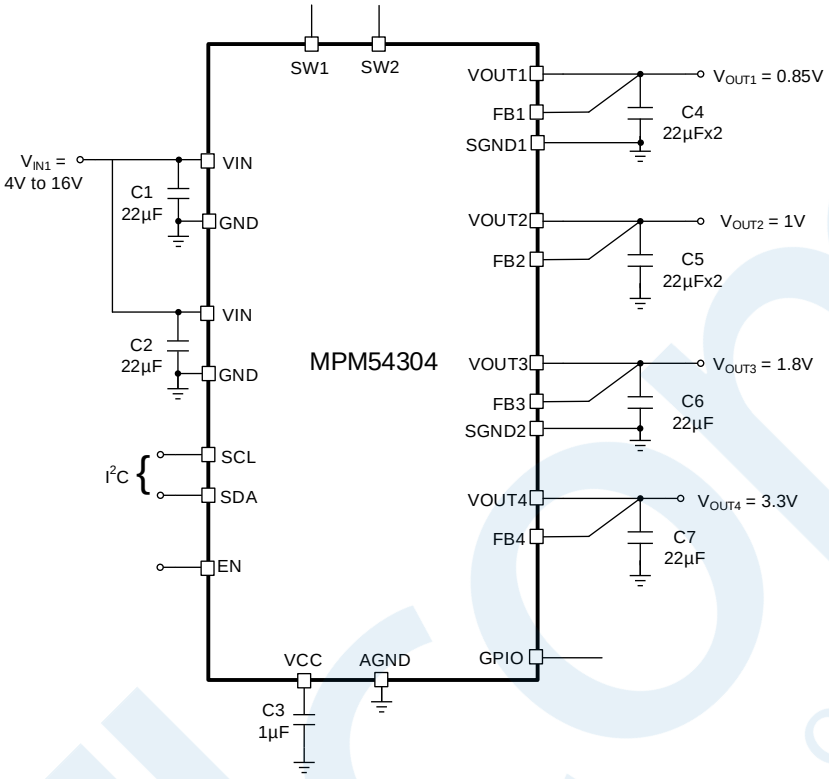


Figure 16: 4V to 16V Input and Quad-Output

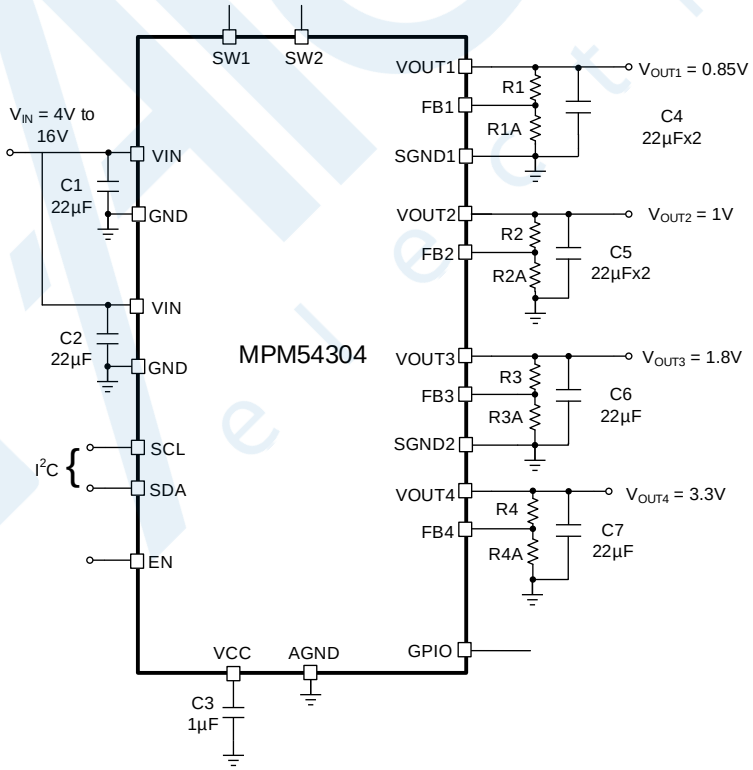


Figure 17: 4V to 16V Input and Quad-Output with External Divider

TYPICAL APPLICATION CIRCUITS *(continued)*

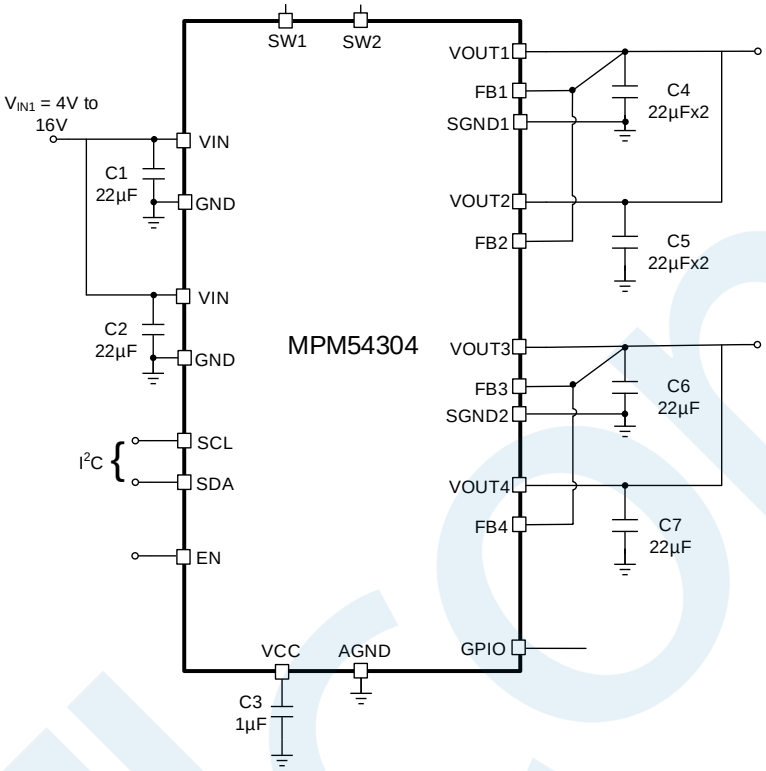


Figure 18: 4V to 16V Input, Dual-Output with Parallel Operation Mode

DEFAULT MTP CONFIGURATION

Table 3: 0000 Suffix Code Configuration

OTP Items	Buck 1	Buck 2	Buck 3	Buck 4
Output Voltage Set Method	I²C	I²C	I²C	I²C
Output Voltage	1V	3.3V	1.8V	1.5V
Initial On/Off	On	On	On	On
Mode	FCCM	FCCM	FCCM	FCCM
Soft-Start Delay Time Slot	0ms	3ms	1ms	2ms
Soft-Start Time (V_O = 0% to 100%)	1ms	1.6ms	1.1ms	0.9ms
Valley Current Limit	4.2A	3A	2A	3A
Buck Output Discharge EN	Enabled	Enabled	Enabled	Enabled
Buck Output Limit EN	Enabled	Disabled	Disabled	Disabled
Buck Parallel Mode Operation	Unparalleled		Unparalleled	
Switching Frequency	800kHz			
VIN UVLO Rising	4.5V			
GPIO	PG			
Shutdown Delay EN	Enabled			
PG Delay Time	0.2ms			
Software Initial I²C Slave Address	0x68			
MTP Configure Code	0x00			

Table 4: 0000 Suffix Code Register Value

Suffix Code	Register	Hex Value
0000	0x40	02h
0000	0x41	EBh
0000	0x42	2Dh
0000	0x43	33h
0000	0x44	5Dh
0000	0x45	B7h
0000	0x46	11h
0000	0x47	4Fh
0000	0x48	7Dh
0000	0x49	21h
0000	0x4A	59h
0000	0x4B	5Fh
0000	0x4C	F3h
0000	0x4D	68h
0000	0x4E	40h
0000	0x4F	00h

Table 5: 0001 Suffix Code Configuration

Suffix Code: 0001				
OTP Items	**Buck 1**	**Buck 2**	**Buck 3**	**Buck 4**
Output Voltage Set Method	External divider	External divider	External divider	External divider
FB Voltage	0.6V	0.6V	0.6V	0.6V
Initial On/Off	On	On	On	On
Mode	FCCM	FCCM	FCCM	FCCM
Soft-Start Delay Time Slot #	0ms	2ms	1ms	3ms
Soft-Start Time (V_O = 0% to 100%)	0.9ms	0.9ms	0.9ms	0.9ms
Valley Current Limit	4.2A	4.2A	3A	3A
Buck Output Discharge EN	Enabled	Enabled	Enabled	Enabled
Buck Output Limit EN	Enabled	Enabled	Disabled	Disabled
Buck Parallel Mode Operation	Unparalleled		Unparalleled	
Switching Frequency	800kHz			
VIN UVLO Rising	4.5V			
GPIO	PG			
Shutdown Delay EN	Enabled			
PG Delay Time	0.2ms			
Software Initial I²C Slave Address	0x68			
MTP Configure Code	0x01			
MTP Revision Number	0x00			

Table 6: 0001 Suffix Code Register Value

Suffix Code	Register	Hex Value
0001	0x40	03h
0001	0x41	EBh
0001	0x42	05h
0001	0x43	23h
0001	0x44	EDh
0001	0x45	05h
0001	0x46	13h
0001	0x47	5Fh
0001	0x48	05h
0001	0x49	33h
0001	0x4A	5Fh
0001	0x4B	05h
0001	0x4C	F3h
0001	0x4D	68h
0001	0x4E	40h
0001	0x4F	01h

Table 7: 0002 Suffix Code Configuration

Suffix Code: 0002				
OTP Items	**Buck 1**	**Buck 2**	**Buck 3**	**Buck 4**
Output Voltage Set Method	External divider	External divider	External divider	External divider
FB Voltage	0.6V	0.6V	0.6V	0.6V
Initial On/Off	On	On	On	On
Mode	FCCM	FCCM	FCCM	FCCM
Soft-Start Delay Time Slot #	0ms	0ms	1ms	3ms
Soft-Start Time (V_O = 0% to 100%)	0.9ms	0.9ms	0.9ms	0.9ms
Valley Current Limit	4.2A	4.2A	3A	3A
Buck Output Discharge EN	Enabled	Enabled	Enabled	Enabled
Buck Output Limit EN	Enabled	Enabled	Disabled	Disabled
Buck Parallel Mode Operation	Paralleled		Unparalleled	
Switching Frequency	800kHz			
VIN UVLO Rising	4.5V			
GPIO	PG			
Shutdown Delay EN	Enabled			
PG Delay Time	0.2ms			
Software Initial I²C Slave Address	0x68			
MTP Configure Code	0x02			
MTP Revision Number	0x00			

Table 8: 0002 Suffix Code Register Value

Suffix Code	Register	Hex Value
0002	0x40	03h
0002	0x41	EBh
0002	0x42	05h
0002	0x43	23h
0002	0x44	EDh
0002	0x45	05h
0002	0x46	13h
0002	0x47	5Fh
0002	0x48	05h
0002	0x49	33h
0002	0x4A	5Fh
0002	0x4B	05h
0002	0x4C	F3h
0002	0x4D	68h
0002	0x4E	41h
0002	0x4F	02h

Table 9: 0003 Suffix Code Configuration

Suffix Code: 0003				
OTP Items	**Buck 1**	**Buck 2**	**Buck 3**	**Buck 4**
Output Voltage Set Method	External divider	External divider	External divider	External divider
FB Voltage	0.6V	0.6V	0.6V	0.6V
Initial On/Off	On	On	On	On
Mode	FCCM	FCCM	FCCM	FCCM
Soft-Start Delay Time Slot #	0ms	2ms	1ms	1ms
Soft-Start Time (V_O = 0% to 100%)	0.9ms	0.9ms	0.9ms	0.9ms
Valley Current Limit	4.2A	4.2A	3A	3A
Buck Output Discharge EN	Enabled	Enabled	Enabled	Enabled
Buck Output Limit EN	Enabled	Enabled	Disabled	Disabled
Buck Parallel Mode Operation	Unparalleled		Paralleled	
Switching Frequency	800kHz			
VIN UVLO Rising	4.5V			
GPIO	PG			
Shutdown Delay EN	Enabled			
PG Delay Time	0.2ms			
Software Initial I²C Slave Address	0x68			
MTP Configure Code	0x03			
MTP Revision Number	0x00			

Table 10: 0003 Suffix Code Register Value

Suffix Code	Register	Hex Value
0003	0x40	03h
0003	0x41	EBh
0003	0x42	05h
0003	0x43	23h
0003	0x44	EDh
0003	0x45	05h
0003	0x46	13h
0003	0x47	5Fh
0003	0x48	05h
0003	0x49	33h
0003	0x4A	5Fh
0003	0x4B	05h
0003	0x4C	F3h
0003	0x4D	68h
0003	0x4E	42h
0003	0x4F	03h

Table 11: 0004 Suffix Code Configuration

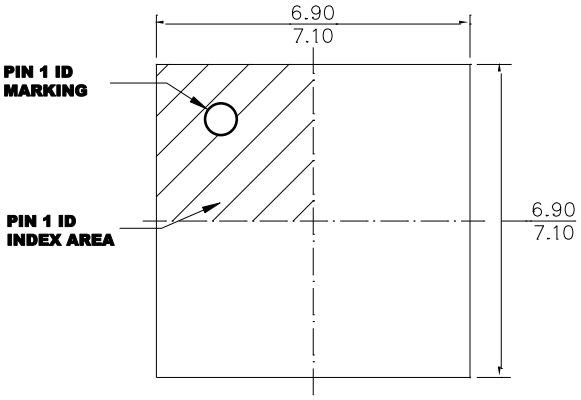
Suffix Code: 0004				
OTP Items	**Buck1**	**Buck2**	**Buck3**	**Buck4**
Output Voltage Set Method	External divider	External divider	External divider	External divider
FB Voltage	0.6V	0.6V	0.6V	0.6V
Initial On/Off	On	On	On	On
Mode	FCCM	FCCM	FCCM	FCCM
Soft-Start Delay Time Slot #	0ms	0ms	1ms	1ms
Soft-Start Time (V_O = 0% to 100%)	0.9ms	0.9ms	0.9ms	0.9ms
Valley Current Limit	4.2A	4.2A	3A	3A
Buck Output Discharge EN	Enabled	Enabled	Enabled	Enabled
Buck Output Limit EN	Enabled	Enabled	Enabled	Disabled
Buck Parallel Mode Operation	Paralleled		Paralleled	
Switching Frequency	800kHz			
VIN UVLO Rising	4.5V			
GPIO	PG			
Shutdown Delay EN	Enabled			
PG Delay Time	0.2ms			
Software Initial I²C Slave Address	0x68			
MTP Configure Code	0x04			
MTP Revision Number	0x00			

Table 12: 0004 Suffix Code Register Value

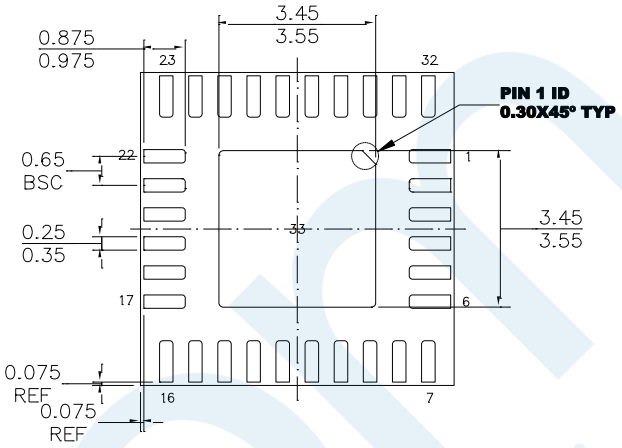
Suffix Code	Register	Hex Value
0004	0x40	03h
0004	0x41	EBh
0004	0x42	05h
0004	0x43	23h
0004	0x44	EDh
0004	0x45	05h
0004	0x46	13h
0004	0x47	5Fh
0004	0x48	05h
0004	0x49	33h
0004	0x4A	5Fh
0004	0x4B	05h
0004	0x4C	F3h
0004	0x4D	68h
0004	0x4E	43h
0004	0x4F	04h

PACKAGE INFORMATION

LGA-33 (7mmx7mm)

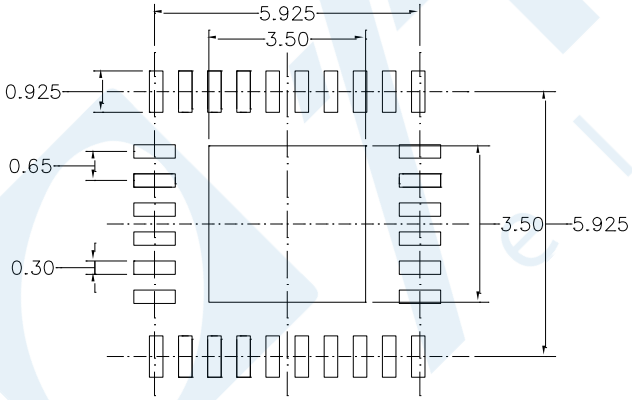


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.