MPM3695-100

16V, 100A, Scalable, DC/DC Power Module with PMBus

DESCRIPTION

The MPM3695-100 is a 100A, scalable, fully integrated power module with a PMBus interface. The device offers a complete power solution that achieves up to 100A of output current, with excellent load and line regulation across a wide input voltage range. The MPM3695-100 operates at a high efficiency across a wide load range, and can be paralleled to deliver up to 800A of current.

By integrating four interleaved phases in a single molded power module, the MPM3695-100 adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control to provide ultra-fast transient response and simple loop compensation. The PMBus interface provides module configurations and monitoring of key parameters.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPM3695-100 requires a minimal number of readily available, external components. It is available in a BGA (15mmx30mmx5.18mm) package.

FEATURES

- 3.2V to 16V Input Voltage Range with External 3.3V VCC Bias
- 4V to 16V Input Voltage Range with Internal VCC Bias
- 0.5V to 3.3V Output Voltage Range
- 100A Continuous Current for Outputs Up to 1.8V
- 60A Continuous Current for 3.3V Output
- Parallelable Up to 800A with Active Curernt Balancing
- Auto-Interleaving for Parallel Operation
- Output Voltage Remote Sensing
- ±1% Reference Voltage Accuracy (-40°C to +125°C)
- PMBus 1.3 Compliant
- Telemetry Readback including V_{IN}, V_{OUT}, I_{OUT}, Temperature, and Faults
- Configurable via the PMBus:
  - Output Voltage
  - Soft-Start Time
  - Over-Current (OC), Over-Temperature (OT), Over-Voltage (OV), Under-Voltage (UV), Under-Voltage Lockout (UVLO) Limits
  - PWM Mode
  - Switching Frequency
- Available in a BGA (15mmx30mmx5.18mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Industrial Equipment
- Servers and Computing
- FPGA and ASIC Core Power

TYPICAL APPLICATION

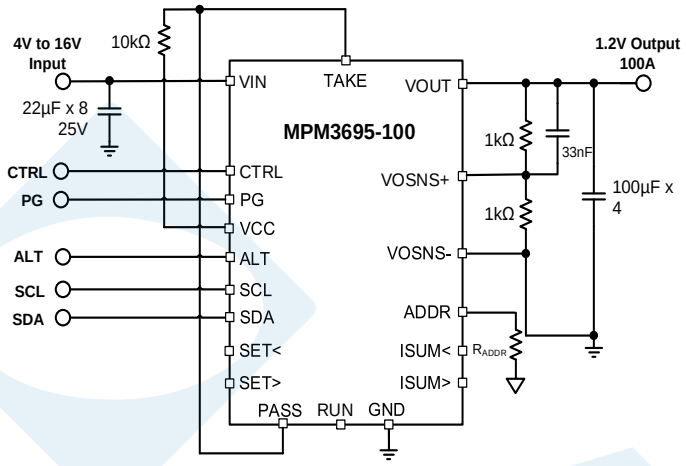
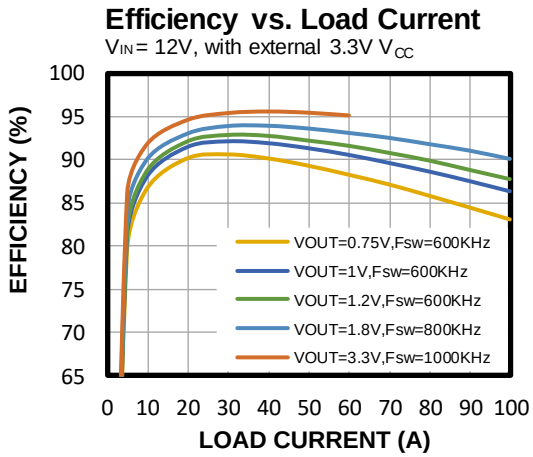


Figure 1: Typical Application Circuit for Single-Module Operation at 1.2V Output



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3695GBH-100-xxxx**	BGA (15mmx30mmx5.18mm)	*See Below*	3
MPM3695GBH-100-0001	BGA (15mmx30mmx5.18mm)	*See Below*	3
EVKT-MPM3695-100A	-	-	-
EVKT-MPM3695-200A	-	-	-
EVKT-MPM3695-400A	-	-	-

* Add –T for tray package (e.g. MPM3695GBH-100-0001–T).

** The 4-digit suffix code “-xxxx” is the configuration identifier for the register settings stored in the non-volatile memory (NVM) of the power module. The default configuration code is “-0001”. For customized configurations, contact an MPS FAE to assign a 4-digit suffix code.

TOP MARKING

MPS YYWW
M3695-100
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
M3695-100: Part number
LLLLLLLLL: Lot number
M: Module

MPM3695-100 EVALUATION KIT

Evaluation kit contents (items listed below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website):

EVKT-MPM3695-100A: Single-Module Operation

#	Part Number	Item	Qty
1	EVM3695-100-BH-00A	MPM3695GBH-100 evaluation board for single-module operation	1
2	EVKT-USBI2C-02	USB to I^2C communication interface device, USB cable, and ribbon cable	1

EVKT-MPM3695-200A: Dual-Module Operation

#	Part Number	Item	Qty
1	EVM3695-100-BH-00B	MPM3695GBH-100 evaluation board for dual-module operation	1
2	EVKT-USBI2C-02	USB to I^2C communication interface device, USB cable, and ribbon cable	1

EVKT-MPM3695-400A: Four-Module Operation

#	Part Number	Item	Qty
1	EVM3695-100-BH-00C	MPM3695GBH-100 evaluation board for four-module operation	1
2	EVKT-USBI2C-02	USB to I²C communication interface device, USB cable, and ribbon cable	1

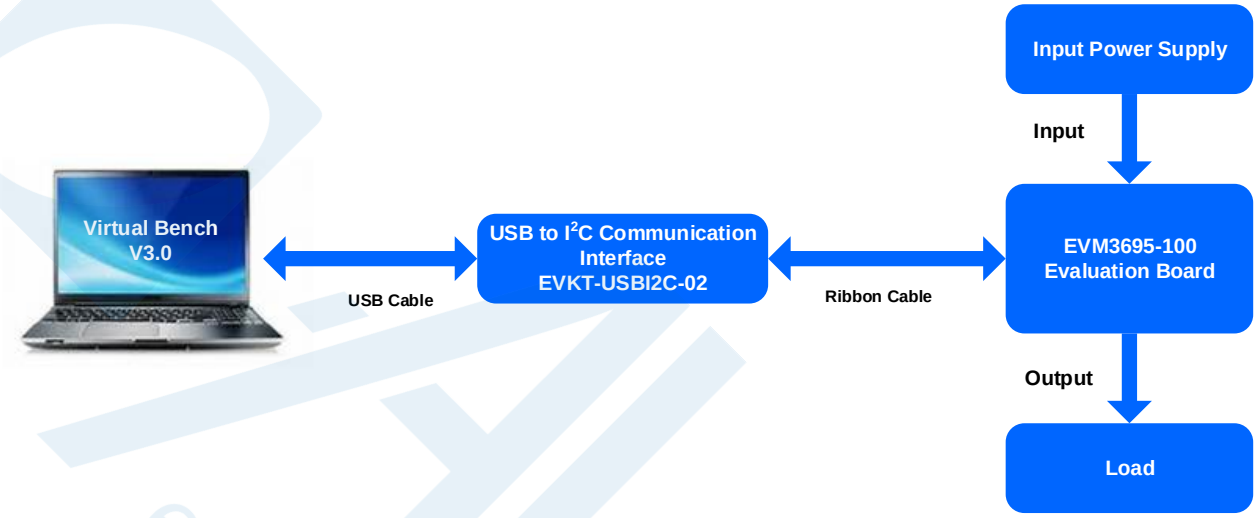
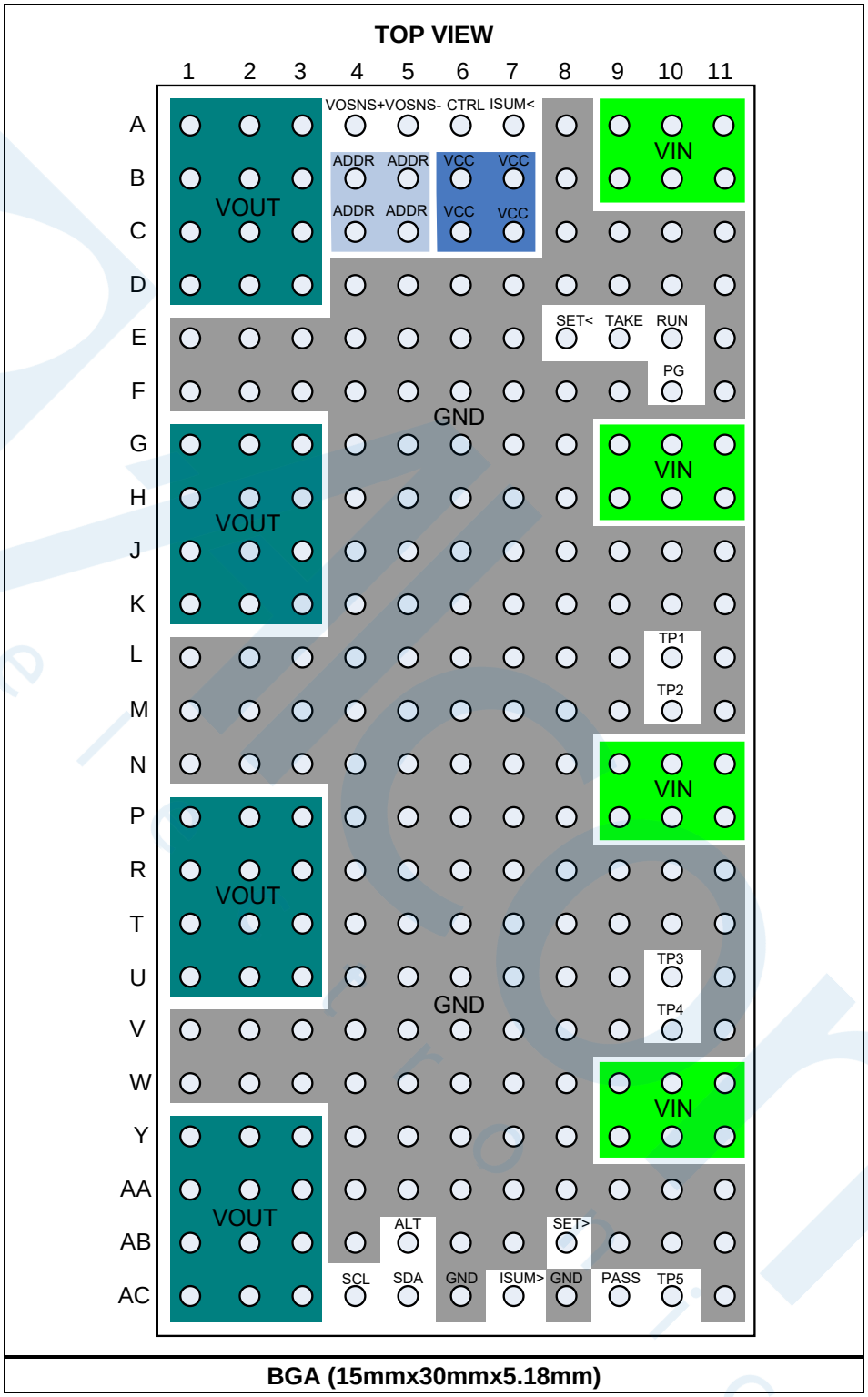


Figure 2: Evaluation Board Set-Up

PACKAGE REFERENCE



BGA (15mmx30mmx5.18mm)

PIN NUMBER LIST

Table 1: Pins A1~E11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VOUT	B1	VOUT	C1	VOUT	D1	VOUT	E1	GND
A2	VOUT	B2	VOUT	C2	VOUT	D2	VOUT	E2	GND
A3	VOUT	B3	VOUT	C3	VOUT	D3	VOUT	E3	GND
A4	VOSNS+	B4	ADDR	C4	ADDR	D4	GND	E4	GND
A5	VOSNS-	B5	ADDR	C5	ADDR	D5	GND	E5	GND
A6	CTRL	B6	VCC	C6	VCC	D6	GND	E6	GND
A7	ISUM<	B7	VCC	C7	VCC	D7	GND	E7	GND
A8	GND	B8	GND	C8	GND	D8	GND	E8	SET<
A9	VIN	B9	VIN	C9	GND	D9	GND	E9	TAKE
A10	VIN	B10	VIN	C10	GND	D10	GND	E10	RUN
A11	VIN	B11	VIN	C11	GND	D11	GND	E11	GND

Table 2: Pins F1~K11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
F1	GND	G1	VOUT	H1	VOUT	J1	VOUT	K1	VOUT
F2	GND	G2	VOUT	H2	VOUT	J2	VOUT	K2	VOUT
F3	GND	G3	VOUT	H3	VOUT	J3	VOUT	K3	VOUT
F4	GND	G4	GND	H4	GND	J4	GND	K4	GND
F5	GND	G5	GND	H5	GND	J5	GND	K5	GND
F6	GND	G6	GND	H6	GND	J6	GND	K6	GND
F7	GND	G7	GND	H7	GND	J7	GND	K7	GND
F8	GND	G8	GND	H8	GND	J8	GND	K8	GND
F9	GND	G9	VIN	H9	VIN	J9	GND	K9	GND
F10	PG	G10	VIN	H10	VIN	J10	GND	K10	GND
F11	GND	G11	VIN	H11	VIN	J11	GND	K11	GND

Table 3: Pins L1~R11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
L1	GND	M1	GND	N1	GND	P1	VOUT	R1	VOUT
L2	GND	M2	GND	N2	GND	P2	VOUT	R2	VOUT
L3	GND	M3	GND	N3	GND	P3	VOUT	R3	VOUT
L4	GND	M4	GND	N4	GND	P4	GND	R4	GND
L5	GND	M5	GND	N5	GND	P5	GND	R5	GND
L6	GND	M6	GND	N6	GND	P6	GND	R6	GND
L7	GND	M7	GND	N7	GND	P7	GND	R7	GND
L8	GND	M8	GND	N8	GND	P8	GND	R8	GND
L9	GND	M9	GND	N9	VIN	P9	VIN	R9	GND
L10	TP1	M10	TP2	N10	VIN	P10	VIN	R10	GND
L11	GND	M11	GND	N11	VIN	P11	VIN	R11	GND

Table 4: Pins T1~Y11

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
T1	VOUT	U1	VOUT	V1	GND	W1	GND	Y1	VOUT
T2	VOUT	U2	VOUT	V2	GND	W2	GND	Y2	VOUT
T3	VOUT	U3	VOUT	V3	GND	W3	GND	Y3	VOUT
T4	GND	U4	GND	V4	GND	W4	GND	Y4	GND
T5	GND	U5	GND	V5	GND	W5	GND	Y5	GND
T6	GND	U6	GND	V6	GND	W6	GND	Y6	GND
T7	GND	U7	GND	V7	GND	W7	GND	Y7	GND
T8	GND	U8	GND	V8	GND	W8	GND	Y8	GND
T9	GND	U9	GND	V9	GND	W9	VIN	Y9	VIN
T10	GND	U10	TP3	V10	TP4	W10	VIN	Y10	VIN
T11	GND	U11	GND	V11	GND	W11	VIN	Y11	VIN

Table 5: Pins AA1~AC11

Pin	Name	Pin	Name	Pin	Name
AA1	VOUT	AB1	VOUT	AC1	VOUT
AA2	VOUT	AB2	VOUT	AC2	VOUT
AA3	VOUT	AB3	VOUT	AC3	VOUT
AA4	GND	AB4	GND	AC4	SCL
AA5	GND	AB5	ALT	AC5	SDA
AA6	GND	AB6	GND	AC6	GND
AA7	GND	AB7	GND	AC7	ISUM>
AA8	GND	AB8	SET>	AC8	GND
AA9	GND	AB9	GND	AC9	PASS
AA10	GND	AB10	GND	AC10	TP5
AA11	GND	AB11	GND	AC11	GND

PIN FUNCTIONS

Name	Description
VIN	**Supply voltage.** This pin provides power to the module. Decoupling capacitors must be connected between VIN and GND.
VOUT	**Module output voltage node.** Connect VOUT to a wide PCB copper plane.
GND	**Power ground.** Connect all GND pins together on a copper plane.
VCC	**Output of the internal 3.3V LDO.** Connect all four VCC pins together for single-phase operation. For parallel operation, connect the VCC pins of the master phase and slave phases together.
CTRL	**Converter control.** CTRL is a digital input that turns the regulator on and off. Drive CTRL high to turn the regulator on; drive CTRL low to turn it off. Do not float this pin. For parallel operation, connect the CTRL pins of the master and slave phases together.
VOSNS-	**Output voltage sense negative return.** Connect this pin directly to the GND sense point of the load. Short VOSNS- to GND if remote sense is not used. For parallel operation, connect the VOSNS- pins of the master and slave phases together.
VOSNS+	**Output voltage sense positive return.** Connect this pin to the output voltage (V_{OUT}) sense positive side to provide a feedback voltage (V_{FB}) to the system. For parallel operation, connect the VOSNS+ pins of the master and slave phases together.
PG	**Multi-purpose power good output.** For the PG pin to pull high and indicate whether V_{OUT} has exceeded 90% of the nominal voltage, a pull-up resistor must be connected to a DC voltage. There is a delay from PG going from low to high. Do not float this pin.
PASS	**Passes trigger signal to the TAKE pin.** Connect the PASS and TAKE pins for single-phase operation. For multi-phase operation, see the Typical Application Circuits section on page 47.
TAKE	**Receives trigger signal from PASS pin or RUN signal.** Pull the TAKE pin of the master phase to 3.3V. Connect the PASS and TAKE pins for single-phase operation. For multi-phase operation, see the Typical Application Circuits section on page 47.
RUN	**Trigger signal for slave phases.** Keep this pin floating for single-phase operation. For multi-phase operation, see the Typical Application Circuits section on page 47.
SET<, SET>	**PWM signal setting.** The SET< and SET> pins are connected internally. Float the SET< and SET> pins for single-module operation. For multi-module operation, connect the SET pins of the master and slave phases together. Use either the SET< or SET> pin to connect to other MPM3695-100 devices
ISUM<, ISUM>	**Reference current output.** The ISUM< and ISUM> pins are connected internally. Float the ISUM< and ISUM> pins for single-module operation. For multi-module operation, connect the ISUM of the master and slave phases together. Use either the ISUM< or ISUM> pin to connect to other MPM3695-100 devices.
SCL	**PMBus serial clock.**
SDA	**PMBus serial data.**
ALT	**PMBus alert.** Open-drain output, active low. A pull-up resistor must be connected from ALT to a 3.3V rail.
ADDR	**PMBus address setting pins.** Connect all four ADDR pins together. Connect a resistor from the ADDR pins to GND to set the device's address. For parallel operation, the same address should be selected for all modules.
TP1~TP5	**Test pins.** Float these pins. Do not connect them.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{OUT} 5.5V
V_{CC} 4.5V
V_{CC} (1s) (2) 6V
All other pins .....-0.3V to +4.3V
All other pins (1s) (2) 6V
Continuous power dissipation (T_A = 25°C) (3) 24.95W
Junction temperature .....170°C
Storage temperature ..... -65°C to +170°C

ESD Ratings

Human body model (HBM) ..... ±1000V
Charged device model (CDM).....±750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4V to 16V
Supply voltage (V_{IN}) (5).....3.2V to 16V
Output voltage (V_{OUT}).....0.5V to 3.3V
External V_{CC} bias .....3V to 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

BGA (15mmx30mmx5.18mm)		
EVM3695-100-BH-00A (6)	5.77	0.74 . °C/W
JESD51-7 (7)	10.3	7.7 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Voltage rating during MTP programming.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
4) The device is not guaranteed to function outside of its operating conditions.
5) An external 3.3V V_{CC} bias is required. Writing to MTP memory is not supported with an external 3.3V V_{CC} bias.
6) Measured on EVM3695-100-BH-00A, 25cmx15cm, 6-layer PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Supply Current						
Shutdown supply current	I_{IN}	V_{CTRL} = 0V		10	16	mA
Input Voltage						
Input voltage range	V_{IN}	Internal VCC	4		16	V
		With external 3.3V V_{CC}	3.2		16	V
Output Voltage (8)						
Output voltage range (8)	V_{OUT_RANGE}		0.5		3.3	V
Load regulation (8)	$V_{OUT\_DC\_LOAD}$	I_{OUT} from 0A to 100A		±0.5%		V_{OUT}
Line regulation (8)	$V_{OUT\_DC\_LINE}$	V_{IN} from 4V to 16V, I_{OUT} = 100A		±0.5%		V_{OUT}
Current Limit						
Individual valley current limit	I_{LIM}	Individual phase current limit; D7h, bits[4:0] = 5b'10010		27		A
Minimum individual valley current limit configurable value (8)		Individual phase current limit		1.5		A
Maximum individual valley current limit configurable value (8)		Individual phase current limit		27		A
Individual low-side negative current limit in OVP	$I_{LIM\_NEG\_OVP}$	Individual phase current limit		-13		A
CTRL						
CTRL on threshold	$CTRL_{ON}$		2.2			V
CTRL off threshold	$CTRL_{OFF}$				1.2	V
Timing and Frequency						
Switching frequency (8)	f_{SW}	Individual phase		600		kHz
Minimum on time (8)	t_{ON_MIN}	f_{SW} = 1000kHz, V_{OUT} = 0.6V		50		ns
Minimum off time (8)	t_{OFF_MIN}	V_{FB} = 480mV		220		ns
Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}	D4h, bits[1:0] = 00	111%	115%	119%	V_{REF}
UVP threshold	V_{UVP}	D9h, bits[3:2] = 10	75%	79%	83%	V_{REF}
Maximum configurable OVP threshold	V_{OVP_MAX}	D4h, bits[1:0] = 11	126%	130%	134%	V_{REF}
Minimum configurable OVP threshold	V_{OVP_MIN}	D4h, bits[1:0] = 00	111%	115%	119%	V_{REF}
Maximum configurable UVP threshold	V_{UVP_MAX}	D9h, bits[3:2] = 11	80%	84%	88%	V_{REF}
Minimum configurable UVP threshold	V_{UVP_MIN}	D9h, bits[3:2] = 00	65%	69%	73%	V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Analog-to-Digital Converter (ADC) (8)						
Voltage range			0		1.28	V
ADC resolution				10		bits
DNL				1		LSB
Sample rate				3		kHz
Digital-to-Analog Converter (DAC) (Feedback Voltage)						
Range (8)		21h, bits[11:0] = 0x0258h; 29h, bits[9:0] = 0x01F4h	450	600	672	mV
Feedback accuracy	V_{FB}	21h, bits[11:0] = 0x0258h; 29h, bits[9:0] = 0x01F4h	594	600	606	mV
Resolution		Per LSB		2		mV
Feedback voltage with margin high (8)	$V_{FB\_MG\_HIGH}$			672		mV
Feedback voltage with margin low (8)	$V_{FB\_MG\_LOW}$			450		mV
Soft Start and Turn-On/Off Delay						
Soft-start time (9)	t_{SS}	61h, bits[2:0] = 3b'001		2		ms
Turn-on delay	t_{ON_DELAY}	60h, bits[7:0] = 0x00h		0		ms
Turn-off delay	t_{OFF_DELAY}	64h, bits[7:0] = 0x00h		0		ms
Error Amplifier						
Feedback current	I_{FB}	V_{FB} = V_{REF} (V_{FB} is the difference between VOSNS+ and VOSNS-)		50	100	nA
Soft Shutdown						
Soft shutdown discharge FET	R_{ON_DISCH}	Individual phase		60		Ω
Under-Voltage Lockout (UVLO)						
VCC UVLO rising threshold	VCC_{VTH}		2.6	2.75	2.9	V
VCC UVLO threshold hysteresis	VCC_{HYS}			250		mV
Minimum configurable input turn-on voltage	$V_{IN\_ON\_MIN}$	V_{CC} = 3.3V	2.65	2.9	3.1	V
Maximum configurable input turn-on voltage	$V_{IN\_ON\_MAX}$		16	16.5	17	V
Minimum configurable input turn-off voltage	$V_{IN\_OFF\_MIN}$	V_{CC} = 3.3V		2.75		V
Maximum configurable input turn-off voltage (8)	$V_{IN\_OFF\_MAX}$			15.75		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG)						
PG high threshold	PG_{VTH_HI}	V_{FB} from low to high; D9h, bits[1:0] = 01		94%		V_{REF}
PG low threshold	PG_{VTH_LO}	V_{FB} from high to low; D9h, bits[3:2] = 10		79%		V_{REF}
PG low-to-high delay	t_{PGTD}	D1h, bits[5:2] = 0000		2		ms
PG sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 3V		1.5		µA
PG low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, T_J = 25°C		600	720	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, T_J = 25°C		700	820	
Thermal Protection (TP)						
TP fault rising threshold (8)	T_{SD_RISE}	4Fh = 0x96h		150		°C
TP fault falling threshold (8)	T_{SD_FALL}	4Fh = 0x96h; D6h, bits[2:1] = 01		125		°C
TP warning rising threshold (8)	T_{WARN_RISE}	51h = 0082h		130		°C
TP warning falling threshold (8)	T_{WARN_FALL}	51h = 0082h; D6h, bits[2:1] = 01		105		°C
Min TP warning temperature (8)	$T_{SD\_WARN\_MIN}$			35		°C
Max TP warning temperature (8)	$T_{SD\_WARN\_MAX}$			160		°C
Monitoring Parameters						
Output voltage monitor accuracy (8)		V_{OUT} = 0.6V	0.588	0.6	0.612	V
Input voltage monitor accuracy			11.76	12	12.24	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
PMBus DC Characteristics (SDA, SCL, ALERT, CTRL) (8)						
Input high voltage	V_{IH}				2.1	V
Input low voltage	V_{IL}		0.8			V
Output low voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALERT = 3.3V	-10		+10	µA
Maximum voltage (SDA, SCL, ALERT, CTRL)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance on SDA, SCL	C_{PIN}				10	pF
PMBus Timing Characteristics (8)						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between a stop and start condition	4.7			µs
Hold time			4.0			µs
Repeated start condition set-up time			4.7			µs
Stop condition set-up time			4.0			µs
Data hold time			300			ns
Data set-up time			250			ns
Clock low timeout			25		35	ms
Clock low period			4.7			µs
Clock high period			4.0		50	µs
Clock/data falling time					300	ns
Clock/data rising time					1000	ns

Notes:

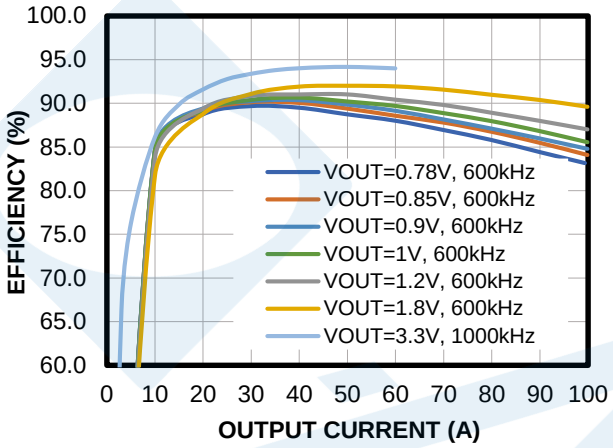
8) Guaranteed by sample characterization.
9) Guaranteed by sample characterization. Not tested in production. The parameter is tested during parameters characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz, T_A = 25°C, unless otherwise noted.

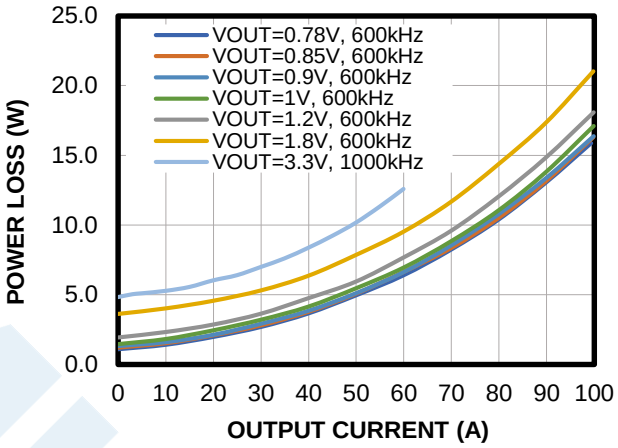
Efficiency vs. Output Current

V_{IN} = 12V, without external 3.3V V_{CC}



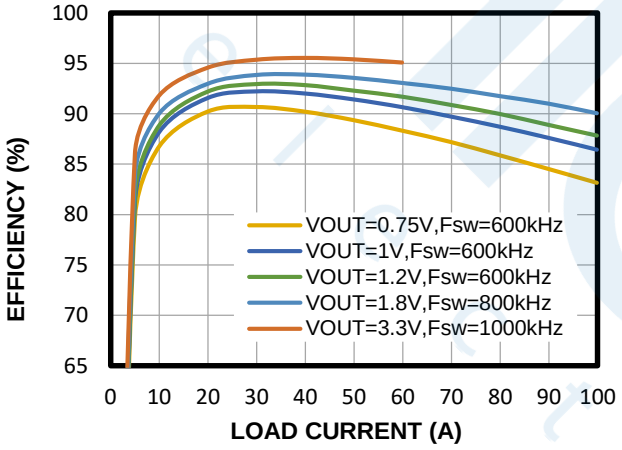
Power Loss vs. Output Current

V_{IN} = 12V, without external 3.3V V_{CC}



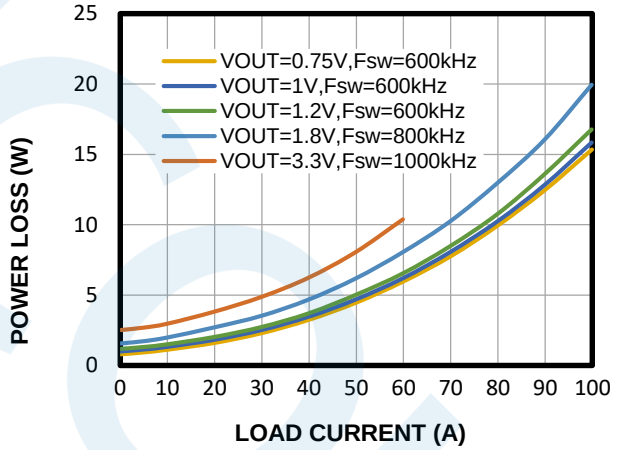
Efficiency vs. Load Current

V_{IN} = 12V, with external 3.3V V_{CC}



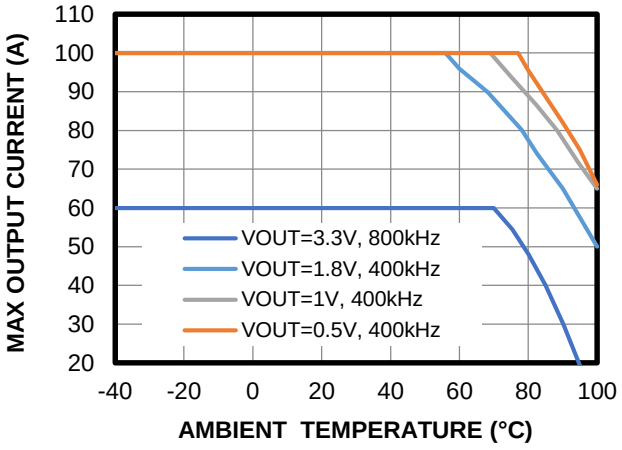
Power Loss vs. Load Current

V_{IN} = 12V, with external 3.3V V_{CC}



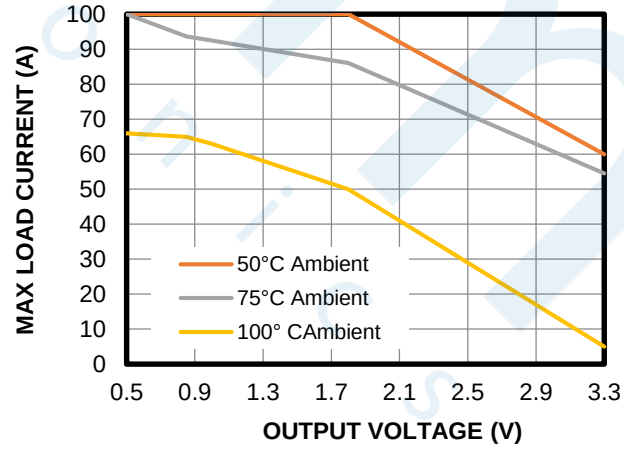
Thermal Derating

V_{IN} = 12V, without airflow and external 3.3V V_{CC}



Output Voltage Derating

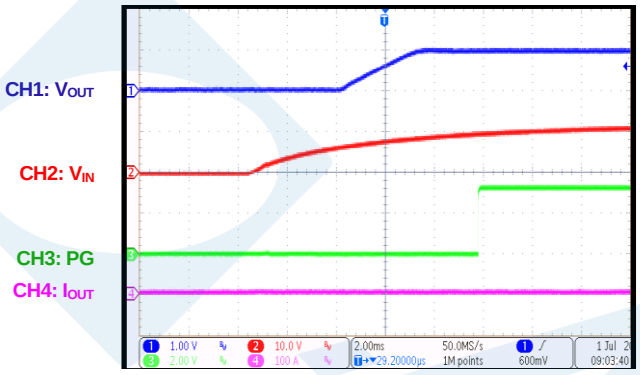
V_{IN} = 12V, without airflow and external 3.3V V_{CC}



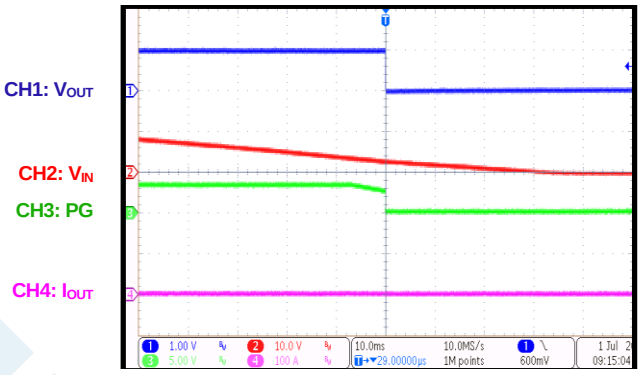
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz, T_A = 25°C, unless otherwise noted.

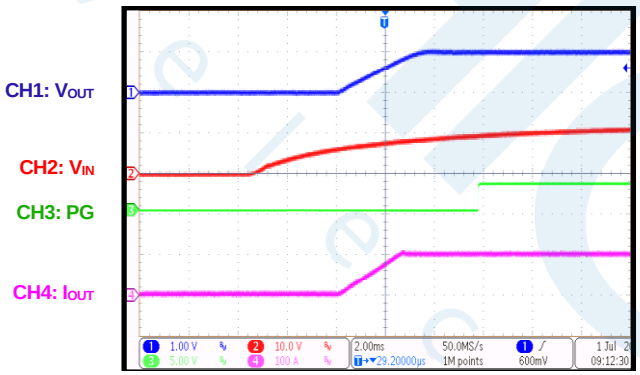
Start-Up through VIN
No load



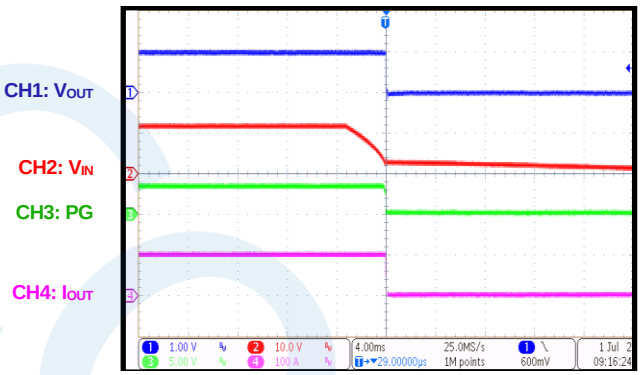
Shutdown through VIN
No load



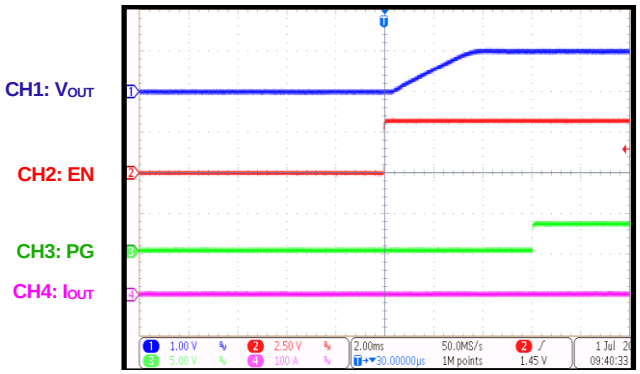
Start-Up through VIN
Full load



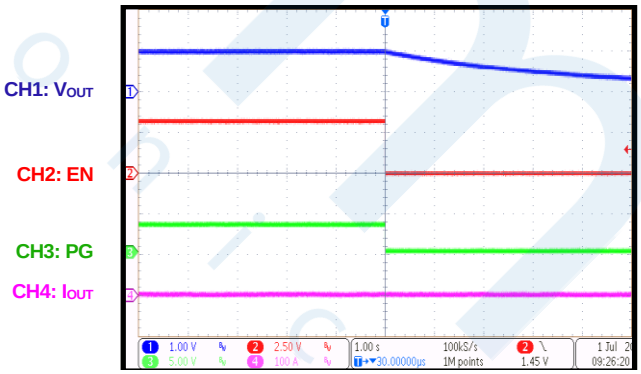
Shutdown through VIN
Full load



Start-Up through EN
No load



Shutdown through EN
No load

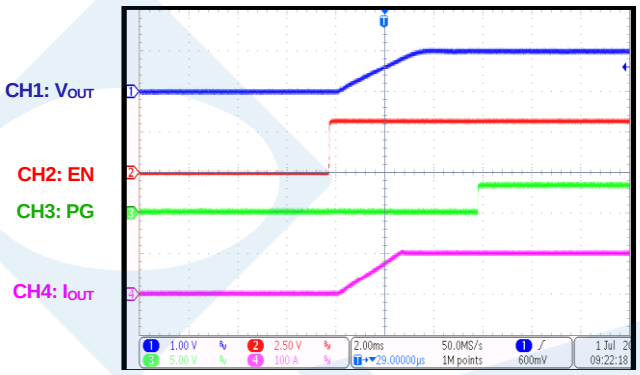


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz, T_A = 25°C, unless otherwise noted.

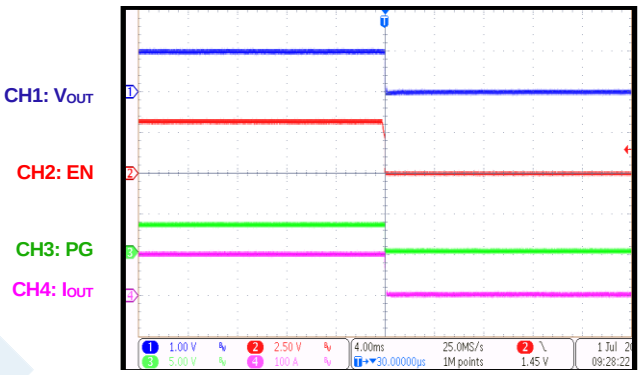
Start-Up through EN

Full load



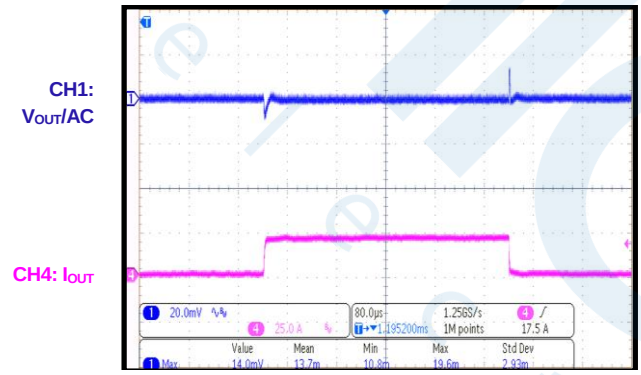
Shutdown through EN

Full load



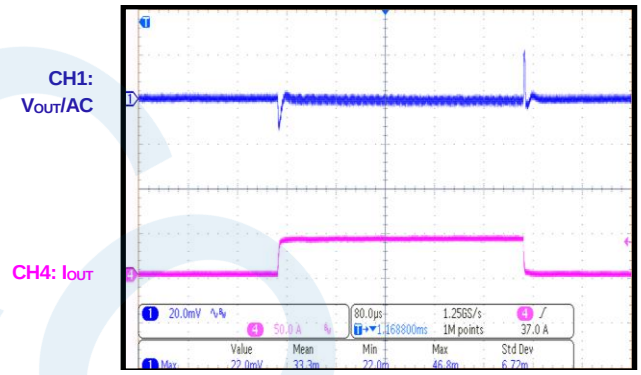
Load Transient, Single-Module Operation

V_{OUT} = 0.78V, 0A to 25A,
C_{OUT} = 20 x 47µF + 5 x 220µF



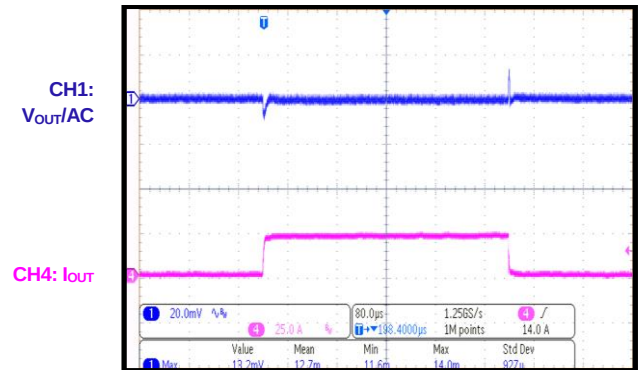
Load Transient, Single-Module Operation

V_{OUT} = 0.78V, 0A to 50A,
C_{OUT} = 20 x 47µF + 5 x 220µF



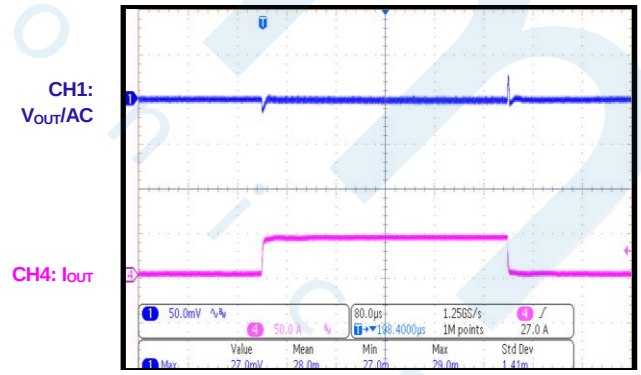
Load Transient, Single-Module Operation

V_{OUT} = 0.9V, 0A to 25A,
C_{OUT} = 20 x 47µF + 4 x 220µF



Load Transient, Single-Module Operation

V_{OUT} = 0.9V, 0A to 50A,
C_{OUT} = 20 x 47µF + 4 x 220µF



FUNCTIONAL BLOCK DIAGRAM

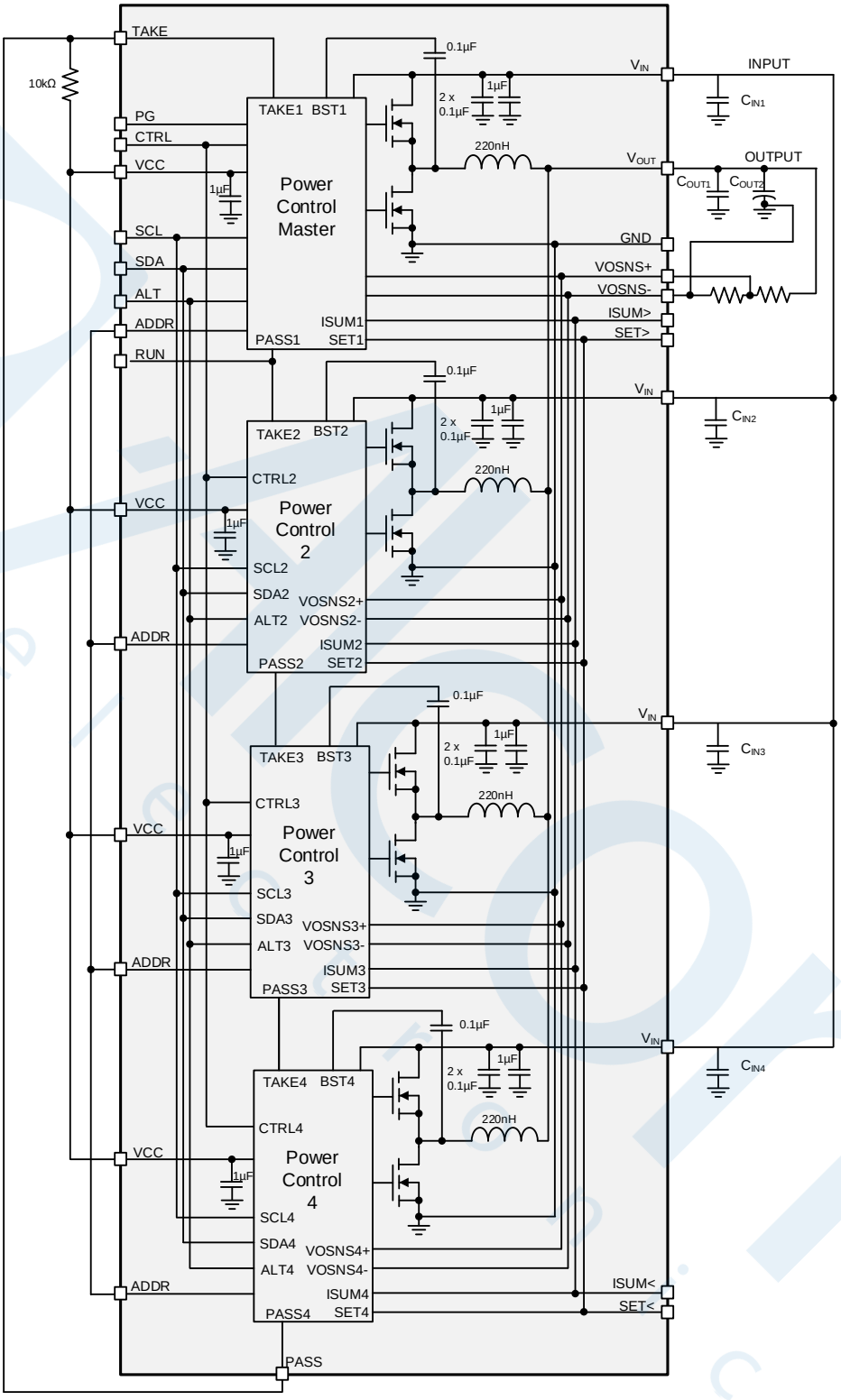


Figure 3: Functional Block Diagram

OPERATION

The MPM3695-100 is a fully integrated power module with up to 100A of continuous output current on a BGA (15mmx30mmx5.18mm) package. For applications that require more than 100A, up to eight MPM3695-100 modules can be connected in parallel to deliver an output current up to 800A. The MPM3695-100 employs multi-phase constant-on-time (MCOT) control to provide fast transient response. Internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

Poly-Phase Architecture

The MPM3695-100 integrates four sets of half-bridges with a power controller in each module. In single-module operation, the four phases are phase-shifted by 90° to minimize the output voltage ripple. One of the internal phases must be configured as the master phase, and the other three phases are slave phases.

MCOT Operation: Master Phase

The master phase performs the following functions:

- Accepts both write and read commands through the PMBus from a host.
- Generates the SET signal.
- Manages start-up, shutdown, and all of the protection functions.
- Monitors fault alerts from the slave phases through the PG pin.
- Generates the first on pulse.
- Generates the on pulse when receiving RUN and SET signals.
- Dynamically adjusts its on time to ensure equal current sharing.
- Generates the PASS signal.

MCOT Operation: Slave Phases

The slave phases perform the following functions:

- Accept write commands through the PMBus from a host.
- Receive SET signal(s) from a master phase.
- Start the on pulse when receiving RUN and SET signals.
- Dynamically adjust their on time to ensure equal current sharing on their own phase based on the per-phase and total current.
- Generate the PASS signal

Parallel Operation

In parallel configuration, one master module and up to seven slave modules are connected in parallel. The output current (I_{OUT}) is shared equally between all MPM3695-100 power modules with active current balancing. The Typical Application Circuits section on page 47 illustrates two and four MPM3695-100s in parallel configuration. In parallel operation, each switching period is divided by up to eight interleaved phases with 45° phase-shifting. For four-module operation, two half-bridges are turned on simultaneously at each PWM pulse. The TAKE pin of the master module must be pulled up to a voltage source through a resistor. The MPM3695-100 detects its master/slave configuration by monitoring the state of the TAKE pin during start-up. The RUN and TAKE pins of all phases are connected in a cascaded manner.

Ramp Compensation

The MPM3695-100 operates with zero-ESR ceramic output capacitors by using internal ramp compensation. A triangular RAMP signal is generated internally, then superimposed onto the FB signal.

The triangular RAMP signal starts to rise once (V_{FB} + RAMP) drops below the reference signal and a SET pulse is generated. The RAMP signal rise time is fixed. The amplitude of the ramp compensation is selectable through register D0h, bits[3:1] to support a wide range of operation configurations.

There is a tradeoff between stability and load transient response. A larger RAMP signal provides better stability but slower load transient response, and vice versa. Optimize ramp compensation selection based on the design criteria for each application (see Table 6 on page 19).

Table 6: Recommended Ramp and Resistor Divider Values

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	R_1 (kΩ)	R_2 (kΩ)	Ramp (mV)	C_{FF} (nF)
12	0.78	600	1	3.3	41	33
12	0.9	600	1	2	41	33
12	1.0	600	1	1.5	41	33
12	1.2	600	1	1	41	33
12	1.8	600	2	1	41	33
12	3.3	1000	4.53	1	41	33

PMBUS INTERFACE

PMBus Serial Interface Description

The Power Management Bus (PMBus) is an open-standard, power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional, serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled up to a bus voltage when they are in an idle state. When connecting to the lines, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM3695-100 is a PMBus slave device that supports both standard mode (100kHz) and fast modes (400kHz and 1000kHz).

Slave Address

A unique address should be set for each slave device that is connected to the same PMBus. The ADDR pin configures the address for the MPM3695-100. There is a 10μA current flowing out of the ADDR pin. Connect a resistor between the ADDR pin and AGND to set the ADDR voltage. The internal analog-to-digital converter (ADC) converts the ADDR pin voltage to set the PMBus address. A maximum of 16 addresses can be set by the ADDR pin. Table 7 lists the PMBus address for different resistor values. MFR_ADDR_PMBUS (D3h) can be used to digitally set the PMBus address.

For multi-phase configuration, the slave phases can share the same address as the master or they can have different addresses, depending on the application requirements. The slave phases can only accept write commands, which means they cannot accept read commands from the PMBus master. However, the master phase can accept both write and read commands from the PMBus master.

Start and Stop Commands

Start and stop commands are signaled by the master device to indicate the beginning and the end of the PMBus transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 4 on page 21).

Table 7: ADDR Resistor vs. PMBus Address

R_{ADDR} (kΩ)	Slave Address
1.24	30h
3.74	31h
6.2	32h
8.2	33h
11.3	34h
13.7	35h
16.2	36h
18.7	37h
21	38h
24	39h
26.1	3Ah
28.7	3Bh
30.9	3Ch
33	3Dh
36	3Eh
39	3Fh

The master then generates the SCL clock signal(s) and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MPM3695-100 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM3695-100 acknowledges this process by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM3695-100. The MPM3695-100 performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus transactions on the MPM3695-100 are done using defined bus protocols. The following protocols can be implemented:

- Send byte with packet error checking (PEC)
- Receive byte with PEC
- Write byte with PEC

- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus Message Format

Figure 5 on page 22 shows the message formats. Unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the MPM3695-100 is driving the bus.

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

A represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the ACK bit for the last byte read is a logic 1, indicated by $\overline{A}$.

Packet Error Checking (PEC)

The MPM3695-100's PMBus interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the MPM3695-100 during a read transaction, or sent by the bus host to the MPM3695-100 during a write transaction.

The PEC byte detects errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MPM3695-100 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MPM3695-100.

PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices with which it can communicate. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins from a number of devices. When the host interrupt occurs, the host issues a message on the bus using the PMBus receive byte, or on the received byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have a PMBus alert signal return their own 7-bit address as the 7MSB of the data byte. The LSB value is not used, and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices have successfully transmitted their addresses.

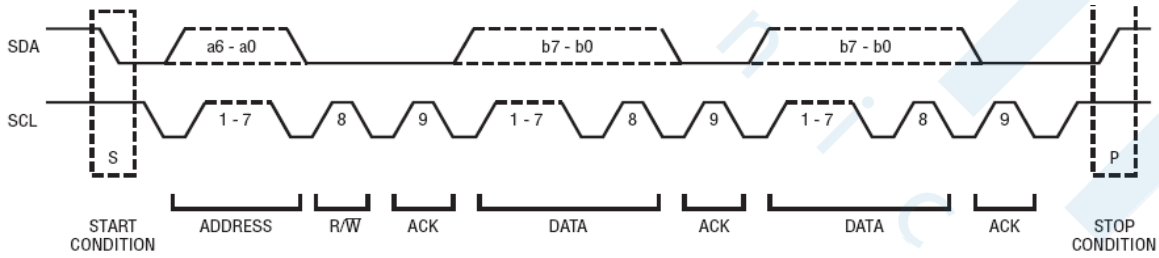


Figure 4: Data Transfer through the PMBus

a) Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	PEC	A	P

b) Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

c) Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P

d) Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

e) Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

f) Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	A	P

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	8	1	1
Data Byte High	A	PEC	A	P

g) Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count = N	A	...

8	1	8	1	...	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	P

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count = N	A	...

8	1	8	1	...	8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	PEC	A	P

Figure 5: PMBus Message Format

Data and Numerical Formats

The MPM3695-100 uses a direct internal format to represent real-world values such as voltage, current, power, and temperature.

All numbers with no suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 5’b01010 indicates a 5-bit binary data where the data is 01010.

The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number with a hexadecimal value of A3.

PMBus Communication Failure

A data transmission fault occurs when data is not properly transferred between the devices. There are several possible data transmission faults:

- Sending too little data
- Reading too little data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus Reporting and Status Monitoring

The MPM3695-100 supports real-time monitoring for some operation parameters and status with PMBus interface (see Table 8).

Table 8: PMBus Monitored Parameters and Statuses

Parameter/Status	PMBus
Output voltage (V_{OUT})	1.25mV/LSB
Output current (I_{OUT})	62.5mA/LSB
Temperature	1°C/LSB
Input voltage (V_{IN})	25mV/LSB
V_{IN} over-voltage (OV)	✓
V_{IN} under-voltage (UV)	✓
V_{IN} OV warning	✓
V_{IN} UV warning	✓
V_{OUT} OV	✓
V_{OUT} UV	✓
Over-temperature (OT)	✓
OT warning	✓
V_{OUT} over-current (OC)	✓
V_{OUT} OC	✓

MTP Programming

The MPM3695-100 has a built-in, multiple-time programmable (MTP) memory to store user configurations. The standard command register STORE_USER_ALL (15h) is not supported by the MPM3695-100. Instead, the MTP cells can be configured using the following command combination:

1. E7h (2000h)
2. E7h (1000h)
3. E7h (4000h)

In the GUI, the above commands are integrated together and named STORE_USER_ALL (15h). This means that MPS’s GUI supports the 15h command.

When the MTP is being configured, the VCC voltage (V_{CC}) may reach as high as 5V. Ensure that VCC is connected to circuits that can withstand this voltage. MTP configuration typically takes about 300ms.

REGISTER MAP

Name	Code	Type	Bytes	Default Value	MTP
OPERATION	01h	R/W with PEC	1	0x80	✓
ON_OFF_CONFIG	02h	R/W with PEC	1	0x1e	✓
CLEAR_FAULTS	03h	Send byte with PEC	0	-	-
WRITE_PROTECT	10h	R/W with PEC	1	0x00	✓
STORE_USER_ALL	15h	Send byte with PEC	0	-	-
RESTORE_USER_ALL	16h	Send byte with PEC	0	-	-
CAPABILITY	19h	R with PEC	1	0xB0	-
VOUT_MODE	20h	R with PEC	1	0x40	-
VOUT_COMMAND	21h	R/W with PEC	2	0x0258 (1.2V)	✓
VOUT_MAX	24h	R/W with PEC	2	0x0BB8 (6V)	✓
VOUT_MARGIN_HIGH	25h	R/W with PEC	2	0x02A0 (1.344V)	✓
VOUT_MARGIN_LOW	26h	R/W with PEC	2	0x01FE (1.02V)	✓
VOUT_SCALE_LOOP	29h	R/W with PEC	2	0x01F4 (0.5)	✓
VOUT_MIN	2Bh	R/W with PEC	2	0x00FA (0.5V)	✓
VIN_ON	35h	R/W with PEC	2	0x0010 (4V)	✓
VIN_OFF	36h	R/W with PEC	2	0x000B (2.75V)	✓
OT_FAULT_LIMIT	4Fh	R/W with PEC	2	0x00A0(160°C)	✓
OT_WARN_LIMIT	51h	R/W with PEC	2	0x008C (140°C)	✓
VIN_OV_FAULT_LIMIT	55h	R/W with PEC	2	0x0024 (18V)	✓
VIN_OV_WARN_LIMIT	57h	R/W with PEC	2	0x0022 (17V)	✓
VIN_UV_WARN_LIMIT	58h	R/W with PEC	2	0x0001 (0.25V)	✓
TON_DELAY	60h	R/W with PEC	2	0x0000 (0ms)	✓
TON_RISE	61h	R/W with PEC	2	0x0002 (4ms)	✓
TOFF_DELAY	64h	R/W with PEC	2	0x0000 (0ms)	✓
STATUS_BYTE	78h	R with PEC	1	-	-
STATUS_WORD	79h	R with PEC	2	-	-
STATUS_VOUT	7Ah	R with PEC	1	-	-
STATUS_IOUT	7Bh	R with PEC	1	-	-
STATUS_INPUT	7Ch	R with PEC	1	-	-
STATUS_TEMPERATURE	7Dh	R with PEC	1	-	-
STATUS_CML	7Eh	R with PEC	1	-	-
READ_VIN	88h	R with PEC	2	-	-
READ_VOUT	8Bh	R with PEC	2	-	-
READ_IOUT	8Ch	R with PEC	2	-	-
READ_TEMPERATURE_1	8Dh	R with PEC	2	-	-
MFR_CTRL_COMP	D0h	R/W with PEC	1	0x0D	✓
MFR_CTRL_VOUT	D1h	R/W with PEC	1	0x00	✓
MFR_CTRL_OPS	D2h	R/W with PEC	1	0x03	✓
MFR_ADDR_PMBUS	D3h	R/W with PEC	1	0x30	✓
MFR_VOUT_FAULT_LIMIT	D4h	R/W with PEC	1	0x03	✓
MFR_OVP_NOCP_SET	D5h	R/W with PEC	1	0x02	✓
MFR_OT_OC_SET	D6h	R/W with PEC	1	0x09	✓
MFR_OC_PHASE_LIMIT	D7h	R/W with PEC	1	0x11 (102A total, 25.5A per phase)	✓
MFR_PGOOD_ON_OFF_LIMIT	D9h	R/W with PEC	1	0x00	✓
MFR_VOUT_STEP	DAh	R/W with PEC	1	0x04	✓
MFR_CTRL	EAh	R/W with PEC	2	0xE8	✓

Note:

10) For manufacturer use. Write-only.

OPERATION (01h)

The OPERATION command is a paged register. This command turns the converter output on and off in conjunction with input from the CTRL pin. It also sets V_{OUT} to the upper or lower margin voltages. The device remains in the commanded operating mode until a subsequent OPERATION command (or a change in the state of the CTRL pin) instructs the converter to change to another mode.

This command can re-enable the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown does not clear the fault registers.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Function							X	
Default Value	1	0	0	0	0	0	0	0

Bits[7:6]	Bits[5:4]	Bits[3:2]	Bits[1:0]	On/Off	Margin State	01h
00	xx	xx	xx	Immediate off	N/A	0x00
01	xx	xx	xx	Soft shutdown	N/A	0x60
10	00	xx	xx	On	Off	0x80
10	01	01	xx	On	Margin low (ignore fault)	0x94
10	01	10	xx	On	Margin low (act on fault)	0x98
10	10	01	xx	On	Margin high (ignore fault)	0xA4
10	10	10	xx	On	Margin high (act on fault)	0xA8

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of the CTRL pin input and PMBus commands required to turn the converter on and off. This includes how the converter responds when V_{IN} is applied.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R/W	R/W	R/W	R/W	R
Function	X			ON	OP	CTRL	POL_CTRL	DELAY
Default value	0	0	0	1	1	1	1	0

ON

The ON bit sets the default to either operate whenever V_{IN} is present, or for the on/off operation to be controlled by the CTRL pin and PMBus commands.

Bit[4] Value	Description
0	The converter starts up any time V_{IN} is present, regardless of the state of the CTRL pin.
1	The converter does not start up unless commanded by the CTRL pin and OPERATION command (as configured in bits[3:0]).

OP

The OP bit controls how the converter responds to OPERATION commands.

Bit[3] Value	Description
0	The converter ignores the ON bit in the OPERATION command from the PMBus.
1	The converter responds to the ON bit in the OPERATION command from the PMBus.

CTRL

The CTRL bit controls how the converter responds to the CTRL pin.

Bit[2] Value	Description
0	The converter ignores the CTRL pin (the device turning on and off is only controlled by the OPERATION command).
1	The converter requires the CTRL pin to be asserted to start up. Depending on bit[3] (OP), the OPERATION command may also be required to instruct the converter to start up.

POL_CTRL

The POL_CTRL bit sets the polarity of the CTRL pin. This function is disabled.

Bit[1] Value	Description
0	Active low (pull the CTRL pin low to start the converter).
1	Active high (pull the CTRL pin high to start the converter).

DELAY

The DELAY bit sets the shutdown action when the converter is commanded off through the PMBus. This bit is read-only and cannot be modified by the end user.

Bit[0] Value	Description
0	TOFF_DELAY, TOFF_FALL.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command resets all stored warning and fault flags. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared, or may be reasserted almost immediately. Issuing a CLEAR_FAULTS command does not cause the converter to restart in the event of a fault shutdown. To restart the device, issue an OPERATION on command after the fault condition is cleared. This command uses the PMBus to send the byte protocol.

WRITE PROTECT (10h)

The WRITE_PROTECT command controls writing to the converter. The provides protection against accidental changes.

All supported commands (registers) may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits[7:0] Value								Description
0	0	0	0	0	0	0	0	Enables writes to all registers.
0	0	1	0	0	0	0	0	Disables all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND registers.
0	1	0	0	0	0	0	0	Disables all writes except to the WRITE_PROTECT, OPERATION, and PAGE registers.
1	0	0	0	0	0	0	0	Disables all writes except to the WRITE_PROTECT register.

When 10h is set to a value other than 0x00 to configure the MTP, register 15h can only be set through MPS's GUI. The MTP's E7h command cannot be used. For more details, see the MTP Programming section on page 23.

The default value for this register is 0x00.

STORE_USER_ALL (15h)

The STORE_USER_ALL command writes the data from the registers to the internal MTP(s). This occurs when the MPM3695-100 receives a STORE_USER_ALL command from the PMBus interface. The MPM3695-100 does not support the 15h command via the MTP. However, the device can accept the 15h command from MPS's GUI. For more details, see the MTP Programming section on page 23.

The following registers can be stored using STORE_USER_ALL:

- OPERATION (01h)
- ON_OFF_CONFIG (02h)
- WRITE_PROTECT (10h)
- VOUT_COMMAND (21h)
- VOUT_MAX (24h)
- VOUT_MARGIN_HIGH (25h)
- VOUT_MARGIN_LOW (26h)
- VOUT_SCALE_LOOP (29h)
- VOUT_MIN (2Bh)
- VIN_ON (35h)
- VIN_OFF (36h)
- OT_FAULT_LIMIT (4Fh)
- OT_WARN_LIMIT (51h)
- VIN_OV_FAULT_LIMIT (55h)
- VIN_OV_WARN_LIMIT (57h)
- VIN_UV_WARN_LIMIT (58h)
- TON_DELAY (60h)
- TON_RISE (61h)
- TOFF_DELAY (64h)
- MFR_CTRL_COMP (D0h)
- MFR_CTRL_VOUT (D1h)
- MFR_CTRL_OPS (D2h)
- MFR_ADDR_PMBUS (D3h)
- MFR_VOUT_FAULT_LIMIT (D4h)
- MFR_OVP_NOCP_SET (D5h)
- MFR_OT_OC_SET (D6h)
- MFR_OC_PHASE_LIMIT (D7h)
- MFR_PGOOD_ON_OFF_LIMIT (D9h)
- MFR_VOUT_STEP (DAh)
- MFR_CTRL (EAh)

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPM3695-100 to copy the entire contents of the MTP to the matching locations in the registers. The values in the registers are overwritten by the values retrieved from the MTP. Any items in the MTP that do not have matching locations in the operating memory are ignored.

This command can be used while the MPM3695-100 is operating, but the device may be unresponsive.

This command is write-only.

CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus functions supported by the MPM3695-100. This command is read with the PMBus read byte protocol.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PEC	MAX_BUS_SPEED		ALERT	X			
Default Value	1	0	1	1	0	0	0	0
Details	PEC supported, max speed 1MHz, supports PMBus alert and ARA							

Bits[6:5] Value		Meaning
0	0	The maximum supported bus speed is 100kHz.
0	1	The maximum supported bus speed is 1MHz.
1	0	The maximum supported bus speed is 400kHz.
1	1	Reserved.

The default value for this register is 0xB0.

VOUT_MODE (20h)

The VOUT_MODE command reads and commands V_{OUT}. The 3MSB are used to determine the data format (only direct format is supported), and the remaining 5 bits represent the exponent used in the V_{OUT} read/write commands.

The default value for this register is 0x40.

VOUT_COMMAND (21h)

The VOUT_COMMAND command sets V_{OUT}. To calculate the feedback reference voltage, multiply VOUT_COMMAND by VOUT_SCALE_LOOP.

For more details, see the Setting the Output Voltage section on page 43.

Command	VOUT_COMMAND															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default Value	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

The value is unsigned and 1LSB = 2mV. The default value of 21h is 1.2V, meaning the default value of this register is 0x0258.

VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on V_{OUT}, regardless of any other commands or combinations. VOUT_MAX provides a safeguard against the user accidentally setting V_{OUT} too high. It does not replace over-voltage protection (OVP).

Command	VOUT_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default Value	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

If an attempt is made to set V_{OUT} to a level that exceeds VOUT_MAX, the device takes the following actions:

1. The commanded V_{OUT} is set to VOUT_MAX.
2. The VOUT bit is set in STATUS_WORD.
3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.
4. The device notifies the host.

The value is unsigned and 1LSB = 2mV. The maximum value of VOUT_MAX is 6V, and the default value is 6V. The default value of this register is 0x0BB8h.

VOUT_MARGIN_HIGH (25h)

Command	VOUT_MARGIN_HIGH															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default Value	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

The value is unsigned and 1LSB = 2mV. The default value is 1.344V, meaning the default value of this register is 0x02A0.

VOUT_MARGIN_LOW (26h)

Command	VOUT_MARGIN_LOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0

The value is unsigned and 1LSB = 2mV. The default value is 1.02V, meaning the default value of this register is 0x1fe.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP sets the feedback resistor divider ratio, which is equal to (V_{OSNS+} - V_{OSNS-}) / V_{OUT}. This command should match the actual value of the feedback resistor divider, regardless of whether it is an external or internal feedback resistor divider.

Command	VOUT_SCALE_LOOP															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X						0.001/LSB									
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

The value is unsigned and 1LSB = 0.001. The default value is 0.5, meaning the default value of this register is 0x01F4.

VOUT_MIN (2Bh)

The VOUT_MIN command sets a lower limit on the converter's V_{OUT}, regardless of any other commands or combinations. VOUT_MIN provides a safeguard against a user accidentally setting V_{OUT} too low. It does not replace under-voltage protection (UVP).

Command	VOUT_MIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0

If an attempt is made to program V_{OUT} below the limit set by this command, the device takes the following actions:

1. The commanded V_{OUT} is set to VOUT_MIN.
2. The VOUT bit is set in STATUS_WORD.
3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.
4. The device notifies the host.

The minimum value of VOUT_MIN is 0.5V. The value is unsigned and 1LSB = 2mV. The default value is 0.5V, meaning the default value of this register is 0x00FA.

VIN_ON (35h)

The VIN_ON command sets the V_{IN} value at which the converter starts to run if all other required start-up conditions are met. VIN_ON should be always set above VIN_OFF with a sufficient margin so that there is no bouncing between VIN_ON and VIN_OFF during power conversion.

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

The value is unsigned and 1LSB = 250mV. The default value is 4V.

VIN_OFF (36h)

The VIN_OFF command sets the V_{IN} value at which the converter, once operation has started, should stop power conversion. VIN_OFF should always be set below VIN_ON with a sufficient margin so that there is no bouncing between VIN_OFF and VIN_ON during power conversion.

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

The value is unsigned and 1LSB = 250mV. The default value is 2.75V.

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command reads and configures the threshold for over-temperature (OT) fault detection. If the measured temperature exceeds this value, an OT fault is triggered. The MPM3695-100 resumes normal operation after OTP based on the OT_RESPONSE in register MFR_OT_OC_SET (D6h). If an OT fault occurs, the OT fault flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), and the ALT# signal is asserted. Once the measured temperature falls below the value in this register, the MOSFET may switch back on with the OPERATION command when the device is operating in latch-off mode. The minimum temperature fault detection time should be shorter than 20ms. The temperature range is 0°C to 255°C.

If an OT fault occurs when the temperature exceeds this register value, the MPM3695-100 attempts to auto-retry once the temperature drops 20°C below this register value.

Command	OT_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								1°C/LSB							
Default Value	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

The value is unsigned and 1LSB = 1°C. The default value is 160°C, meaning the default value for this register is 00a0h.

OT_FAULT_LIMIT should be set below 160°C. If OT_FAULT_LIMIT is set above 160°C, the register value is ignored and the MPM3695-100 enters thermal shutdown if the junction temperature reaches 160°C.

Table 9 shows the relationship between the direct values and real-world values.

Table 9: Direct vs. Real-World OT Values

Direct Value	Real-World Value (°C)
0000 0000	0
0000 0001	1
1111 1111	255

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT commands reads and configures the threshold for over-temperature (OT) warning detection. If the sensed temperature exceeds this value, an OT warning is triggered. If an OT warning occurs, the OT warning flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), and the ALT# signal is asserted. The minimum temperature warning detection time should be shorter than 20ms.

Command	OT_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								1°C/LSB							
Default Value	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

The value is unsigned and 1LSB = 1°C. The default value is 140°C, meaning the default value for this register is 0x8Ch.

OT_WARN_LIMIT should be set below 160°C. The relationship between the direct value and real-world values are the same as OT_FAULT_LIMIT.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command reads and configures the threshold for V_{IN} over-voltage (OV) fault detection. If V_{IN} exceeds the value in this register, V_{IN} OV fault flags are set in the respective registers and the MPM3695-100 disables the power stage. If V_{IN} drops below VIN_OV_FAULT_LIMIT, the MPM3695-100 resumes normal operation.

Command	VIN_OV_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										500mV/LSB					
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

The value is unsigned and 1LSB = 500mV.

VIN_OV_FAULT_LIMIT should not be set above 18V.

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command reads and configures the threshold for V_{IN} over-voltage (OV) warning detection. If V_{IN} exceeds the value in this register, the V_{IN} OV warning flags are set in the respective registers and the ALT# signal is asserted.

Command	VIN_OV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										500mV/LSB					
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

The value is unsigned and 1LSB = 500mV.

VIN_OV_WARN_LIMIT should not be set above 17V.

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command reads and configures the threshold for the V_{IN} under-voltage (UV) fault detection. If V_{IN} falls below the value in this register, then the V_{IN} UV warning flags are set in the respective registers and the ALT# signal is asserted.

Command	VIN_UV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The value is unsigned and 1LSB = 250mV. The default value is 0.25V, meaning the default value for this register is 0x01.

TON_DELAY (60h)

The TON_DELAY command sets the time from when a start command is received (as configured by the ON_OFF_CONFIG command) until V_{OUT} starts to rise.

Command	TON_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								4ms/LSB							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB = 4ms. The maximum value for this register is 0x0100 (1024ms). The default value is 0ms.

TON_RISE (61h)

The TON_RISE command sets the soft-start time from when V_{OUT} starts to rise until it reaches the regulation point.

Command	TON_RISE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Function	X													1ms/LSB		
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Only the following values are supported:

- 3’b000: 1ms
- 3’b001: 2ms
- 3’b010: 4ms
- 3’b011: 8ms
- 3’b100 and up: 16ms

The default value is 4ms, meaning the default value for this register is 0x02.

TOFF_DELAY (64h)

The TOFF_DELAY command sets the from when EN turns off to when V_{OUT} starts to fall.

Command	TOFF_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								4ms/LSB							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB = 4ms. The maximum value is FFh (1020ms). The default value is 0ms.

STATUS_BYTE (78h)

The STATUS_BYTE command returns the value of certain flags indicating the MPM3695-100's status. Accesses to this command use the read byte protocol. To clear the bits in this register, the underlying fault must first be removed, then a CLEAR_FAULTS command must be issued.

Bits	Name	Behavior	Default	Description
7	RESERVED	N/A	0	Always reads as 0.
6	OFF	Live	0	0: The device is enabled 1: The device is disabled. This may be due to a V_{IN} under-voltage (UV) or over-voltage fault (OV), or from receiving an OPERATION off command
5	VOUT_OV	Latch	0	0: No V_{OUT} OV fault has occurred 1: A V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	0	0: No over-current (OC) fault has occurred 1: An OC fault has occurred
3	VIN_UV	N/A	0	Not supported, always reads as 0.
2	OT_FAULT_WARN	Latch	0	0: No over-temperature (OT) warning or fault has occurred 1: An OT warning or fault has occurred
1	COMM_ERROR	Latch	0	0: No communication error has occurred 1: A communication error has occurred
0	NONE_OF_THE_ABOVE	Latch	0	0: No other fault or warning has occurred 1: A fault or warning not listed in bits[7:1] has occurred

STATUS_WORD (79h)

The STATUS_WORD command returns the value of certain flags indicating the MPM3695-100's status. To clear the bits in this register, the underlying fault must first be removed, then a CLEAR_FAULTS command must be issued.

Bits	Name	Behavior	Default	Description
15	VOUT_STATUS	Latch	0	0: No V_{OUT} fault or warning has occurred 1: A V_{OUT} fault or warning has occurred
14	IOUT_STATUS	Latch	0	0: No I_{OUT} fault has occurred 1: An I_{OUT} fault has occurred
13	VIN_STATUS	Latch	0	0: No V_{IN} fault has occurred 1: A V_{IN} fault has occurred.
12	MFR_STATUS	N/A	0	Always reads as 0.
11	POWER_GOOD#	Live	0	0: A power good (PG) signal has been asserted 1: A PG signal has not been asserted
10	RESERVED	N/A	0	Always reads as 0.
9	RESERVED	N/A	0	Always reads as 0.
8	UNKNOWN	Latch	0	0: No other fault has occurred 1: A fault type not specified in bits[15:1] has been detected.
Low Byte	STATUS_BYTE	N/A	0	See the description for STATUS_BYTE (78h).

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 data byte with information related to V_{OUT} faults.

Bits	Name	Behavior	Default	Description
7	VOUT_OV_FAULT	Latch	0	0: No V_{OUT} over-voltage (OV) fault has occurred 1: A V_{OUT} OV fault has occurred
6	RESERVED	Latch	0	Always reads as 0.
5	RESERVED	Latch	0	Always reads as 0.
4	VOUT_UV_FAULT	Latch	0	0: No V_{OUT} under-voltage (UV) fault has occurred 1: A V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN	Latch	0	0: No VOUT_MAX or VOUT_MIN warning has occurred 1: An attempt has been made to set V_{OUT} to a value above VOUT_MAX or below VOUT_MIN
2	RESERVED	N/A	0	Always reads as 0.
1	RESERVED	N/A	0	Always reads as 0.
0	UNKNOWN	Latch	0	0: No other fault has occurred 1: A fault type not specified in bits[15:1] of STATUS_WORD has occurred

STATUS_IOUT (7Bh)

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	IOUT_OC	VIN_OV_ WARN	IOUT_OC_ WARNING	X				
Default Value	0	0	0	0	0	0	0	0

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns the value of certain flags indicating the device's V_{IN} status. To clear the bits in this register, the underlying fault or warning must first be removed, then a CLEAR_FAULTS command must be issued.

Bits	Name	Behavior	Default	Description
7	VIN_OV_FAULT	R/Latch	0	0: No over-voltage (OV) condition has been detected on the OV pin 1: An OV condition has been detected on the OV pin
6	VIN_OV_WARN	R/Latch	0	0: No OV condition has been detected on the VIN pin 1: An OV condition has been detected on the VIN pin
5	VIN_UV_WARN	R/Latch	0	0: No under-voltage (UV) condition has been detected on the VIN pin 1: An UV condition has been detected on the VIN pin
4:0	RESERVED	R	0	Always reads as 0000.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE returns the value of flags indicating an over-temperature (OT) fault or OT warning. To clear bits in this register, the underlying fault must first be removed, then a CLEAR_FAULTS command must be issued.

Bits	Name	Behavior	Default	Description
7	OT_FAULT	R/Latch	0	0: No over-temperature (OT) fault has occurred 1: An OT fault has occurred
6	OT_WARNING	R/Latch	0	0: No OT warning has occurred 1: An OT warning has occurred
5:0	RESERVED	R	0	Always reads as 0.

STATUS_CML (7Eh)

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	Invalid or unsupported command	Invalid or unsupported data	X	Memory fault detected	X	X	Other fault	Memory busy
Default Value	0	0	0	0	0	0	0	0

READ_VIN (88h)

The READ_VIN command returns the 10-bit measured V_{IN} value.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X						25mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_VOUT (8Bh)

The READ_VOUT command returns the 13-bit measured V_{OUT} value.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X			1.25mV/LSB												
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_IOUT (8Ch)

The READ_IOUT command returns the 14-bit measured I_{OUT} value. This value is also compared to IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT, and affects STATUS_IOUT.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		62.5mA/LSB													
Default value	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for over-temperature (OT) fault and warning detection. This value ranges between 40°C and 215°C.

Command	READ_TEMPERATURE_1															
Format	Two's complement integer															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X							1°C/LSB								
Default Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

READ_TEMPERATURE_1 is a 2-byte, two's complement integer. Bit[9] is the signed bit.

Table 10 shows the relationship between the direct values and real-world values.

Table 10: Direct vs. Real-World Values

Sign	Direct Value	Real-World Value (°C)
0	0 0000 0000	0
0	0 0000 0001	+1
0	1 1111 1111	+511
1	0 0000 0001	-511
1	1 1111 1111	-1

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the PMBus protocol revision to which the device is compliant. Access to this command uses the read byte protocol. Bits[7:4] indicate the PMBus revision of specification Part I to which the device is compliant. Bits[3:0] indicate the revision of specification Part II to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default Value	0	0	1	1	0	0	1	1

Bits[7:4] always reads as 4'b0011 to indicate PMBus specification Part I, Revision 1.3.

Bits[3:0] always reads as 4'b0011 to indicate PMBus specification Part II, Revision 1.3.

MFR_CTRL_COMP (D0h)

The MFR_CTRL_COMP command adjusts loop compensation.

Bits	Name	Access	Behavior	Default	Description
7:5	RESERVED	R/W	Live	0000	Reserved.
4	CFF	R/W	Live	0	Sets the feed-forward capacitance (C_{FF}). 0: 20pF 1: 50pF

3:1	RAMP	R/W	Live	110	Sets the internal ramp compensation to stabilize the loop. The actual ramp amplitude is related to the selection from register EAh, bit[3]. See the table below for more details. **EAh, Bit[3] = 1 (Multi-Phase)** 000: 8.6mV 001: 15mV 010: 27mV 011: 45mV 100: 13mV 101: 23mV 110: 41mV 111: 68mV
0	SLAVE_FAULT_ DETECTION	R/W	Live	1	Enables the slave fault detection function through the PG pin. 0: Slave-phase fault detection is enabled 1: Slave-phase fault detection is disabled

The default value of D0h is 0x0D.

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command adjusts the MPM3695-100's V_{OUT} behaviors.

Bits	Name	Access	Behavior	Default	Description
7	RESERVED	R/W	Live	0	Reserved.
6	VO_ DISCHARGE	R/W	Live	0	Enables active V_{OUT} discharging when the MPM3695-100 is commanded to turn off through CTRL or an OPERATION off command. 1: V_{OUT} discharges at CTRL low 0: No active V_{OUT} discharging
5:2	PG_DELAY	R/W	Live	0000	Set the PG pull-high time after soft-start finishes. 0000: 2ms 0001: 3ms …… 1110: 16ms 1111: 1ms
1:0	VO_RANGE	R/W	Live	00	Chooses the voltage divider radio. 00: External voltage divider 01: Internal voltage divider: V_{REF} / V_{OUT} = 0.4V to 1.344V 10: Internal voltage divider: V_{REF} / V_{OUT} = 0.7V to 2.688V 11: Internal voltage divider: V_{REF} / V_{OUT} = 1.3V to 5.376V

MFR_CTRL_OPS (D2h)

The MFR_CTRL_OPS command sets the switching frequency (f_{SW}) and light-load operation mode.

Bits	Name	Access	Behavior	Default	Description
7:3	RESERVED	N/A	N/A	00000	Reserved.
2:1	SWITCHING_ FREQUENCY	R/W	Live	01	00: Set f_{SW} to 400kHz 01: Set f_{SW} to 600kHz 10: Set f_{SW} to 800kHz 11: Set f_{SW} to 1000kHz

0	SKIP_CCM(SYNC)	R/W	Live	1	0: Pulse-skip mode (PSM) at light loads 1: Forced continuous conduction mode (FCCM) at light loads

The default value of this register is 0x03.

MFR_ADDR_PMBUS (D3h)

Command	MFR_ADDR_PMBUS							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ENABLE	ADDR						
Default Value	0	0	1	1	0	0	0	0

Bits	Name	Description
7	ENABLE	1: The address is determined by bits[6:0] of this command 0: The address is determined by the ADDR pin
6:0	ADDR	Determines the PMBus address if bit[7] of this command is set to 1.

The default value of D3h is 0x30.

MFR_VOUT_FAULT_LIMIT (D4h)

The MFR_VOUT_FAULT_LIMIT command sets the over-voltage protection (OVP) thresholds.

Bits	Name	Access	Behavior	Default	Description
7:4	RESERVED	N/A	N/A	0000	Reserved.
3:2	OV_EXIT_TH	R/W	Live	00	00: 10% of V_{REF} 01: 50% of V_{REF} 10: 80% of V_{REF} 11: 102.5% of V_{REF}
1:0	OV_ENTER_TH	R/W	Live	11	00: 115% of V_{REF} 01: 120% of V_{REF} 10: 125% of V_{REF} 11: 130% of V_{REF}

All OVP thresholds are relative to V_{REF}.

MFR_OVP_NOCP_SET (D5h)

The MFR_OVP_NOCP_SET command sets the V_{OUT} over-voltage protection (OVP) responses and the negative over-current protection (NOCP) delay time.

Bits	Name	Access	Behavior	Default	Description
7:4	RESERVED	N/A	N/A	0000	Reserved.
3	DELAY_NOCP	R/W	Live	0	0: 100ns delay after NOCP 1: 200ns delay after NOCP
2	RESERVED	N/A	N/A	N/A	Reserved.
1:0	VOUT_OV_ RESPONSE	R/W	Live	10	00: Latch-off mode with V_{OUT} discharging 01: Latch-off mode without V_{OUT} discharging in discontinuous conduction mode (DCM) 10: Hiccup mode with V_{OUT} discharging 11: Hiccup mode without V_{OUT} discharging in DCM

Bits[1:0] (VOUT_OV_RESPONSE) tell the converter how to respond to a V_{OUT} over-voltage (OV) fault. If an OV fault occurs, the device also takes the following actions:

1. Sets the VOUT_OV bit in STATUS_BYTE.
2. Sets the VOUT bit in STATUS_WORD.
3. Sets the V_{OUT} over-voltage fault bit in STATUS_VOUT.
4. Notifies the host by asserting the ALERT pin.

The four OV responses are described in greater detail below.

- Latch-off mode with V_{OUT} discharging: If the device reaches the over-voltage (OV) threshold, the LS-FET turns on until it reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. This process continues until V_{FB} drops below the OVP exit threshold set by register D4h, bits[3:2]. Then the LS-FET turns off. If V_{FB} exceeds the OV entry threshold again, then the LS-FET turns on again to discharge V_{OUT}. The converter does not attempt to restart until power is cycled on either VIN, VCC, or CTRL.
- Latch-off mode without V_{OUT} discharging (only effective in DCM): If the device reaches the OV entry threshold, the LS-FET turns on. When the inductor current reaches 0A, the converter enters Hi-Z mode (output disabled) and the converter stops discharging V_{OUT}. The converter does not attempt to restart until power is cycled on either VIN, VCC, or CTRL.
- Hiccup mode with V_{OUT} discharging: If the device reaches the OV entry threshold, the LS-FET turns on until the device reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. This process continues until V_{FB} drops below the OVP exit threshold set by register D4h, bits[3:2]. Then the LS-FET turns off and a new soft start is initiated.
- Hiccup mode without V_{OUT} discharging: If the device reaches the OV entry threshold, the LS-FET turns on until the device reaches NOCP. Then a new soft start is initiated.

The default value of this register is 0x02.

MFR_OT_OC_SET (D6h)

The MFR_OT_OC_SET command sets the over-current protection (OCP) response and the over-temperature protection (OTP) hysteresis. It is a 1-byte command.

Bits	Name	Access	Behavior	Default	Description
7:4	RESERVED	N/A	N/A	N/A	Reserved.
3	OC_RESPONSE	R/W	Live	01	0: Latch-off mode 1: Retry mode
2:1	OT_HYST	R/W	Live	00	00: 20°C 01: 25°C 10: 30°C 11: 35°C
0	OT_RESPONSE	R/W	Live	1	0: Latch-off mode 1: Retry after the temperature drops by the value set by bits[2:1] of this command

The OCP hiccup time is about 5 times the soft-start time set by TON_RISE (61h).

The default value of this register is 0x09.

MFR_OC_PHASE_SET (D7h)

The MFR_OC_PHASE_SET command sets the inductor valley current limit for each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive over-current (OC) cycles, OCP is triggered. This is a 1-byte command.

Bits	Name	Access	Behavior	Default	Description
7:5	RESERVED	N/A	N/A	000	Reserved.
4:0	OC_LIMIT	R/W	Live	10001	Current limit. 1.5A/LSB.

The value is unsigned and 1LSB = 1.5A. The default value is 25.5A for a single-phase inductor valley current limit.

MFR_PGOOD_ON_OFF_LIMIT (D9h)

The MFR_PGOOD_ON_OFF_LIMIT command sets the PGOOD on and off thresholds.

Bits	Name	Access	Behavior	Default	Description
7:4	RESERVED	N/A	N/A	000	Reserved.
3:2	PG_OFF	R/W	Live	00	00: 69% of V_{REF} 01: 74% of V_{REF} 10: 79% of V_{REF} 11: 84% of V_{REF}
1:0	PG_ON	R/W	Live	00	00: 90% of V_{REF} 01: 92.5% of V_{REF} 10: 95% of V_{REF} 11: 97.5% of V_{REF}

PG_OFF also sets the under-voltage protection (UVP) threshold. If V_{FB} drops below the PG_OFF level, the MPM3695-100 triggers UVP. The device responds to UVP the same way it responds to over-current protection (OCP).

Any fault condition pulls PG low.

MFR_VOUT_STEP (DAh)

The MFR_VOUT_STEP command sets the V_{OUT} transition slew rate after soft start finishes. It does not determine the V_{OUT} slew rate during soft start.

Bits	Name	Access	Behavior	Default	Description
7:4	RESERVED	N/A	N/A	0000	Reserved.
3:0	VOUT_STEP	R/W	Live	0100	0000: 20µs/2mV 1LSB = 2.5µs/2mV.

The default value of this register is 0x04.

MFR_CTRL (EAh)

The MFR_CTRL command enables certain functions.

Bits	Name	Access	Behavior	Default	Description
15:10	RESERVED	R	Live	N/A	For manufacturer use only.
9	OSM	R/W	Live	0	Enables output sink mode (OSM). 0: Enable OSM 1: Disable OSM

8:4	RESERVED	R	Live	N/A	For manufacturer use only.
3	PHASE_ OPERATION	R/W	Live	1	Selects single-phase or multi-phase operation. This bit affects the actual ramp amplitude selected through register D0h, bits[3:1]. See the MFR_CTRL_COMP (D0h) section on page 37 for more details. 0: For single-phase operation 1: For multi-phase operation
2:0	RESERVED	R	Live	N/A	For manufacturer use only.

Table 11: 0001 Suffix Code Configuration

Items	Channel 1
V_{OUT} set method	External divider
V_{OUT}	1.2V
V_{FB}	0.6V
Soft-start delay time	4ms
Individual valley current limit	25.5A
Light-load mode	FCCM
Individual switching frequency	600kHz
Ramp	41mV
UVLO rising	4V
UVLO falling	2.75V
Over-temperature (OT) fault limit	160°C
OT warning limit	140°C
V_{IN} over-voltage (OV) fault limit	18V

Table 12: 0001 Suffix Register Value

Register	Hex Value	Register	Hex Value
01	80	60	0
02	1E	61	2
10	0	64	0
21	258	9B	36
24	BB8	D0	D
25	2A0	D1	0
26	1FE	D2	3
29	1F4	D3	30
2b	FA	D4	3
35	10	D5	2
36	B	D6	9
4F	A0	D7	11
51	8C	D9	0
55	24	DA	4
57	22	EA	E8
58	1	-	-

APPLICATION INFORMATION

Operation Mode Selection

The MPM3695-100 provides both forced continuous conduction mode (FCCM) and pulse-skip mode (PSM) for light-load conditions. Four switching frequencies are available under light-load conditions. Set the switching frequency (f_{SW}) through the PMBus.

Setting the Output Voltage

Two feedback resistors are required to set the proper feedback gain. The feedback resistor values (R_1 and R_2) can be calculated with Equation (1):

$$R_2(k\Omega) = \frac{0.6}{V_{OUT}-0.6} \times R_1(k\Omega) \quad (1)$$

Where V_{OUT} is the output voltage.

The V_{OUT} feedback gain (G_{FB}) can be estimated with Equation (2):

$$G_{FB} = \frac{R_2}{R_1+R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) must be placed in parallel with R1. Table 6 on page 19 lists the values of feedback resistors and feed-forward capacitors for common output voltages.

The MPM3695-100 offers V_{OUT} configurability through the PMBus. In addition, V_{OUT} can be adjusted through the PMBus by adjusting the internal reference voltage (V_{REF}) of the PWM controller.

V_{REF} (default 0.6V) can be adjusted to be between 0.5V and 0.672V. For a given feedback resistor network, the maximum output voltage (V_{OUT_MAX}) can be calculated with Equation (3):

$$V_{OUT\_MAX} = \frac{0.672}{G_{FB}} \quad (3)$$

The minimum output voltage (V_{OUT_MIN}) can be estimated with Equation (4):

$$V_{OUT\_MIN} = \frac{0.5}{G_{FB}} \quad (4)$$

Follow the steps below to configure V_{OUT} through the PMBus:

1. Calculate G_{FB} with Equation (2), then write this value to the VOUT_SCALE_LOOP register.
2. Write the V_{OUT} settings to the VOUT_COMMAND register.
3. V_{REF} is automatically updated based on the commanded V_{OUT} and G_{FB}.

V_{OUT} monitoring through the PMBus is enabled by setting VOUT_SCALE_LOOP to a value that matches G_{FB}.

For applications where the PMBus interface is not required, V_{REF} is 0.6V by default and the MPM3695-100 operates in analog mode. Calculate the feedback resistor values with Equation (1).

Soft Start

The soft-start time (t_{SS}) can be configured using register 61h. The minimum t_{SS} is 1ms, but it can also be set to 2ms, 4ms, 8ms, or 16ms.

Pre-Biased Start-Up

The MPM3695-100 is designed for monotonic start-up into pre-biased loads. If V_{OUT} is pre-biased to a certain voltage during start-up, both the HS-FET and LS-FET are disabled until the internal V_{REF} exceeds V_{FB}.

Output Voltage Discharge

V_{OUT} discharge mode is enabled if the MPM3695-100 is disabled through the CTRL pin. In this case, both the high-side and low-side switches latch off and a discharge FET (connected between SW and GND) turns on to discharge the output capacitor. A typical discharge FET on resistance is 60Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge FET turns off.

Current Sense and Over-Current Protection (OCP)

The MPM3695-100 features on-die current sensing and a configurable inductor valley current limit threshold. The inductor valley over-current limit can be configured via register D7h, which sets the per-phase inductor valley current limit for both single- and multi-phase operation.

While the LS-FET is on, the inductor current is sensed and monitored cycle by cycle. The HS-FET does not turn on if an over-current (OC) condition is detected while the LS-FET is on. Therefore, the inductor current is also limited cycle by cycle. If an OC condition remains for 31 consecutive cycles, OCP is triggered.

If V_{OUT} drops below the under-voltage protection (UVP) threshold, the MPM3695-100 enters OCP immediately.

Once OCP is triggered, MPM3695-100 either enters hiccup mode or latch-off mode, depending on the register setting. To re-enable the device, cycle the power on VCC or CTRL.

Negative Inductor Current Limit

When the LS-FET detects a negative current below the limit (about -13A), the LS-FET turns off for a certain period to limit the negative current. This period is set by register D5h, bit[3].

Under-Voltage Protection (UVP)

The MPM3695-100 monitors V_{OUT} through the VOSNS+ and VOSNS- pins. Under-voltage protection (UVP) is triggered if V_{FB} drops below the UVP threshold. Once UVP is triggered, the MPM3695-100 enters either hiccup mode or latch-off mode, depending on the register setting. To re-enable the device, cycle the power on VCC or CTRL.

Over-Voltage Protection (OVP)

Over-voltage protection (OVP) is triggered if V_{FB} exceeds the OVP threshold. See the MFR_OVP_NOCP_SET (D5h) section on page 39 for more details.

Output Sinking Mode (OSM)

The MPM3695-100 enters output sinking mode (OSM) if V_{OUT} exceeds V_{REF} by 5% while simultaneously being below the OVP threshold in PSM. Once OSM is triggered, the MPM3695-100 runs in FCCM. The device exits OSM once the HS-FET turns back on.

Over-Temperature Protection (OTP)

The MPM3695-100 monitors the junction temperature. If the junction temperature exceeds the over-temperature protection (OTP) threshold, the MPM3695-100 enters either hiccup or latch-off mode depending on the PMBus selection. To re-enable the device, cycle the power on VCC or CTRL.

Power Good (PG)

The MPM3695-100 has an open-drain power good (PG) output. The PG pin must be pulled high to VCC (or a voltage source below 3.6V) through a pull-up resistor (typically 100kΩ). PG is initially pulled low once V_{IN} is applied to the MPM3695-100. After V_{FB} reaches the threshold set by POWER_GOOD_ON and the delay set by MFR_CTRL_VOUT completes, the PG pin is pulled high.

PG latches low if any fault occurs and a protection is triggered (e.g. UV, OV, OT, UVLO). After PG latches off, it cannot be pulled high again unless a new soft start is initiated.

If the input supply fails to power the MPM3695-100, the PG pin latches off.

Figure 5 shows the relationship between the PG voltage (V_{PG}) and the pull-up current (I_{PG}).

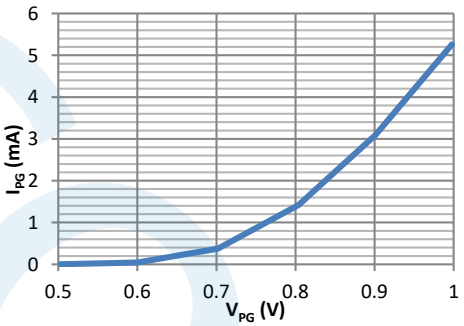


Figure 5: Power-Good Current vs. Power Good Voltage

Selecting the Input Capacitor

The buck converter has a discontinuous input current, and requires a capacitor to supply the AC current to the module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. When designing the PCB layout, place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with temperature. Ceramic capacitors with X5R and X7R dielectrics are recommended because they are fairly stable across a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current.

Estimate the input ripple current with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

The input capacitance determines the converter input voltage ripple. Select a capacitance that meets the relevant input voltage ripple requirements.

Estimate the input voltage ripple with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAP capacitors. Estimate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The ESR contributes minimally to the output voltage ripple, so an external ramp must be implemented to stabilize the system. Design the external ramp using R4, C4, and the equations above.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ESR ramp voltage is high enough to stabilize the system, thus eliminating the need for an external ramp. Select a minimum ESR value (about 12mΩ) to ensure stable operation. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

PCB Layout Guidelines

For the best results, refer to Figure 6 and follow the guidelines below:

VIN

1. Place sufficient decoupling capacitors as close as possible to each set of VIN and GND pins. A minimum of eight 22uF/25V ceramic capacitors are recommend.
2. Place sufficient GND vias around the GND pad of the decoupling capacitors.
3. Avoid placing sensitive signal traces close to the input copper and/or vias without sufficient ground shielding.

VOUT

4. Connect all VOUT pins together on a copper plane.
5. Place sufficient vias near the VOUT pads to provide a current path with minimal parasitic impedance.

GND

6. Connect all GND pins of the module using copper.
7. Place sufficient vias close to the GND pins to provide a current return path with minimal thermal resistance and parasitic impedance.

VOSNS+ and VOSNS-

8. Route VOSNS+ and VOSNS- as differential signals.
9. When modules are paralleled, connect all VOSNS+ pins of the master and slaves, and connect all VOSNS- master and slaves.
10. Avoid routing VOSNS+/- traces close to the input plane and high-speed signals.

SET> and SET<

11. SET< and SET> are connected inside the power module. In parallel operation, choose one SET pin for optimized routing (minimal trace distance) based on the power module placement.
12. Avoid routing SET traces close to the input plane and high-speed signals.

ISUM> and ISUM<

13. ISUM< and ISUM> are connected inside the power module. In parallel operation, choose one ISUM pin for optimized routing (minimal trace distance) based on the power module placement.
14. Avoid routing ISUM traces close to the input plane and high-speed signals.

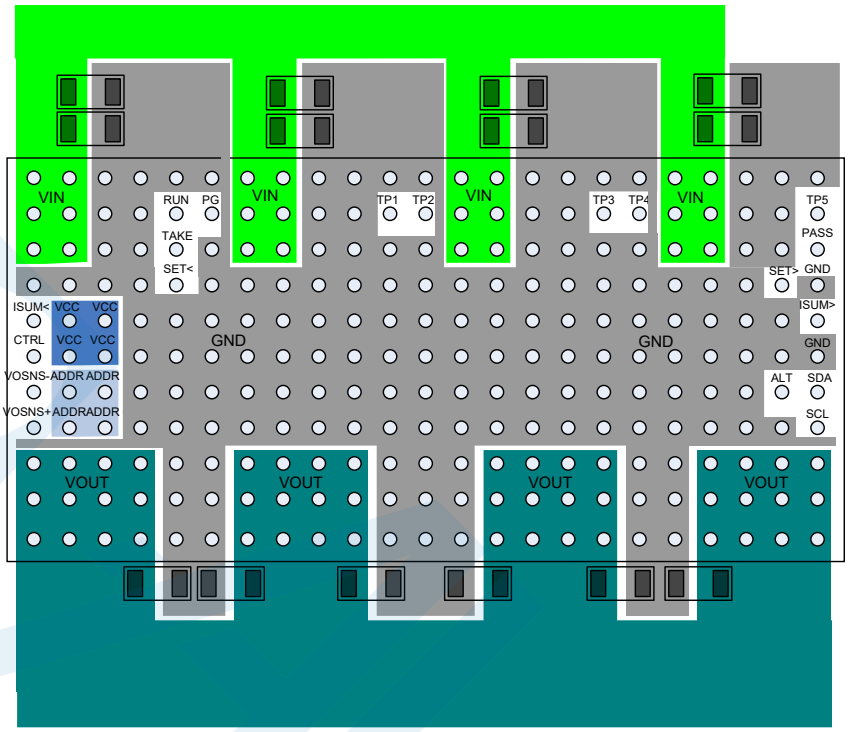


Figure 6: Recommended PCB Layout for Single-Module Operation

TYPICAL APPLICATION CIRCUITS

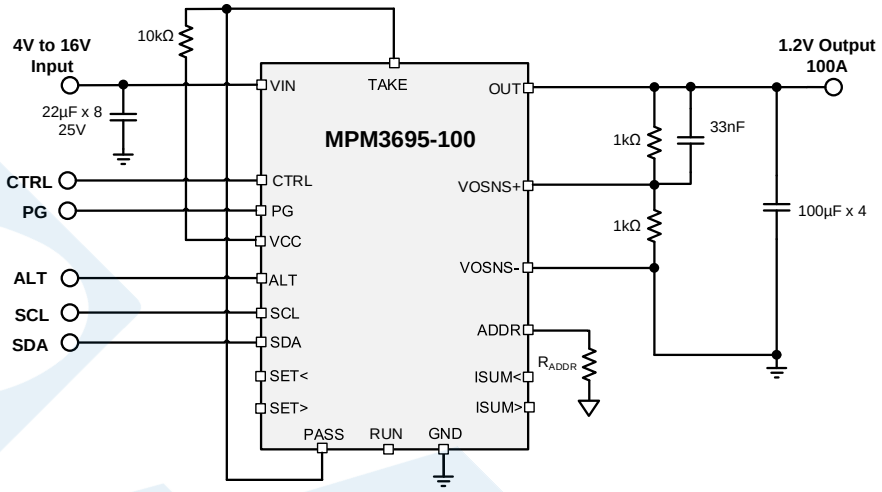


Figure 7: Typical Application Circuit (Single-Module Operation)

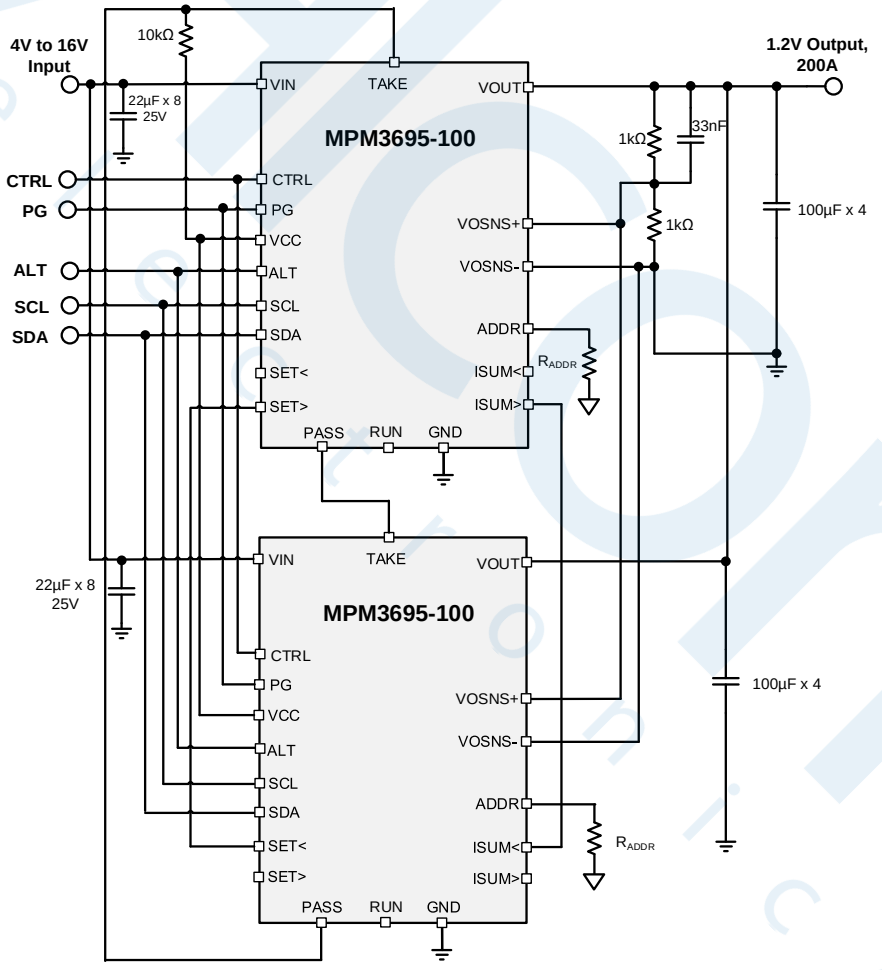


Figure 8: Typical Application Circuit (Dual-Module Operation)

TYPICAL APPLICATION CIRCUITS *(continued)*

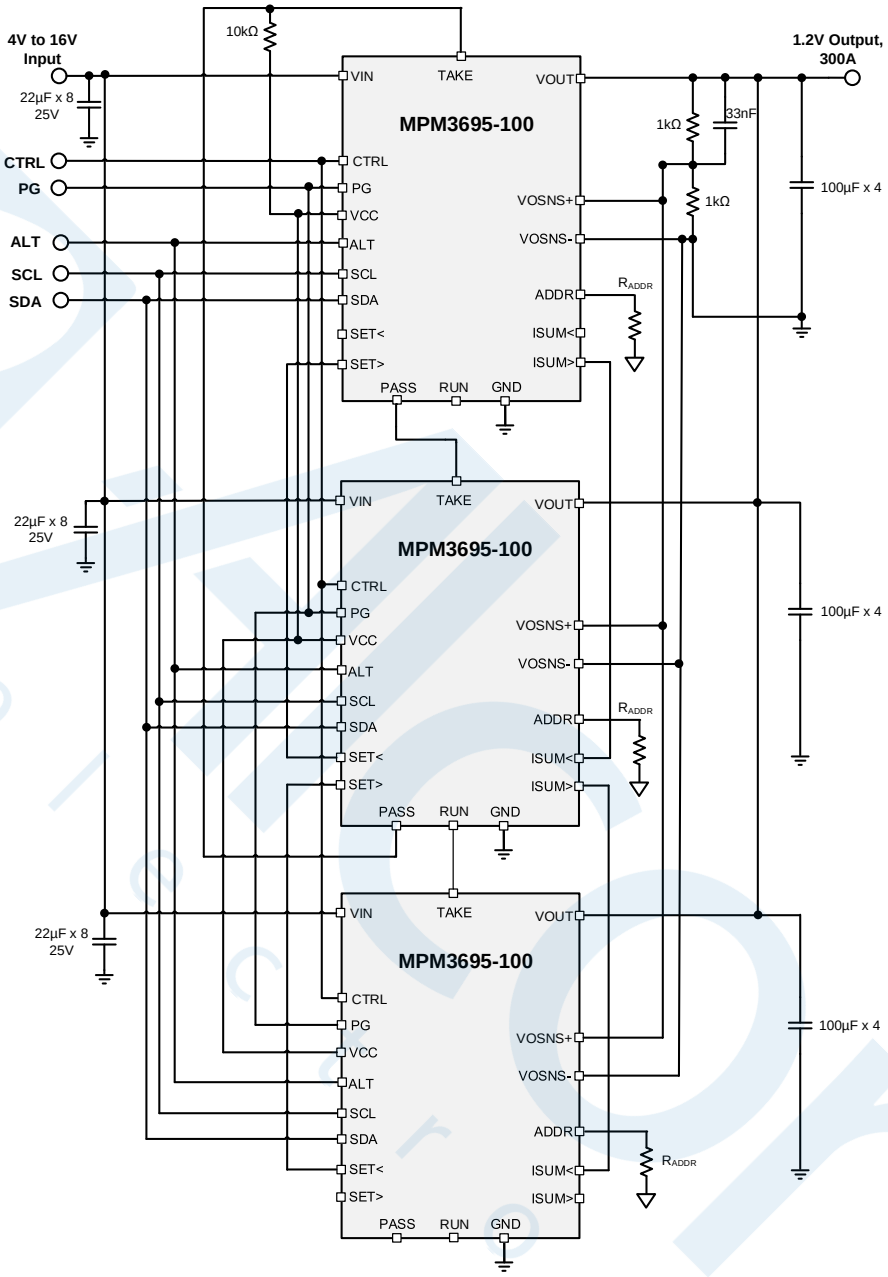


Figure 9: Typical Application Circuit (Three-Module Operation)

TYPICAL APPLICATION CIRCUITS *(continued)*

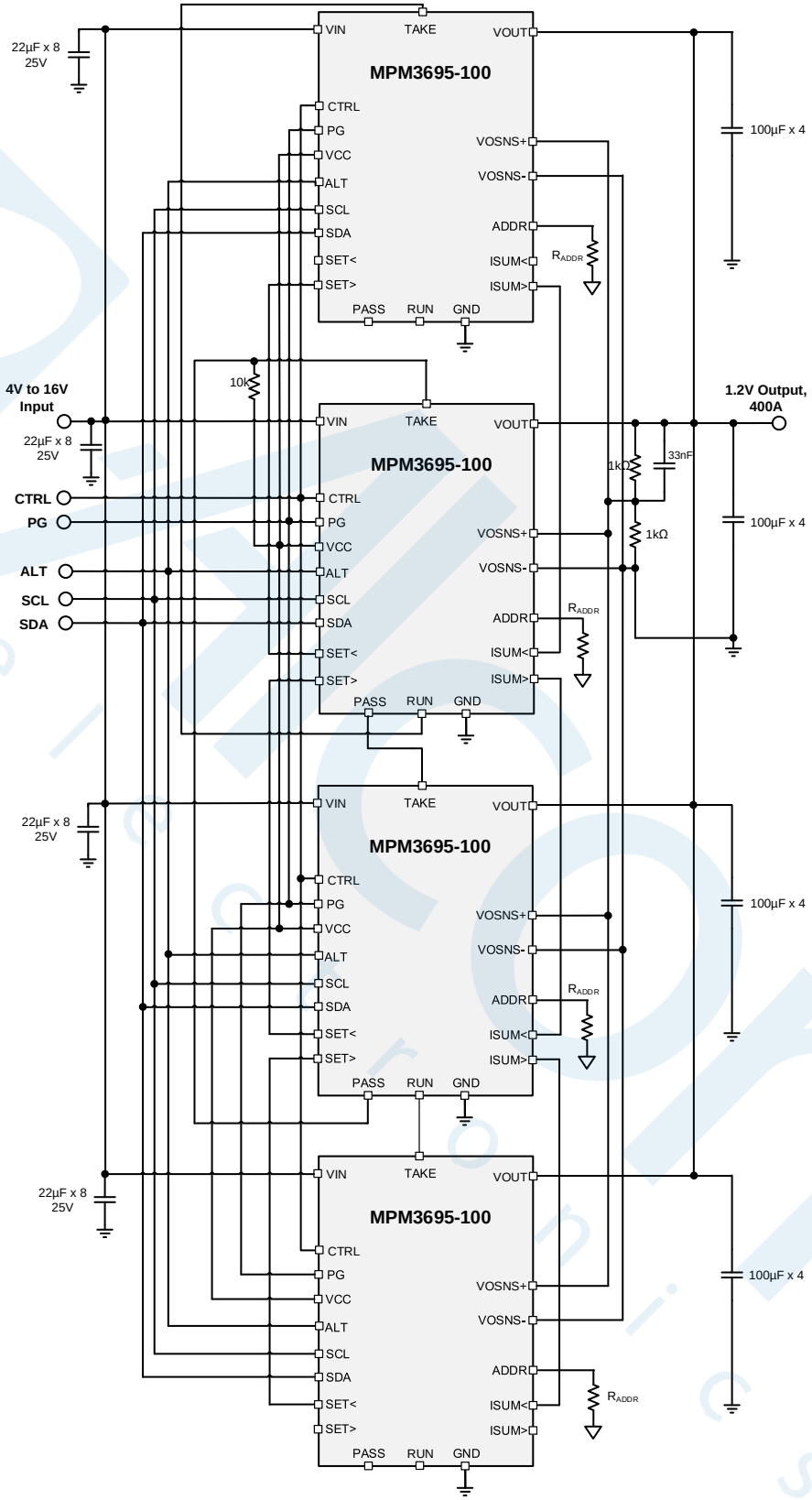
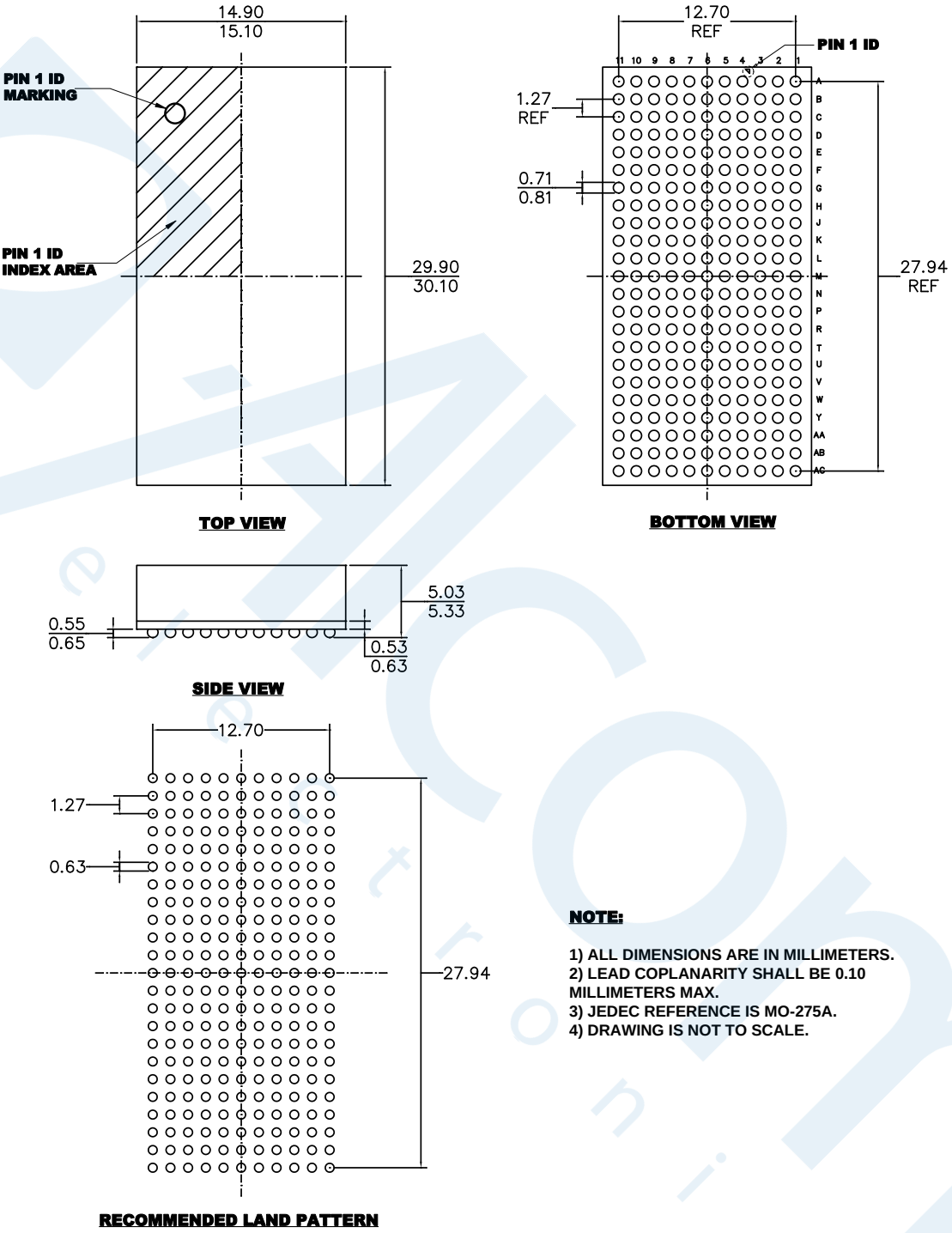


Figure 10: Typical Application Circuit (Four-Module Operation)

PACKAGE INFORMATION

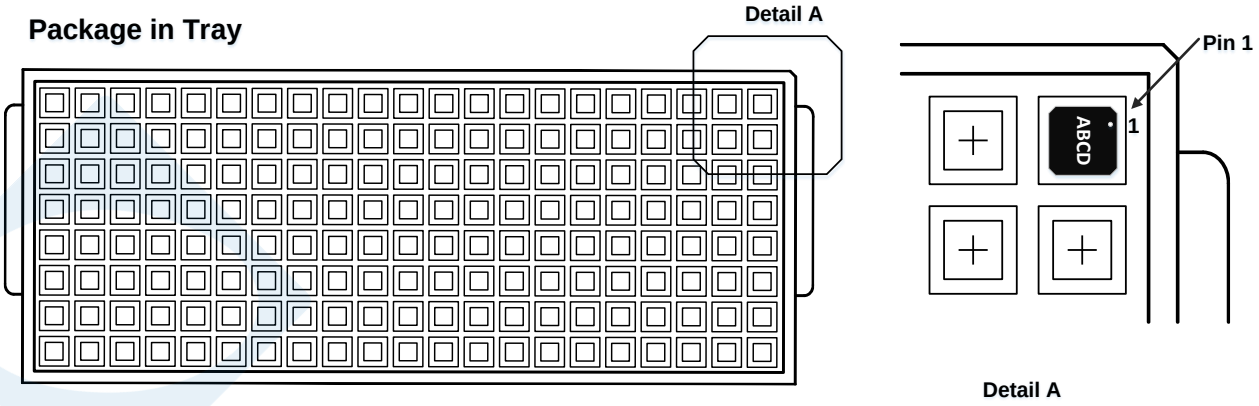
BGA (15mmx30mmx5.18mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION (11)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Carrier Tape Width	Carrier Tape Pitch
MPM3695GBH-100–T	BGA (15mmx30mmx5.18mm)	N/A	48	N/A	N/A	N/A

Note:

11) This is a schematic diagram of the tray. Different packages correspond to different trays with different lengths, widths, and heights.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/25/2021	Initial Release	-