MP2733

Wide Input Range, 4.5A, I²C-Controlled SW Charger with NVDC Power Path and USB OTG and Enhanced ADC

DESCRIPTION

The MP2733 is a 4.5A, highly integrated switch-mode battery charger management device for single-cell Li-ion or Li-polymer batteries. This device works with narrow voltage DC (NVDC) system power path management, and is well-suited for a variety of applications, including smartphones, tablets, wireless cameras, and other portable devices. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The I²C interface allows the device to be flexibly controlled with configurable charging and system settings.

The MP2733 supports a wide range of input sources, including standard USB host ports and high-powered wall adapters with fast charge capabilities. The MP2733 provides USB input type detection via the DP/DM pins.

The device supports USB On-the-Go (OTG) operation by supplying 5V on the input bus, with an output current limit up to 3A.

The MP2733 initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in different stages. Charging automatically terminates when a full charge is detected. When the charged battery drops below the recharge threshold, the charger automatically begins another charging cycle.

The charger provides various safety features for battery charging and system operations, including a charging safety timer, battery temperature monitoring, and over-voltage protection (OVP), and over-current protection (OCP). If a fault occurs, the charger asserts an INT signal to the host. The device provides BATTFET disable control to enter shipping mode, as well as system reset functionality via the DISC pin.

The MP2733 is available in a QFN-26 (3.5mmx3.5mm) package.

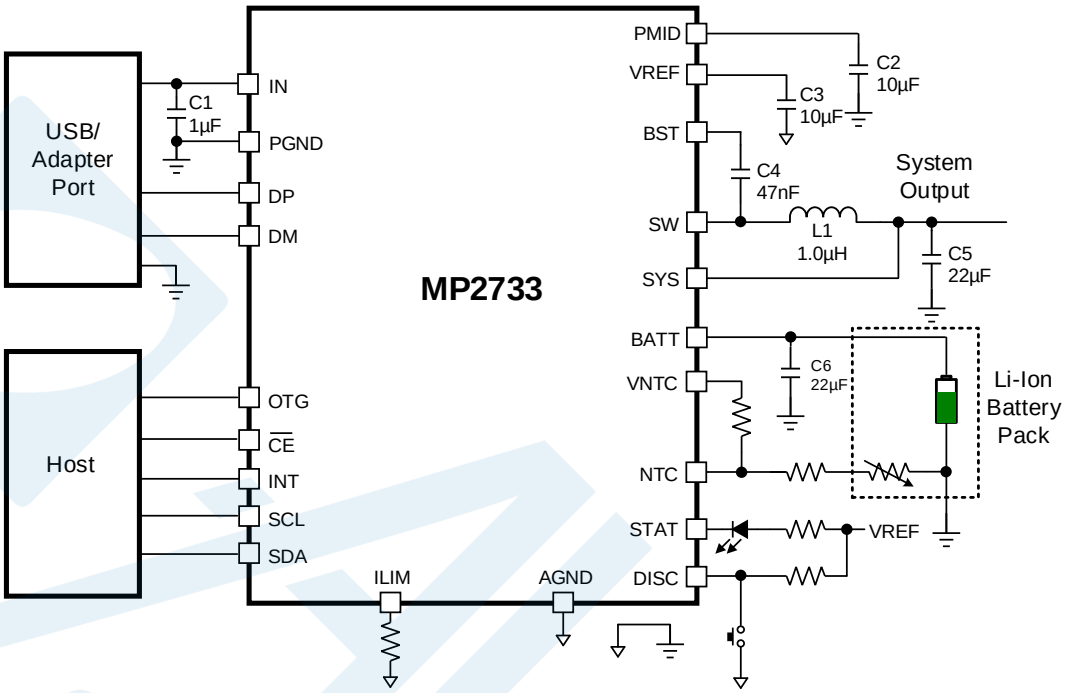
FEATURES

- 3.7V to 16V Operating Input Voltage Range
- Up to 22V Sustainable Voltage
- High-Efficiency, 4.5A, 1.35MHz Buck Charger with Up to 92% Charge Efficiency with 3A Charge Current:
  - Configurable D+/D- for Flexible Fast Charge Protocol Support
- USB OTG with 4.8V to 5.5V Adjustable Output: Up to 3A Output, Up to 93% Efficiency with 1.5A Output
- NVDC Power Path Management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- High Battery Discharge Efficiency with 14mΩ BATTFET Up to 8.5A
- I²C Interface for Flexible System Parameter Setting and Status Reporting
- Fully Integrated MOSFETs, Current Sensing
- Dedicated DISC Pin to Control Shipping Mode and System Reset
- 13μA Low Battery Leakage Current in Shipping Mode
- Integrated ADC Monitors Input Voltage and Current, Battery Voltage, Charge Current, System Voltage, and Battery Temperature
- Charging Status Indicator
- Safety Features: Configurable JEITA for Battery Temp Protection in Charge Mode, Battery Charging Safety Timer, Thermal Regulation and Shutdown, Watchdog Monitoring I²C, and Input/System OVP
- Available in a QFN-26 (3.5mmx3.5mm) Package

APPLICATIONS

- Tablet PCs
- Smartphones
- Wireless Cameras
- Other Portable Devices

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2733GQC-xxxx**	QFN-26 (3.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP2733GQC–xxxx–Z).

**"xxxx" is the register setting option. The factory default is "0001". This content can be viewed in the I²C Register Map on page 29. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

BQEYW

LLLLL

BQE: Product code of MP2733GQC
Y: Year code
W: Week code
LLLLL: Lot number

EVALUATION KIT EVKT-MP2733

EVKT-MP2733 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2733-QC-00A	MP2733 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

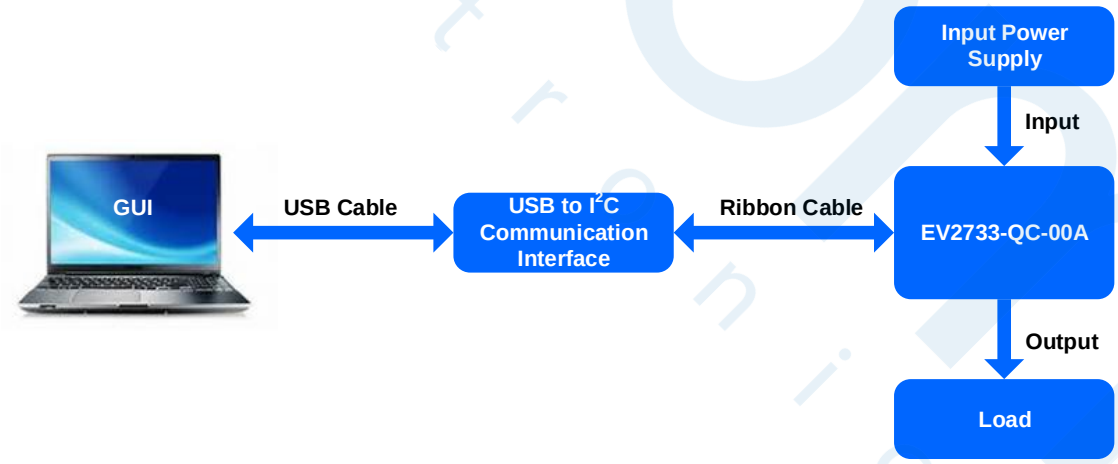
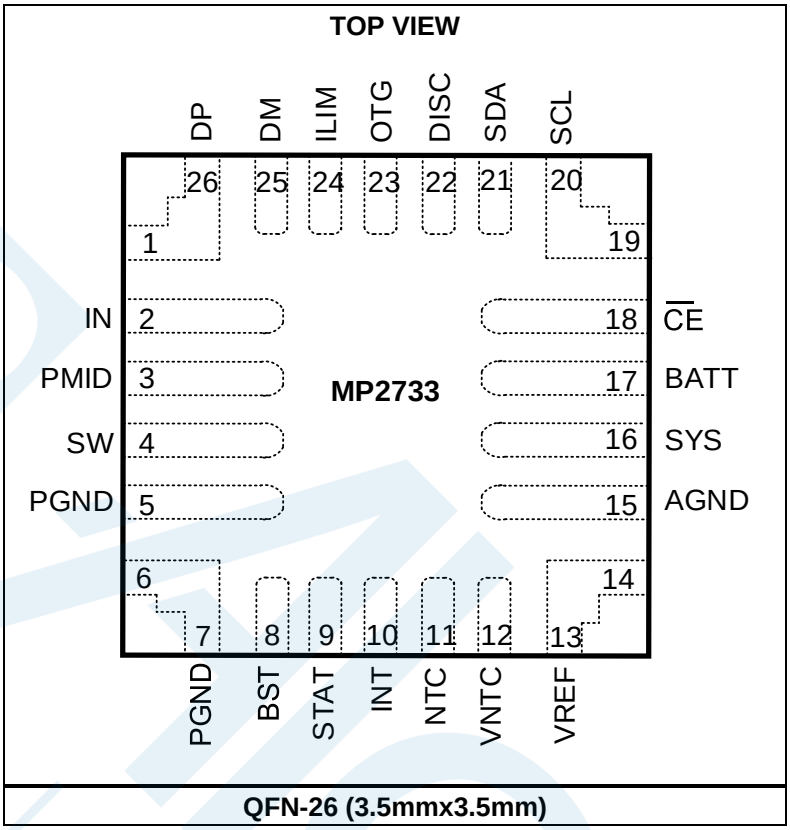


Figure 1: EVKT-MP2733 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-26 (3.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1, 26	DP	I/O	**Positive pin of the USB data line pair.**
2	IN	P	**Power input of the IC.** Place a 1µF ceramic capacitor from IN to PGND, as close as possible to the IC.
3	PMID	P	**Internal power pin.** Connect PMID to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET (HS-FET). Bypass PMID with a 10µF capacitor from PMID to PGND, placed as close as possible to the IC.
4	SW	P	**Switching node.**
5, 6, 7	PGND	P	**Power ground.**
8	BST	P	**Bootstrap pin.** Connect a 47nF bootstrap capacitor between the BST and SW pins to form a floating supply across the power switch driver. This drives the power switch's gate above the supply voltage.
9	STAT	O	**Open-drain charge status output to indicate various charger operations.** Connect STAT to VREF using a 10kΩ resistor.
10	INT	O	**Open-drain interrupt output**. The INT pin can send charging status and fault interrupt signals to the host.
11	NTC	I	**Temperature-sense input**. Connect a negative temperature coefficient thermistor to the NTC pin. Configure the hot and cold temperature windows with a resistor divider connected from VNTC to NTC to AGND. Charging is suspended when the NTC pin is out of range.
12	VNTC	P	**Pull-up voltage bias.** The VNTC pin is the pull-up voltage bias of the NTC comparator resistive divider for both the feedback and the reference.
13, 14	VREF	P	**PWM low-side driver output.** Connect a 10µF ceramic capacitor from VREF to AGND, placed as close as possible to the IC.
15	AGND	P	**Analog ground.**
16	SYS	P	**System output.** Connect a 22µF ceramic capacitor from SYS to PGND, placed as close as possible to the IC.
17	BATT	P	**Battery positive terminal.** Connect a 22µF ceramic capacitor from BATT to PGND, placed as close as possible to the IC.
18	$\overline{CE}$	I	**Active low charge enable pin.** Battery charging is enabled when the corresponding register is set to active and the $\overline{CE}$ pin is low.
19, 20	SCL	I	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
21	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
22	DISC	I	**Battery disconnection control pin.** The DISC pin can be used for shipping mode and system resetting.
23	OTG	I	**Boost mode enable control pin.** The On-The-Go (OTG) function is enabled via the I²C. During boost operation, the OTG pin can go low to suspend boost operation.
24	ILIM	I	**Configurable input current limit.** To set the maximum input current limit, connect a resistor from ILIM to ground. The actual input current limit is the lower value set by the ILIM pin or the I²C.
25	DM	I/O	**Negative pin of the USB data line pair.**

ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID to GND .....-0.3V to +22V
SW to GND .....-0.3V (-2V for 20ns) to +22V
BST to SW.....SW to SW + 5V
BATT, SYS to GND.....-0.3V to +6V
All other pins to GND .....-0.3V to +5V
STAT, INT sink current 10mA
Continuous power dissipation (T_A = 25°C) (2) 2.6W
Junction temperature.....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

V_{IN} to GND ..... 3.7V to 16V (4)
I_{IN}.....Up to 3.25A
I_{SYS} .....Up to 4.5A
I_{CC}.....Up to 4.5A
V_{BATT}.....Up to 4.67V
$I_{DSCHG\ (CONTINUOUS)}$.....Up to 8.5A
$I_{DSCHG\ (PULSE)}$.....Up to 9A
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-26 (3.5mmx3.5mm)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The inherent switching noise voltage should not exceed the absolute maximum rating on either the BST or SW pin. A tight layout minimizes switching loss.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Step-Down Converter						
Input voltage	V_{IN}		3.7		16 (6)	V
Input suspend current	I_{IN_SUS}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, suspend mode, EN_HIZ = 1		1	1.5	mA
Input quiescent current	I_{IN_Q}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, V_{BATT} = 3.6V, converter switching, I_{SYS} = 0A		4		
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling		3	3.2	V
Input UVLO threshold hysteresis		V_{IN} rising		200		mV
Input vs. battery voltage headroom	V_{HDRM}	V_{IN} rising	230	300	370	mV
		V_{IN} falling	120	190	260	mV
Input over-voltage protection (OVP) threshold	V_{IN_OVLO}	V_{IN} rising	5.8	6	6.3	V
		V_{IN} rising, for V_{IN} > 5V	16.2	16.7	17.2	
Input OVP threshold hysteresis		V_{IN} falling		380		mV
Internal reverse blocking MOSFET on resistance	R_{ON_Q1}	Measure from IN to PMID		20		mΩ
High-side MOSFET (HS-FET) on resistance	R_{ON_Q2}	Measure from PMID to SW		25		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{ON_Q3}	Measure from SW to PGND		25		mΩ
Switching frequency	f_{SW}	V_{BATT} = 3.7V, I_{CHG} = 2A, REG0Ah, bit[7] = 0	1.1	1.35	1.6	MHz
SYS Output						
Minimum system regulation voltage (I²C)	$V_{SYS\_REG\_MIN}$	V_{SYS_MIN} + V_{TRACK}, I_{SYS} = 0, V_{BATT} = 3.4V, REG04h, bits[3:1] = 110, REG04h, bit[0] = 1		3.82		V
Battery tracking voltage	V_{TRACK}	REG04h, bit[0] = 0		100		mV
		REG04h, bit[0] = 1		150		mV
Ideal diode forward voltage in supplement mode	V_{FWD}	10mA discharge current		20		mV
SYS vs. BATT comparator	$V_{SYS\_GT\_BATT}$	V_{SYS} falling to enter ideal diode mode		-20		mV
SYS vs. BATT comparator hysteresis		V_{SYS} rising to exit ideal diode mode		50		mV
Battery good comparator (threshold compared with V_{SYS_MIN})	V_{BATT_GD}	V_{BATT} rising to the BATTFET being fully turned on		60		mV
Battery good comparator hysteresis		V_{BATT} falling		100		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery charge voltage regulation (I²C)	V_{BATT_REG}	Depends on the I²C setting	3.4		4.67	V
Battery charge voltage regulation accuracy	$V_{BATT\_REG\_ACC}$	REG07h, bits[7:1] = 1010000, V_{BATT_REG} = 4.2V	-0.5		+0.5	%
		REG07h, bits[7:1] = 1011111, V_{BATT_REG} = 4.35V				
		REG07h, bits[7:1] = 1100100, V_{BATT_REG} = 4.4V				
Fast charge current (I²C)	I_{CC}	Depends on the I²C setting	320		4520	mA
Fast charge current accuracy	I_{CC_ACC}	I_{CC}, bits[6:0] = 0000100, V_{BATT} = 3.8V	442	500	558	mA
		I_{CC}, bits[6:0] = 0100110, V_{BATT} = 3.8V	1739	1850	1951	mA
		I_{CC}, bits[6:0] = 1000011, V_{BATT} = 3.8V	2849	3000	3151	mA
		I_{CC}, bits[6:0] = 1101001, V_{BATT} = 3.8V	4294	4520	4750	mA
Pre-charge to fast charge threshold (I²C)	V_{BATT_PRE}	V_{BATT} rising, REG05h, bit[7] = 1	2.8	3.0	3.1	V
Pre-charge to fast charge hysteresis		V_{BATT} falling		160		mV
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2.0	2.1	V
Trickle charge to pre-charge threshold hysteresis		V_{BATT} falling		50		mV
Trickle-charge current	I_{TC}	V_{BATT} = 1.8V, I_{PRE}, bit[0] = 1		185		mA
		V_{BATT} = 1.8V, I_{PRE}, bit[0] = 0		145		
Pre-charge current (I²C)	I_{PRE}	Depends on the I²C setting	150		750	mA
Pre-charge current accuracy		V_{BATT} = 2.6V, REG06h, bits[7:4] = 0010	182	225	268	mA
Charge termination current threshold (I²C)	I_{TERM}	Depends on the I²C setting	120		720	mA
Termination current accuracy		V_{BATT_REG} = 4.2V, REG06h, bits[3:0] = 0110	298	360	422	mA
Charge termination deglitch time	t_{TERM_DGL}			200		ms
Auto-recharge voltage threshold below V_{BATT_REG}	V_{RECH}	REG07h, bit[0] = 0		110		mV
Auto-recharge deglitch time	t_{RECH_DGL}			200		ms
BATTFET on resistance	R_{ON_Q4}	V_{BATT} = 3.8V		14		mΩ
Battery discharge current limit	I_{DSCHG_LMT}	V_{IN} = 0V, V_{BATT} = 3.8V, OTG disabled, I_{SYS} rising	8.5			A
Battery discharge function controlled by the DISC pin	t_{DISC}	DISC pin low time to turn off the battery discharge function, REG0Ah, bits[1:0] = 00		8		s
		Battery discharge off time to turn on the battery discharge function, REG0Ah, bits[3:2] = 00		0.5		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Input Current Regulation						
Input minimum voltage regulation (I²C)	V_{IN_MIN}		3.7		15.2	V
Input minimum voltage regulation accuracy	$V_{IN\_MIN\_ACC}$	REG01h, bits[6:0] = 0000110, V_{IN_REG} = 4.3V	-3		+3	%
Input current limit	I_{IN_LIM}	USB500	400	450	500	mA
		USB900	750	825	900	
		1A	840	920	1000	
		CDP or 1.5A	1270	1400	1500	
		DCP	1570	1690	1800	
		2A	1750	1880	2000	
		2.1A	1840	1970	2100	
		2.4A	2050	2240	2400	
		3A	2640	2800	3000	
Protection						
Battery over-voltage protection (OVP) threshold	V_{BATT_OVP}	Rising, compared to V_{BATT_REG}		103.5		%
Battery OVP threshold hysteresis		Compared to V_{BATT_REG}		1.5		%
Thermal regulation	T_{J_REG}	T_{J_REG}, bits[1:0] = 11		112		°C
Thermal shutdown threshold (6)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (6)				20		°C
NTC float threshold	V_{FLT}	As a percentage of VNTC		95		%
NTC float threshold hysteresis		As a percentage of VNTC		3.6		%
NTC low temp rising threshold	V_{COLD}	As a percentage of VNTC	71	72	73	%
NTC low temp rising threshold hysteresis		As a percentage of VNTC		1.3		%
NTC cool temp rising threshold	V_{COOL}	As a percentage of VNTC	59	60	61	%
NTC cool temp rising threshold hysteresis		As a percentage of VNTC		1.3		%
NTC warm temp falling threshold	V_{WARM}	As a percentage of VNTC	39.3	40.3	41.3	%
NTC warm temp falling threshold hysteresis		As a percentage of VNTC		1.5		%
NTC hot temp falling threshold	V_{HOT}	As a percentage of VNTC	35.3	36.3	37.3	%
NTC hot temp falling threshold hysteresis		As a percentage of VNTC		1.5		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREF LDO						
VREF LDO output voltage	V_{REF}	V_{IN} = 5V, I_{VREF} = 20mA		3.6		V
VREF LDO current limit	I_{REF_LMT}	V_{VREF} = 3.3V	40			mA
Battery Discharge Operation						
Battery operating range	V_{BATT}		2.6		4.75	V
Battery current in shipping mode	I_{BATT_SP}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATTFET off		13	16	µA
Battery quiescent current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATTFET on, OTG disabled		40	47	µA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATTFET on, OTG enabled		5.0		mA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATTFET on, OTG disabled, ADC enabled		2		mA
OTG output voltage	V_{IN_DSCHG}	REG03h, bits[5:3] = 011, I_{OTG} = 0A		5.07		V
OTG output voltage accuracy		As a percentage of V_{IN_OTG}, I_{OTG} = 0A	-2		+2	%
Battery operation UVLO	V_{BATT_UVLO}	V_{BATT} falling	2.35	2.45	2.55	V
		V_{BATT} rising	2.68	2.8	2.92	V
Battery operation UVLO for OTG	$V_{BATT\_UVLO\_OTG}$	V_{BATT} falling	2.45	2.55	2.65	V
		V_{BATT} rising		3.0		V
OTG output voltage protection threshold	V_{INOVP_DSCHG}	V_{BATT} = 3.7V, OTG is enabled, force a voltage at IN until switching is off		6.15		V
OTG output voltage protection threshold hysteresis				330		mV
OTG output current limit (I²C)	I_{IN_DSCHG}	REG03h, bits[2:0] = 000, V_{BATT} = 3.7V	0.5	0.6	0.7	A
		REG03h, bits[2:0] = 011, V_{BATT} = 3.7V	1.5	1.65	1.8	
		REG03h, bits[2:0] = 101, V_{BATT} = 3.7V	2.1	2.25	2.4	
		REG03h, bits[2:0] = 111, V_{BATT} = 3.7V	3.0	3.15	3.3	
Analog-to-Digital Converter (ADC)						
Resolution	RES			8		bits
Input voltage range	V_{IN}		3.6		15.3	V
Input voltage LSB	V_{IN_RES}			60		mV
Input voltage accuracy	V_{IN_ACC}	V_{IN} = 5V		2		LSB
Battery voltage range	V_{BATT}		0		5.1	V
Battery voltage LSB	V_{BATT_RES}			20		mV
Battery voltage accuracy	V_{BATT_ACC}	V_{BATT} = 3.8V		2		LSB
Charge current range	I_{CHG}		0		5.66	A
Charge current LSB	I_{CHG_RES}			17.5		mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Charge current accuracy	I_{CHG_ACC}	Charge mode, I_{CHG} = 1.84A		3		LSB
System voltage range	V_{SYS}		0		5.1	V
System voltage LSB	V_{SYS_RES}			20		mV
System voltage accuracy	V_{SYS_ACC}	V_{SYS} = 3.8V		2		LSB
Input current range	I_{IN}		0		3.39	A
Input current LSB	I_{IN_RES}			13.3		mA
Input current accuracy	I_{IN_ACC}	I_{IN} = 500mA		4		LSB
NTC voltage range	V_{NTC}		0		100	%
NTC voltage LSB	V_{NTC_RES}			0.392		%
NTC voltage accuracy	V_{NTC_ACC}	V_{NTC} = 50%		2		LSB
DP/DM USB Detection						
DP DCD current source	I_{DP_SRC}		7	10	14	uA
DM pull-down resistance	R_{DM_DOWN}		14.3	20	24.8	kΩ
Data detection voltage	V_{DAT_REF}		0.25	0.325	0.4	V
DP/DM comparator threshold (2.9V)	V_{TH_2P9}		2.8	2.9	3.0	V
DP/DM comparator threshold (2.4V)	V_{TH_2P4}		2.3	2.4	2.5	V
DP/DM comparator threshold (2.2V)	V_{TH_2P2}		2.1	2.2	2.3	V
DP/DM comparator threshold (1.7V)	V_{TH_1V7}		1.6	1.7	1.8	V
DP voltage source	V_{DP_SRC}		0.5	0.6	0.7	V
DM voltage source	V_{DM_SRC}		0.5	0.6	0.7	V
DP sink current	I_{DP_SINK}		70	100	130	μA
DM sink current	I_{DM_SINK}		70	100	130	μA
Leakage current input DP/DM pin	I_{DP_LKG}		-1		+1	μA
	I_{DM_LKG}		-1		+1	μA
Logic I/O Pin Characteristics (STAT, INT, OTG, /CE, DISC)						
Logic low voltage threshold	V_{IL}				0.4	V
Logic high voltage threshold	V_{IH}		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock frequency	f_{CLK}			5		MHz
Watchdog timer	t_{WDT}	REG08h, bits[5:4] = 11		160		s

Note:

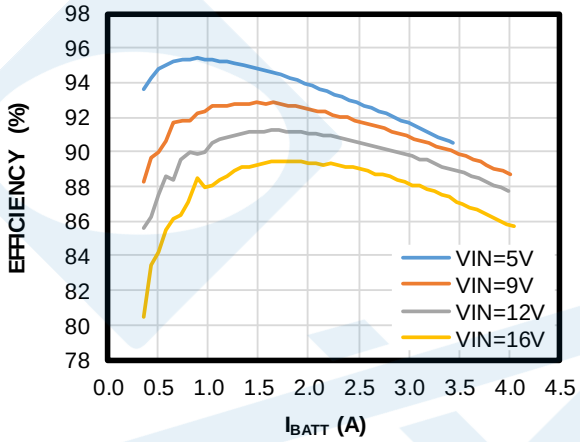
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

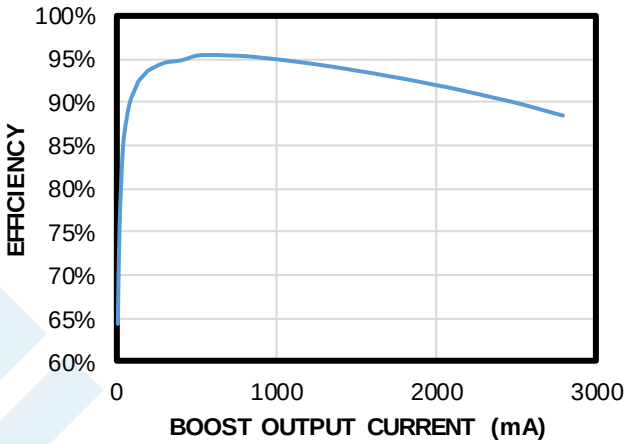
Charge Efficiency

V_{BATT} = 3.8V

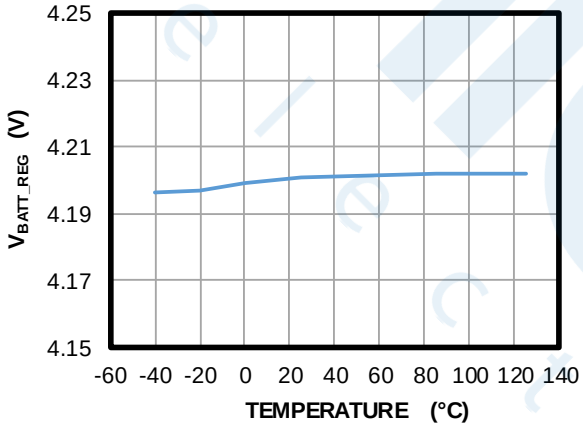


Boost Efficiency

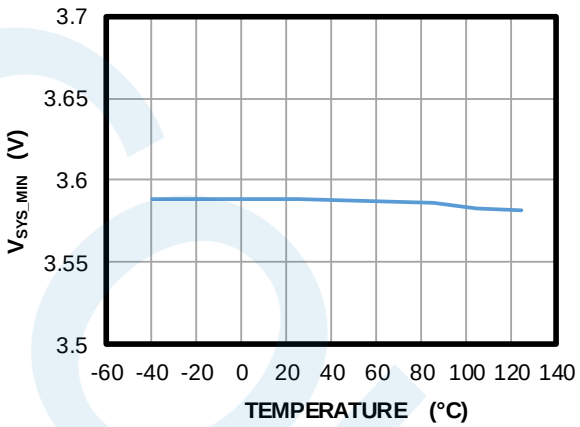
V_{BATT} = 3.8V



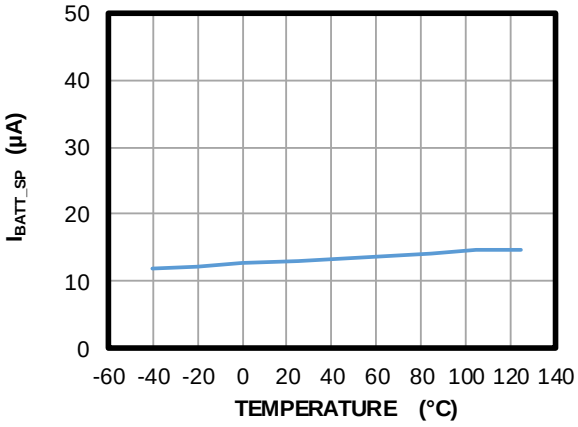
Battery Regulation Voltage vs. Temperature



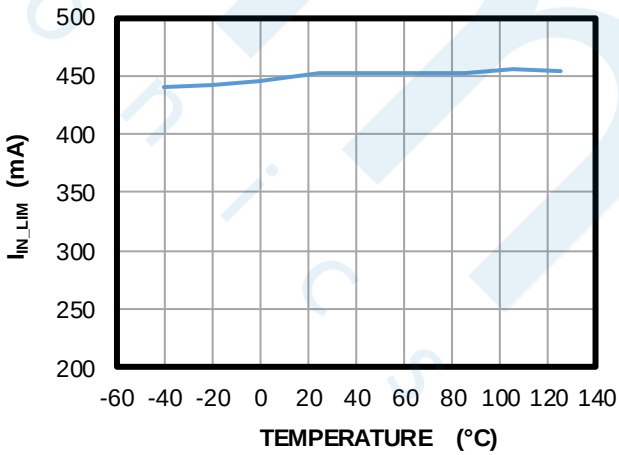
System Minimum Voltage vs. Temperature



Battery Current in Shipping Mode vs. Temperature



500mA Input Current Limit vs. Temperature

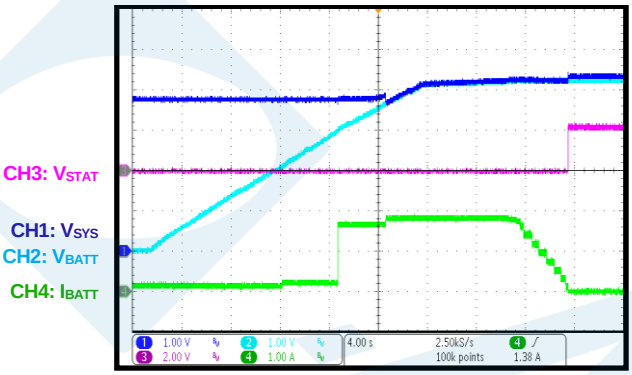


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

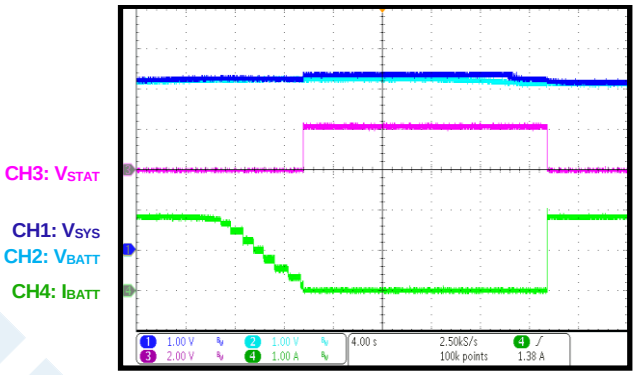
Battery Charge Curve

V_{IN} = 5V, V_{BATT_REG} = 4.2V, I_{SYS} = 0A



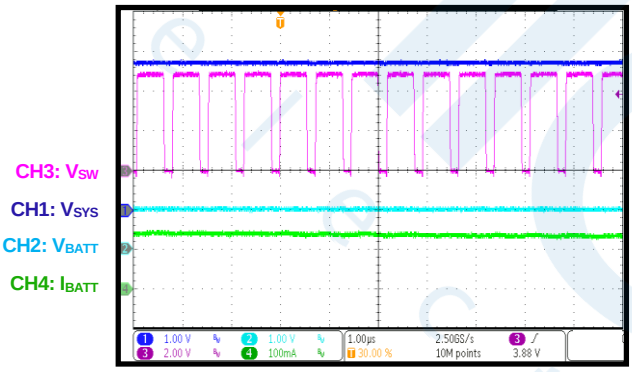
Auto-Recharge

V_{IN} = 5V, V_{BATT_REG} = 4.2V, I_{SYS} = 0A



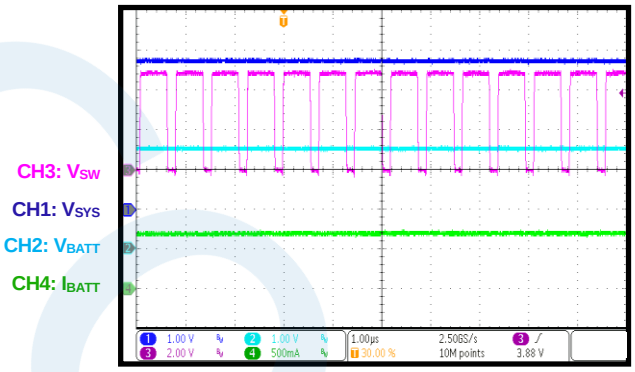
Trickle Charge

V_{IN} = 5V, V_{BATT} = 1.0V, I_{TC} = 145mA



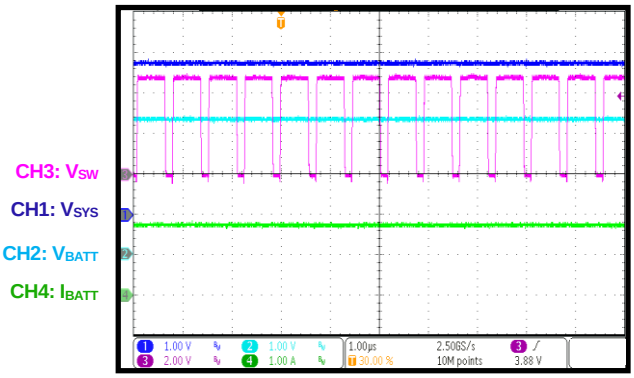
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2.5V, I_{PRE} = 680mA



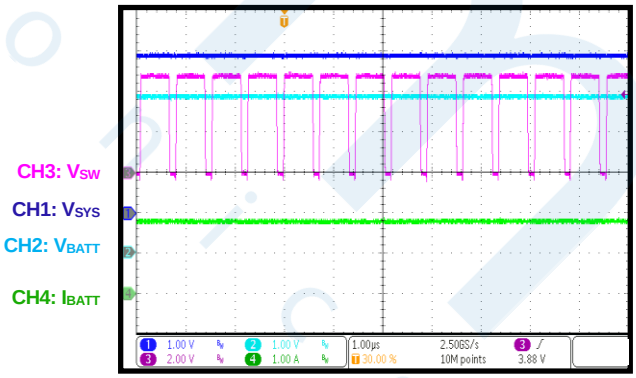
Constant Current Charge

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1840mA



Constant Current Charge

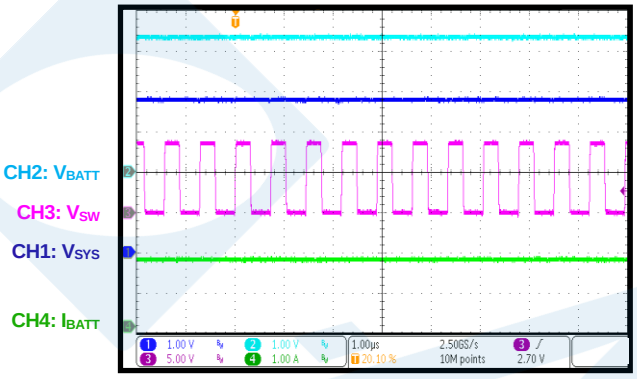
V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} = 1840mA



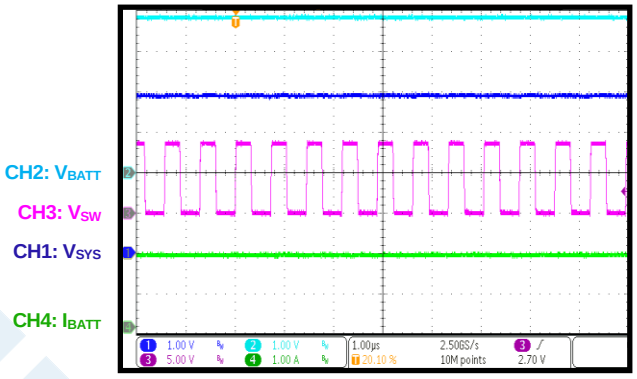
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

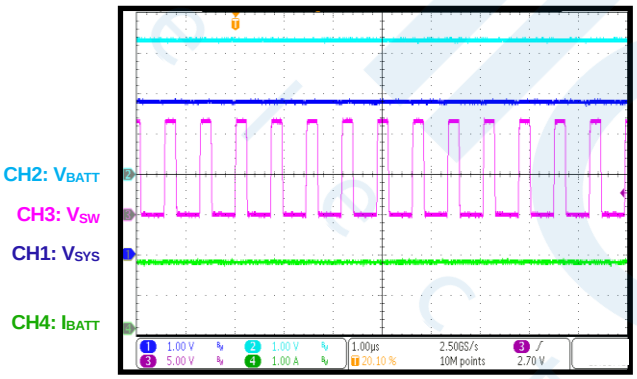
Constant Current Charge
V_{IN} = 9V, V_{BATT} = 3.3V, I_{CC} = 1840mA



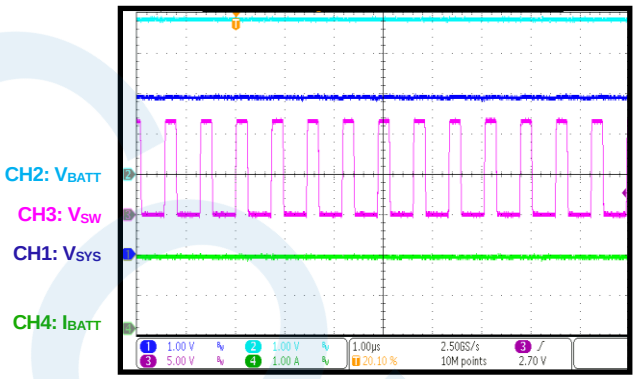
Constant Current Charge
V_{IN} = 9V, V_{BATT} = 3.8V, I_{CC} = 1840mA



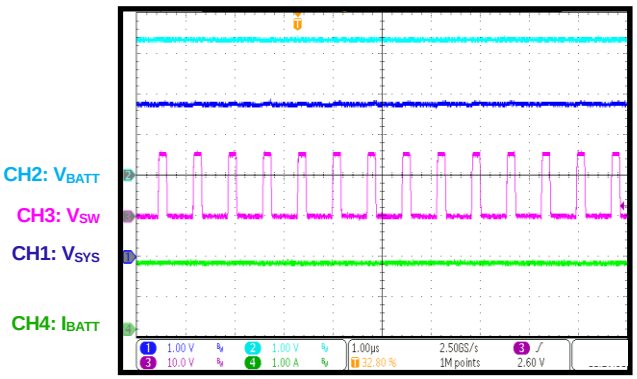
Constant Current Charge
V_{IN} = 12V, V_{BATT} = 3.3V, I_{CC} = 1840mA



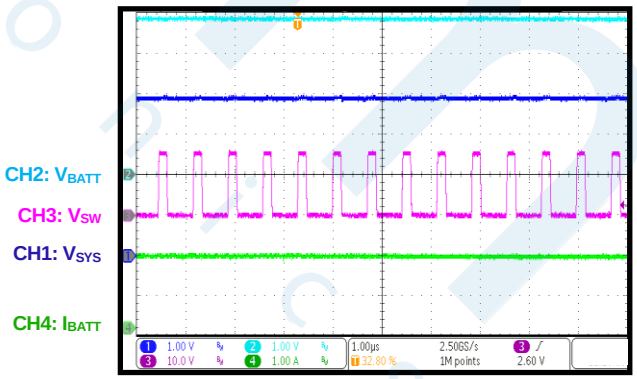
Constant Current Charge
V_{IN} = 12V, V_{BATT} = 3.8V, I_{CC} = 1840mA



Constant Current Charge
V_{IN} = 16V, V_{BATT} = 3.3V, I_{CC} = 1840mA



Constant Current Charge
V_{IN} = 16V, V_{BATT} = 3.8V, I_{CC} = 1840mA

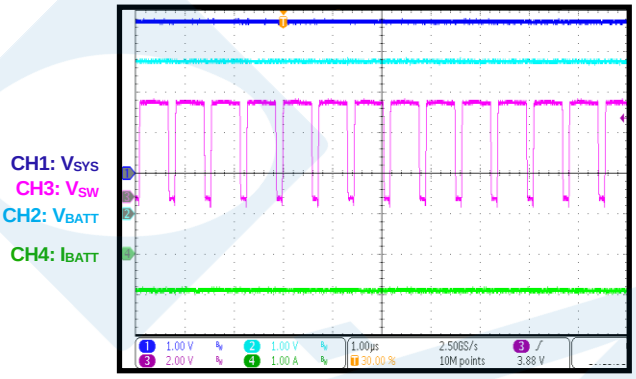


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

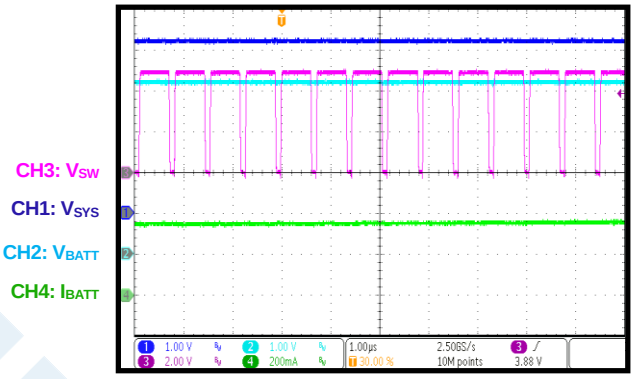
Battery Supplement Mode

V_{IN} = 5V, V_{BATT} = 3.8V, I_{SYS} = 4.5A



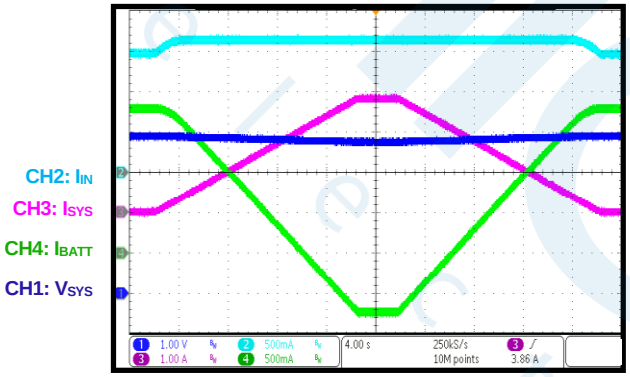
Constant Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.19V, I_{SYS} = 0A



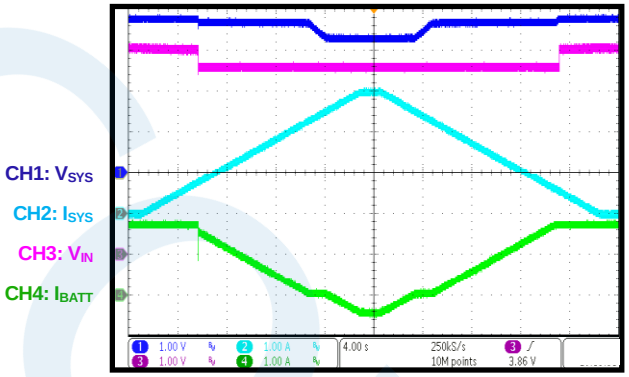
Input Current Limit

V_{IN} = 5V, V_{BATT} = 3.8V, I_{IN_LIM} = 1800mA



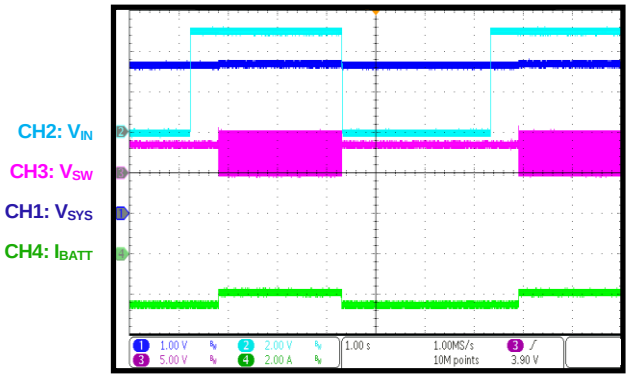
Input Voltage Limit

V_{IN} = 5V (2A), V_{BATT} = 3.3V, V_{IN_MIN} = 4.6V



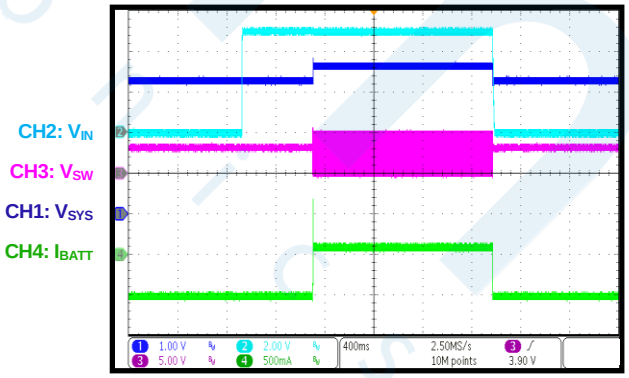
Start-Up/Shutdown

V_{IN} = 5V, I_{IN_LIM} = 500mA, V_{BATT} = 3.8V, I_{SYS} = 2.5A



Start-Up/Shutdown

V_{IN} = 5V, I_{IN_LIM} = 500mA, V_{BATT} = 3.3V, I_{SYS} = 0.5A

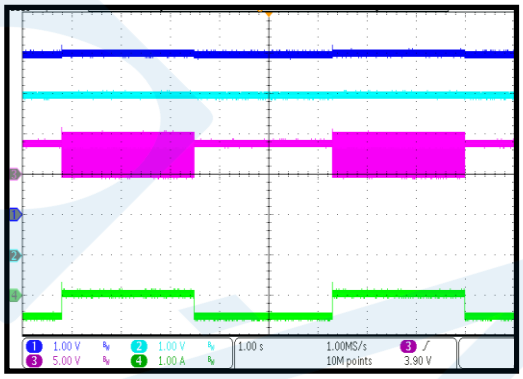


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

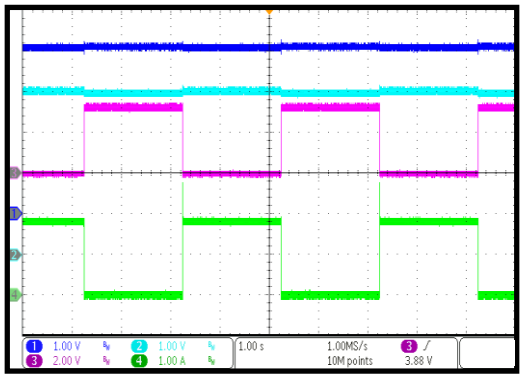
Suspend Mode On/Off

V_{IN} = 5V, I_{IN_LIM} = 500mA, V_{BATT} = 4.0V, I_{SYS} = 0.5A



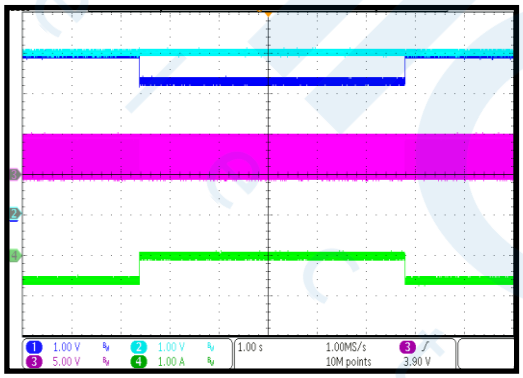
Charge On/Off

V_{IN} = 5V, V_{BATT} = 4.0V, I_{SYS} = 0A



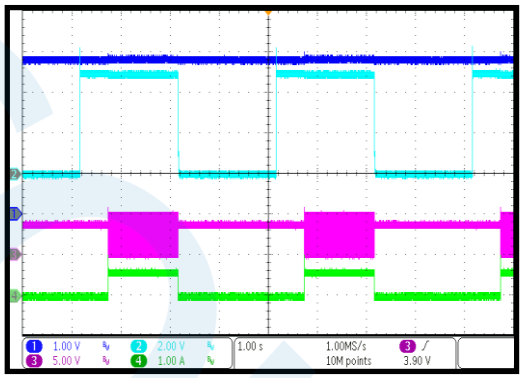
BATTFET On/Off

V_{IN} = 5V, V_{BATT} = 4.0V, I_{SYS} = 4A



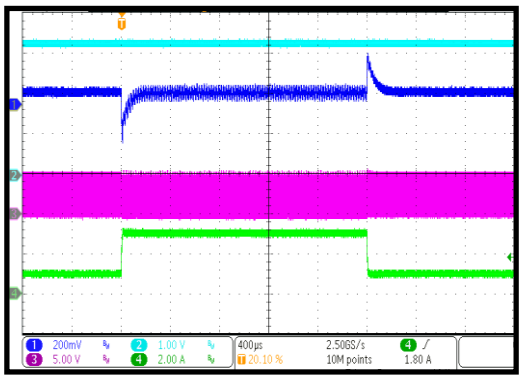
VIN Hot Insertion/Removal

V_{IN} = 5V, I_{IN_LIM} = 500mA, V_{BATT} = 3.8V



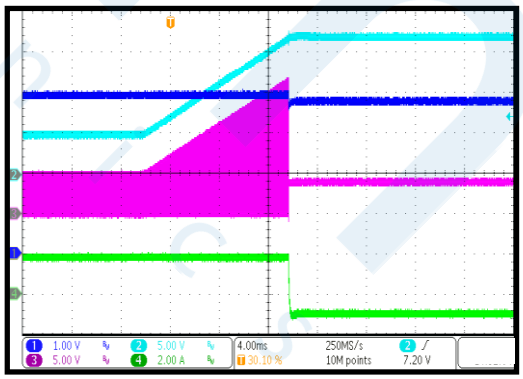
SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.3V, charging disabled, I_{SYS} = 1A to 3A



VIN OVP Test

V_{IN} = 5V to 17V, V_{BATT} = 3.8V, I_{SYS} = 1A

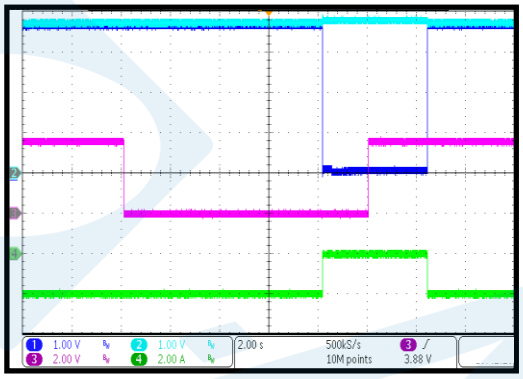


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CHG} = 1.84A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

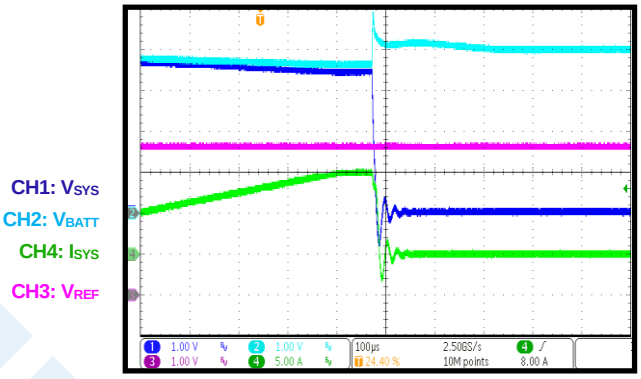
System Reset Mode

V_{IN} = floating, V_{BATT} = 3.8V, I_{SYS} = 2A



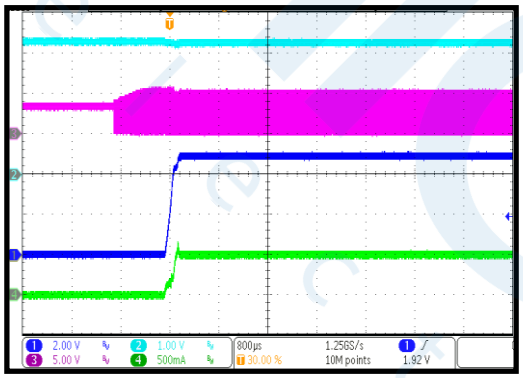
Battery Discharge Current

V_{IN} = floating, V_{BATT} = 4.0V, I_{SYS} = 10A max



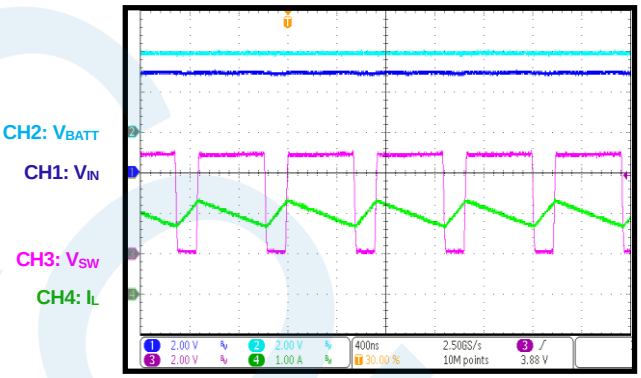
OTG Mode On

V_{IN} = floating, OTG mode, V_{BATT} = 3.3V, I_{IN_DSCHG} = 0.5A, I_{OTG} = 0.5A



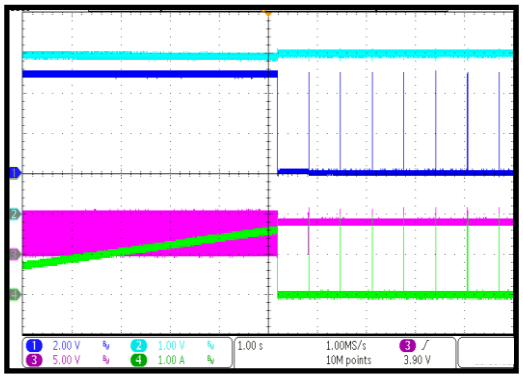
OTG Steady State Operation

V_{IN} = floating, OTG mode, V_{BATT} = 4.0V, I_{IN_DSCHG} = 3.0A, I_{OTG} = 1.5A



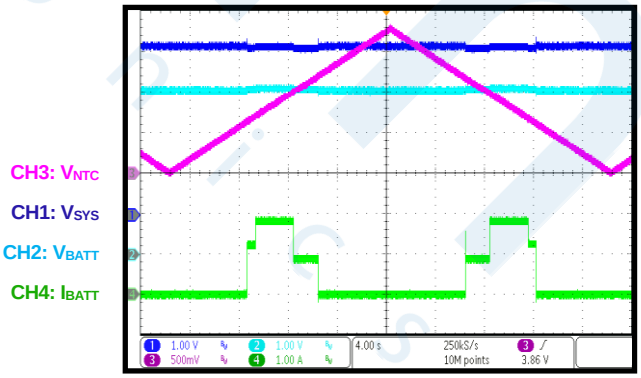
OTG Voltage Regulation

V_{IN} = floating, OTG mode, V_{BATT} = 4.0V, I_{IN_DSCHG} = 1.5A, I_{OTG} = 0A to 1.5A



NTC JEITA Operation

V_{IN} = 5V, V_{BATT} = 4.07V, I_{SYS} = 0A , JEITA_ISET = 50%, JEITA_VSET = -100mV



FUNCTIONAL BLOCK DIAGRAM

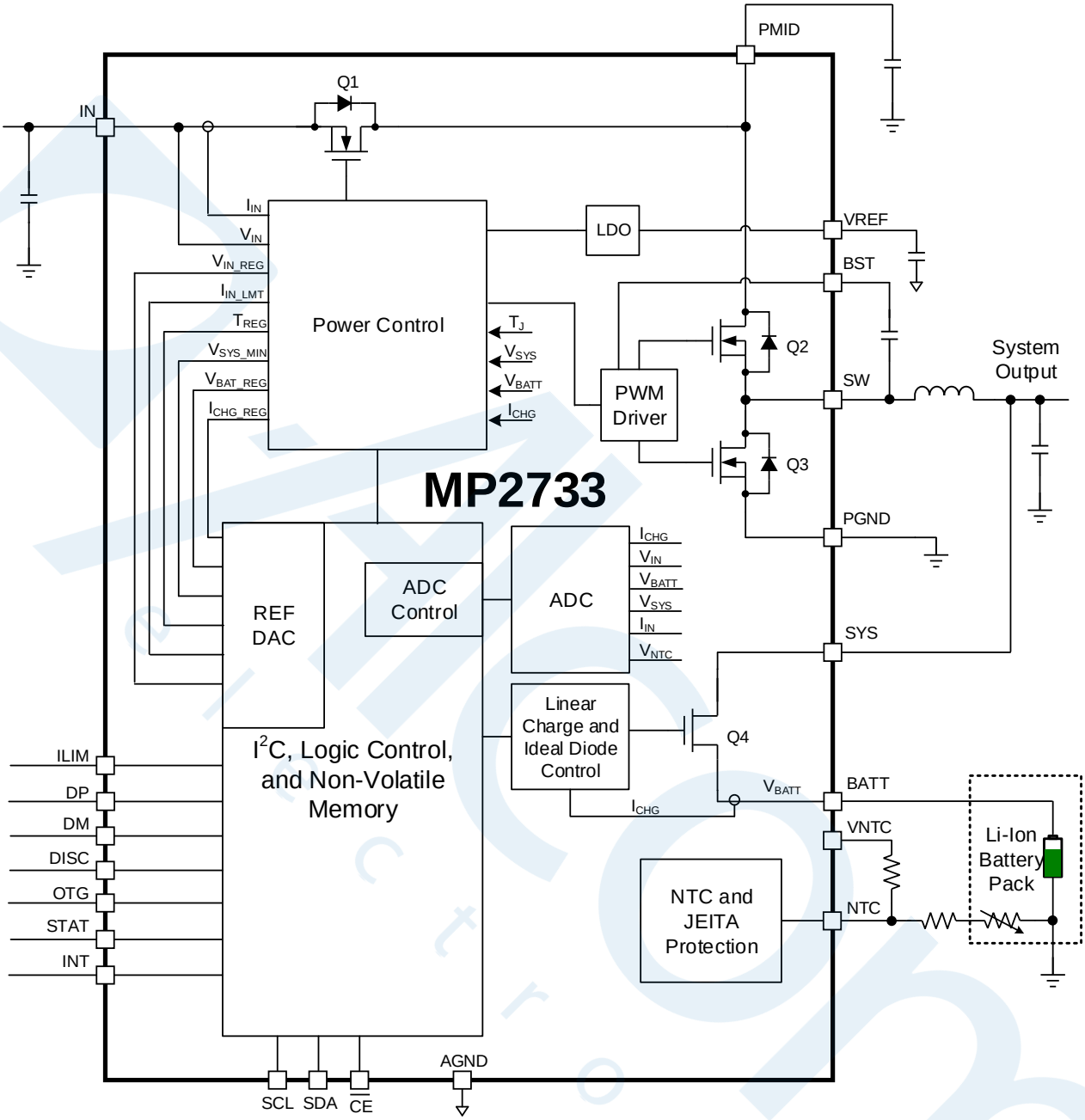


Figure 2: Functional Block Diagram

OPERATION

The MP2733 is a highly integrated, 4.5A, switch-mode battery charger IC with narrow voltage DC (NVDC) power path management for single-cell Li-ion or Li-polymer battery applications. The device integrates a reverse blocking FET (Q1), a high-side MOSFET (Q2), a low-side MOSFET (Q3), and a battery FET (Q4) between the SYS and BATT pins.

Power Supply

The VREF pin's voltage supplies the internal bias circuits, as well as the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) gate drive. The STAT pull-up rail can also be connected to VREF. The VREF pin has an internal LDO with two inputs. One input is from IN, and the other is from a battery. IN and the battery voltage are connected to the input of the LDO via a P-channel MOSFET.

Figure 3 shows the VREF power supply circuit.

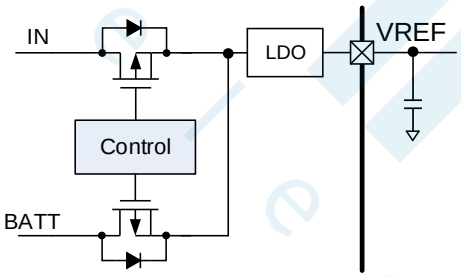


Figure 3: VREF Power Supply Circuit

Device Start-Up from Input Source

When an input source is plugged in, the MP2733 qualifies the input source before start-up. The input source must meet both of the following requirements:

1. $V_{IN} > V_{BATT} + V_{HDRM}$
2. $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$

If the input power source meets the conditions above, a good input is detected, and the device asserts an INT signal to the host. Then the device detects the input source type via the DP/DM pins. When DP/DM detection completes, the status register bit (VIN_STAT) changes and an INT pulse is sent to the host. Then the device starts up the step-down converter.

NVDC Power Path Management

The MP2733 employs an NVDC power structure with the battery FET, decoupling the system from the battery and thus allowing separate controls between the system and the battery. The system is a priority during start-up, even if the battery is deeply discharged or missing. If the input power is available with a depleted battery, the system voltage is regulated to the minimum system voltage ($V_{SYS\_REG\_MIN}$).

Figure 4 shows the NVDC power structure, which is composed of a front-end, step-down DC/DC converter and a battery FET placed between the SYS and BATT pins.

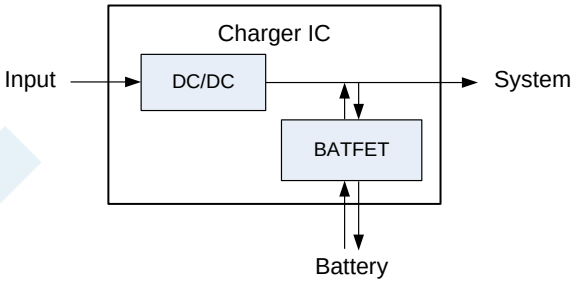


Figure 4: NVDC Power Path Management Structure

The DC/DC converter is a 1.35MHz, step-down switching regulator that directly drives the system load and charges the battery through the battery FET.

The system regulates the voltage in the following ways:

1. If the battery voltage (V_{BATT}) drops below V_{SYS_MIN}, the system voltage is regulated at $V_{SYS\_REG\_MIN}$, which exceeds V_{SYS_MIN} by V_{TRACK}. The battery FET works linearly to charge the battery via a trickle charge, pre-charge, or fast charge current, depending on V_{BATT}. V_{SYS_MIN} can be set via REG04h, bits[3:1], and V_{TRACK} can be set via REG04h, bit[0].
2. When V_{BATT} exceeds V_{SYS_MIN} + V_{BATT_GD} (60mV), the battery FET fully turns on, and the voltage difference between the system and the battery is the V_{DS} of the BATTFET. The charge current loop is implemented by the DC/DC converter's PWM control.
3. If charging is suspended or completed (the battery FET is off), the system voltage is always regulated at its maximum value (V_{SYS_MIN}, V_{BATT}) + V_{TRACK}.

Figure 5 shows the charging voltage regulation.

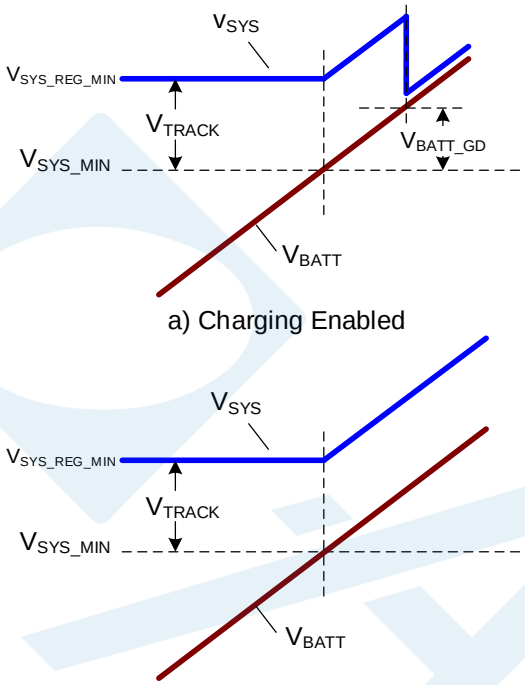


Figure 5: V_{SYS} Variation with V_{BATT}

Dynamic Power Management (DPM)

To meet the maximum current limit in USB specifications and avoid overloading the adapter, the MP2733 features dynamic power management (DPM), and continuously monitors the input current (I_{IN}) and input voltage (V_{IN}). The total input current limit is configurable to prevent the input source from being overloaded. If the input current increases and reaches the input current limit (I_{IN_LIM}), the charge current is reduced to prioritize the system power.

If the preset I_{IN_LIM} exceeds the adapter's rating, the additional minimum input voltage regulation loop activates to prevent the input power source from being overloaded. When V_{IN} falls below the input voltage regulation threshold due to a heavy load, the charge current is reduced to prevent V_{IN} from dropping further.

Power path management can operate in two ways:

1. If $V_{BATT} < V_{SYS\_MIN} + V_{BATT\_GD}$, the system voltage is regulated at $V_{SYS\_REG\_MIN}$. If the input current reaches I_{IN_LIM}, the input current loop controls the DC/DC converter. If the input voltage drops to V_{IN_MIN}, the input voltage loop controls the converter. Then the system voltage drops, and the battery FET driver is pulled down to decrease the charge current. This prioritizes the system power requirement.
2. If the battery is directly connected to the system, and $V_{BATT} > V_{SYS\_MIN} + V_{BATT\_GD}$, there is a free transition between each control loop. In this circumstance, the charge decreases automatically when I_{IN_LIM} or the voltage regulation threshold is reached.

Battery Supplement Mode

If the device reaches I_{IN_LIM} or the input voltage threshold, the charge current decreases. If the input source is still overloaded when the charge current decreases to zero, the system voltage (V_{SYS}) begins to drop. If V_{SYS} drops below V_{BATT}, the MP2733 enters battery supplement mode, in which the battery simultaneously powers the system and the DC/DC converter.

The MP2733 can operate in ideal diode mode to optimize the control transition between the battery FET and DC/DC converter. The battery FET enters ideal diode mode under either of the following conditions:

1. V_{IN} starts up from the battery supply system.
2. $V_{BATT} < V_{SYS\_MIN}$, and V_{SYS} drops below V_{BATT}.

During ideal diode mode, the battery FET operates as an ideal diode, and regulates the battery FET's gate drive. The V_{DS} of the battery FET remains at about 20mV. As the discharge current increases, the battery FET's gate drive increases, and its R_{DS} decreases until the battery FET is fully on.

Battery Charge Profile

If V_{IN} powers on, the CHG_CONFIG bit = 01, and the $\overline{CE}$ pin is low, then the device automatically completes a charging cycle without host involvement. However, the host can set different charging parameters to optimize the charge profile by writing to the corresponding registers via the I²C.

A new charge cycle starts when all of the following conditions are valid:

- Good input power is inserted
- Battery charging is enabled by the I²C, and $\overline{CE}$ is forced to logic low

- There is no thermistor fault on the NTC pin
- There is no safety timer fault
- The BATTFET is not forced to turn off

The MP2733 provides four main charging phases: trickle charge, pre-charge, constant current charge, and constant voltage charge. Each phase is described below:

Phase 1 (trickle charge): When the input power qualifies as a good power supply, the MP2733 checks V_{BATT} to determine whether trickle charge is required. If V_{BATT} is below V_{BATT_TC} (2.0V), a trickle-charge current is applied on the battery, which helps reset the protection circuit in the battery pack. The trickle-charge current can be set via REG06h, bit[4]. If REG06h, bit[4] is set to 1, the trickle-charge current is 185mA. If REG06h, bit[4] is set to 0, the trickle-charge current is 145mA.

Phase 2 (pre-charge): If V_{BATT} exceeds V_{BATT_TC}, the MP2733 starts to safely pre-charge the depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle ends and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via the I²C register REG06h, bits[7:4], and can be set between 150mA and 750mA.

Phase 3 (constant current charge): If V_{BATT} exceeds V_{BATT_PRE} set via REG05h, bit[7], the MP2733 enters a constant current charge (fast charge) phase. The fast charge current can be configured up to 3A via REG05h, bits[5:0].

There are two stages of fast charge. First, the battery FET works linearly to charge the battery with a fast charge current. Once V_{BATT} exceeds V_{SYS_MIN} + V_{BATT_GD}, the battery FET fully turns on. The charge current loop is implemented by the PWM control of the buck converter.

Phase 4 (constant voltage charge): When V_{BATT} reaches the configurable float voltage (V_{BATT_REG}) set via REG07h, bits[7:1], the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the battery termination threshold (I_{TERM}) set via REG06h, bits[3:0] after a 200ms termination deglitch time (assuming that the termination function is enabled if REG08h, bit[7] is set to 1). If I_{TERM} is not reached before the safety charge timer expires (see the Safety Timer section on page 24), the charge cycle ends, and a corresponding timeout fault signal is asserted.

Figure 6 shows the charging profile.

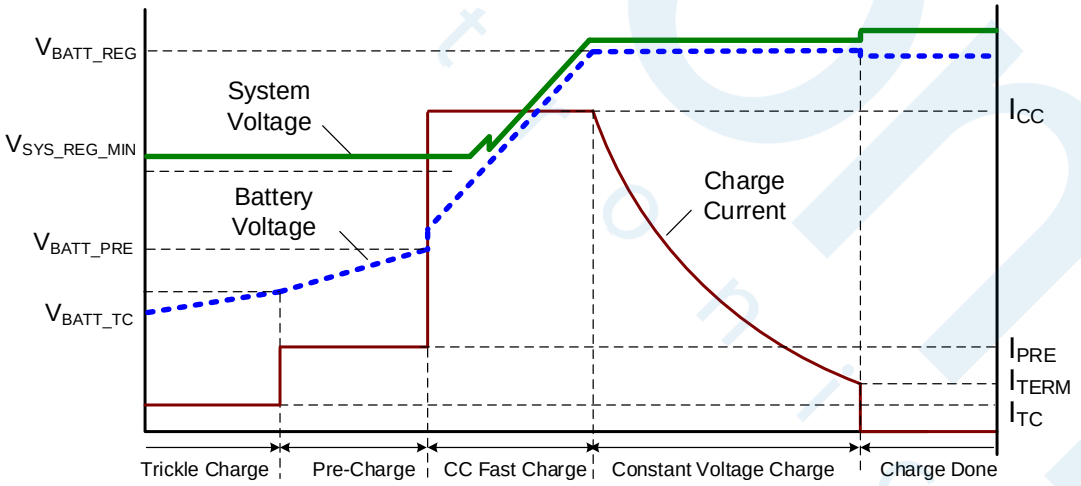


Figure 6: Battery Charging Profile

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as DPM regulation (input current limit or input voltage regulation loop) or thermal regulation. Thermal regulation reduces the charge current such that the IC junction temperature does not exceed the preset limit. Multiple thermal regulation thresholds (between 60°C and 120°C) help the system design meet the thermal requirements for different applications. The junction temperature regulation threshold can be set via REG02h, bits[3:2].

Auto-Recharge

When the battery is done charging, the battery may be discharged due to system consumption or self-discharge. When V_{BATT} is discharged below the recharge threshold after a 200ms auto-recharge deglitch time, the MP2733 automatically begins another charging cycle.

CE Control

$\overline{CE}$ is a logic input pin that enables and disables battery charging, or starts a new charging cycle. Battery charging is enabled when CHG_CONFIG (REG04h, bits[5:4]) is set to 01 and the $\overline{CE}$ pin is pulled to a low logic.

Battery Over-Voltage Protection (OVP)

The MP2733 is designed with built-in battery over-voltage protection (OVP). If V_{BATT} exceeds 103.5% of V_{BATT_REG}, the MP2733 immediately suspends charging and asserts a fault. If battery OVP occurs, charging is disabled but the DC/DC converter continues operating.

System Over-Voltage Protection (OVP)

The MP2733 monitors the voltage at the SYS pin. If an over-voltage condition (V_{SYS} > V_{BATT_REG} + 0.4V) is detected, the DC/DC converter turns off, and the system is powered by the battery via the battery FET.

Automatic Input Current Optimizer (AICO)

The device provides an optimized input current limit (I_{IN_LIM}) without overloading the input source. This function can be enabled or disabled by configuring the AICO_EN bit (disabled by default). If AICO is enabled, automatic input current optimization (AICO) is triggered when I_{IN_LIM} is set to a larger current, and V_{IN} drops to V_{IN_MIN}. This function decreases I_{IN_LIM} step by step until V_{IN} exits V_{IN_MIN} control. I_{IN_LIM} remains optimized and does not automatically run the AICO function unless another V_{IN_MIN} event occurs.

The actual I_{IN_LIM} is reported in the I_{IN_DPM} register when the AICO function is enabled (AICO_EN = 1). If the AICO function is disabled (AICO_EN = 0), I_{IN_LIM} is set by the IIN_LIM register. Any write to IIN_LIM can reset I_{IN_DPM} to the same I_{IN_LIM} value as when the AICO function is enabled.

Input Source Type Detection

The MP2733 features input source detection compatible with USB Battery Charging Specification 1.2 (BC1.2) and nonstandard adapters. The user can force DP/DM detection in host mode by writing 1 to USB_DET_EN (REG0Bh, bit[5]).

When V_{IN} is first applied and a good input source is detected, BC1.2 detection begins with data content detection (DCD). If DCD is effective, the standard downstream port (SDP), charging downstream port (CDP), and dedicated charging port (DCP) can be distinguished. If the 500ms DCD timer expires, then the MP2733 proceeds with nonstandard adapter detection.

DCD uses a current source to detect when the data pins have made contact during an attachment event. The protocol for DCD is described below:

1. The portable device (PD) detects V_{IN} assertion.
2. The PD turns on DP (I_{DP_SRC}) and the DM pull-down resistor.
3. The PD waits for the DP line to pull low.
4. If the DP line is detected to be low for 10ms, the PD starts primary detection.
5. If data contact is not detected, the DCD timer (about 500ms) expires.

After the DCD timer expires, the PD turns off I_{DP_SRC} and the DM pull-down resistor. Then the 50ms timer starts, and the PD can detect a special adapter. If a special adapter is detected, an INT signal is sent to the host. Otherwise, the PD starts primary detection after the 50ms timer expires.

Primary detection is used to distinguish between USB hosts (or the SDP) and different types of charging ports. During primary detection, the IC turns on V_{DP_SRC} on DP, and I_{DM_SINK} on DM. If the portable device is attached to a USB host, the DM pin pulls low. The SDP is detected, and an INT signal is sent to the host.

If the DM pin is high, the IC goes into secondary detection, which distinguishes between a CDP and a DCP.

During secondary detection, the IC turns on V_{DM_SRC} on DM, and I_{DP_SINK} on DP. If the input source is a CDP port and DP is low, then the CDP is detected, and an INT signal is sent to the host.

If DP is high, the DCP source is detected, and an INT signal is sent to the host. In this case, after turning off V_{DM_SRC} and I_{DP_SINK}, V_{DP_SRC} is applied to DP, and the IC goes to fast charge detection.

Fast charge detection identifies whether the input source has fast charge capability.

If DM is always high during fast charge detection, the input source has no fast charge capability. If DM is low for 40ms when the input source has fast charge capability, the MP2733 sends an INT signal to the host. The MP2733 features an I²C-configurable DP/DM output for host-controlled communication, with various fast charge protocols.

Table 1 lists input current limits that are compatible with USB specifications and BC1.2.

Table 1: Input Current Limit vs. USB Type

DP/DM Detection	I_{IN_LIM} (A)	V_{IN_OVP} (V)	V_{IN_MIN} (V)
Nonstandard adapter (1A)	1	6	3.7 to 5.2
Nonstandard adapter (2.1A)	2.1	6	3.7 to 5.2
Nonstandard adapter (2.4A)	2.4	6	3.7 to 5.2
SDP	0.5	6	3.7 to 5.2
CDP	1.5	6	3.7 to 5.2
DCP	1.8	6	3.7 to 5.2

USB detection is independent of the charge enable status. After DP/DM detection completes, the MP2733 indicates the USB port type in the status register VIN_STAT (REG0Ch, bits[7:5]) and fast charge adapter (REG17h, bit[6]), then asserts an INT signal to the host. The host can revise the input current limit according to detection results.

Input Current Limit Setting via ILIM

For safe operation, the MP2733 has an additional hardware pin (ILIM) to adjust the maximum input current limit. The limit can be set by connecting a resistor from ILIM to GND. The actual input current limit is the lower value between what is set by the ILIM pin and the value set by the I²C.

The input current limit set by the ILIM pin can be calculated with Equation (1):

$$I_{IN\_LIM} = \frac{120}{R_{ILIM}(k\Omega)}(A) \quad (1)$$

Battery Temperature Monitor in Charge Mode

The MP2733 continuously monitors the battery's temperature by measuring the voltage at the NTC pin. This value is typically determined by a negative temperature coefficient (NTC) thermistor and external voltage dividers. For the NTC thermistor, a hotter ambient temperature corresponds with a lower resistance and voltage ratio, and vice versa.

Figure 7 on page 24 shows an NTC protection circuit. The external resistor dividers and the internal reference resistor series are pulled up to the VNTC pin. The voltage ratios between the internal and external dividers are compared to determine whether an NTC protection has been triggered. The VNTC voltage (1.7V) is regulated by an LDO that is powered from VREF. The VNTC pin is available in both charge mode and On-the-Go (OTG) mode.

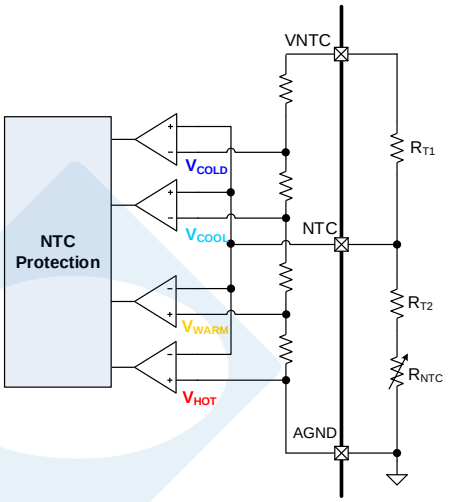


Figure 7: NTC Protection Circuit

The MP2733 provides standard and JEITA battery temperature monitoring, which can be selected via the NTC_TYPE bit. If the standard type is selected, and the external voltage ratio transitions from the high temperature threshold (V_{HOT}) to the low temperature threshold (V_{COLD}), this means that the battery temperature is out of the cold-to-hot range. The IC suspends charging and reports the NTC fault. Once the battery temperature is within the cold-to-hot temperature range again, charging resumes automatically.

If the JEITA type is selected, the MP2733 monitors four temperature thresholds:

1. Cold temperature threshold (T_{NTC} < 0°C, default)
2. Cool temperature threshold (0°C < T_{NTC} < 15°C, default)
3. Warm temperature threshold (45°C < T_{NTC} < 55°C, default)
4. Hot temperature threshold (T_{NTC} > 55°C, default)

For a given NTC thermistor, these temperatures correspond to the values for V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}, respectively. These voltage thresholds can be configured via REG16h, bits[5:0] to set different temperature ranges.

If V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, charging and timers are suspended. If V_{HOT} < V_{NTC} < V_{WARM}, then V_{BATT_REG} is reduced by 200mV (configured via REG16h, bit[7]). If V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to 16.7% of its set value, which can be configured via REG16h, bit[6]. Figure 8 shows the NTC window with JEITA control.

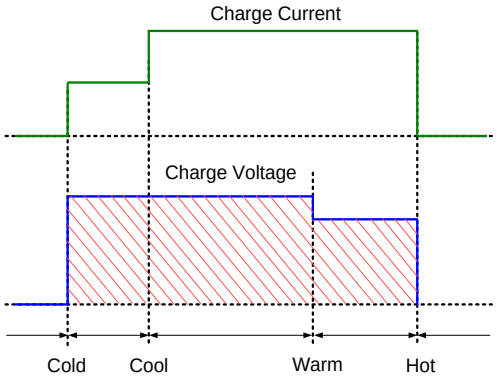


Figure 8: NTC Window with JEITA Control

The MP2733 provides PCB over-temperature (OT) monitoring. The PCB OT response is selected by the NTC_OPTION bit (REG02h, bit[1]). If this bit is set to 1, PCB over-temperature protection (OTP) is enabled. If this bit is set to 0 (the default setting), the battery temperature monitoring and corresponding protection features described above are utilized instead.

While monitoring OT conditions in the PCB, the IC continuously monitors the PCB temperature at the NTC pin. If the NTC pin's voltage is below the threshold that uses V_{HOT}, the DC/DC converter and battery FET turn off. Operation resumes once the NTC pin voltage returns to its normal value.

If the NTC thermistor is removed, NTC is pulled up to VNTC (see Figure 7). If the NTC voltage exceeds 95% of VNTC, then the NTC thermistor is detected to be floating. The MP2733 sends an INT signal to the host, and the RNTC FLOAT_STAT bit is set to 1.

Battery Temperature Monitor in On-the-Go (OTG) Boost Mode

In boost mode, the device monitors whether the battery temperature is within the V_{COLD} and V_{HOT} thresholds, unless boost mode temperature monitoring is disabled by setting EN_OTG NTC (REG02h, bit[5]) to 0. If the temperature goes outside of these thresholds, boost mode is suspended. Once the temperature returns to within these thresholds, boost mode resumes.

Charging STAT Indication

The MP2733 indicates the charging state on the open-drain STAT pin. Table 2 shows the STAT

status. The STAT pin function can be disabled by setting the STAT_EN bit to 0.

Table 2: Operation Indications

STAT	Charging State
Low	Charging
High	Charging complete, charge disabled, input OVP, battery discharge standby mode
Blinking at 1Hz	Charging suspended (battery OVP, system OVP, timer fault, NTC fault, or NTC float)

Interrupt to Host (INT)

The MP2733 also has an alert mechanism that can output an interrupt signal via the INT pin to notify the system of updates by outputting a 256μs, low-state INT pulse. Events that can trigger an INT output are listed below:

- Good input source detected
- DP/DM USB detection completed
- Input removed
- Charge completed
- NTC floats
- VINPPM or IINPPM has been reached
- Any fault in REG0Dh (watchdog timer fault, OTG fault, thermal shutdown, safety timer fault, battery OVP fault, NTC fault) has occurred

If a fault occurs, the charger sends out an INT signal. The fault status is not latched, meaning that the fault status is cleared when the fault condition is removed.

Safety Timer

The MP2733 provides both a pre-charge and complete charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 1 hour when V_{BATT} is below V_{BATT_PRE}. The complete charge safety timer starts when the battery enters constant current charge. The user can configure the constant current charge safety timer via CHG_TMR (REG08h, bits[2:1]). If the safety timer function is not used, it can be disabled by EN_TIMER (REG08h, bit[0]) while initializing charger configuration.

The safety timer is reset at the beginning of a new charging cycle. Before the safety timer expires, any of the actions listed below can reset the safety timer:

- A new charge cycle begins by either input insertion or automatic recharge
- Toggling the $\overline{CE}$ pin low, high, then low (charging enabled)
- Writing CHG_CONFIG (REG04h, bits[5:4]) from 00 to 01 (charging enabled)
- Writing EN_TIMER (REG08h, bit[0]) from 0 to 1 (safety timer enabled)

When safety timer expires, the safety timer fault bit (REG17h, bit[7]) is set to 1 and INT is asserted to the host. Writing the BG_EN bit (REG09h, bit[3]) from 1 to 0 (or re-inserting the input) re-enables input detection, clears the safety timer fault, and restarts the safety timer.

The MP2733 automatically adjusts or suspends the timer if any fault occurs. The timer is suspended if any of the following conditions are met:

- The battery enters supplement mode and $V_{BATT} < V_{SYS\_MIN}$
- Battery OVP occurs
- An NTC hot or cold fault occurs
- The NTC pin is floating
- 0 is written to EN_TIMER (REG08h, bit[0])

The MP2733 provides a way to double the remaining time left on the timer, which is enabled by the TMR2X_EN bit. If the input current limit, input voltage regulation, or thermal regulation threshold is reached, the remaining time on the timer is doubled when TMR2X_EN is enabled. Once the device is cleared of the conditions listed above, the remaining time returns to the original setting.

The safety timer does not operate in USB On-the-Go (OTG) mode.

Watchdog Timer

The MP2733 is a host-controlled device, but it can operate in a default mode without host control. In default mode, all registers are set to the default settings, and the WATCHDOG_FAULT command is set to 1.

In host-controlled mode, all the parameters can be configured by the host. To keep the device in host mode, the host has to periodically reset the

watchdog timer by setting the WATCHDOG_TIMER_RESET bit (REG08h, bit[3]) to 1 before the watchdog timer expires. If the watchdog timer expires, some of the registers are reset to their default values. See the I²C Register Map on page 29 to determine which registers are reset after the watchdog timer expires.

The following actions reset the watchdog timer and ensure that the IC recovers from a watchdog timer fault:

- Writing 1 to the WATCHDOG_TIMER_RESET bit (REG08h, bit[3])
- Toggling the WATCHDOG_TIMER_ENABLE bit (disable first, then enable)

Thermal Regulation and Thermal Shutdown

The MP2733 continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the internal junction temperature reaches the thermal regulation threshold (set by the TJ_REG bit), the MP2733 starts to reduce the charge current to prevent higher power dissipation. During thermal regulation, the THERM_STAT bit is set to 1.

If the junction temperature reaches the thermal shutdown threshold (T_{J_SHDN}, about 150°C), the MP2733 turns off the PWM step-down converter and the BATTFET. The THERMAL_SHUTDOWN bit in the fault register is set to 1, and an INT signal is asserted to the host. Once the junction temperature drops below the T_{J_SHDN} hysteresis threshold, the step-down converter and BATTFET resume normal operation.

Battery Standby Mode

If only the battery is connected and V_{BATT} exceeds the V_{BATT_UVLO} threshold, then the BATTFET turns on and connects the battery to the system. The 14mΩ BATTFET minimizes conduction loss during discharge. The MP2733's quiescent current goes as low as 40μA. The low on resistance and low quiescent current help extend battery runtime.

There is an over-current limit designed in the MP2733 to avoid system over-current conditions while the battery discharges. If the discharge current exceeds this limit (I_{DSCHG_LMT}) after a 50μs blanking time, the discharge FET turns off and enters hiccup mode. After a 600ms recovery time, the discharge FET turns on again. If the discharge current goes high to reach the internal fast-off current limit (14A), the BATTFET turns off immediately and enters hiccup mode.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the BATTFET for system reset or shipping mode. The MP2733 provides both system reset mode and shipping mode for different applications.

The system auto-reset function is selected by setting SYSRST_SEL to 1. Once the logic at DISC is pulled low for longer than 8s (set via the tDISC_L bit (REG0Ah, bits[1:0])) then the system is disconnected from the battery by turning off the BATTFET . After a 4s low period that can be configured by the tDISC_H bit (REG0Ah, bits[3:2]), the BATTFET automatically turns on (see Figure 9).

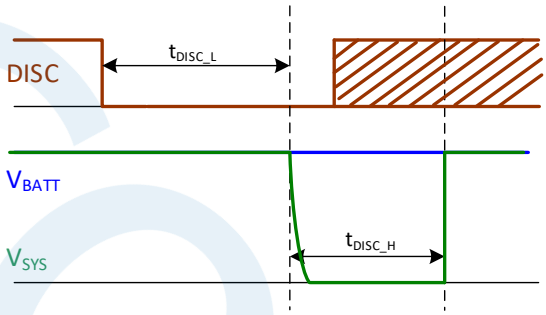


Figure 9: System Auto-Reset

The MP2733 can enter and exit shipping mode through the I²C control of the BATTFET_DIS bit (REG0Ah, bit[5]). Set BATTFET_DIS to 1 to turn off the BATTFET after a 10s delay. In battery standby mode, the delay time is configured by the t_{SM_DLY} bit. Set BATTFET_DIS to 0 to turn the BATTFET on again.

The MP2733 can also enter and exit shipping mode through the DISC pin by setting SYSRST_SEL to 0. If the logic at DISC is pulled low for longer than the time configured by the tDISC_L bit, the battery FET turns off and the device enters shipping mode. If the logic at DISC is pulled low again for time set by the tDISC_H bit, the battery FET turns on and the device exits shipping mode (see Figure 10 on page 27). Once the device exits shipping mode via the DISC pin,

BATTFET_DIS must be set to 0 to reset BATTFET control.

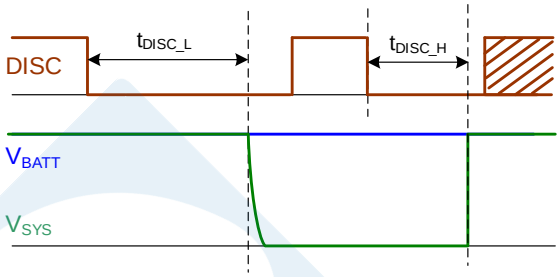


Figure 10: Shipping Mode via the DISC Pin

On-the-Go (OTG) Boost Function

The MP2733 can supply a regulated 5V output at the IN pin to power the peripherals. This output is compliant with USB On-The-Go (OTG) specifications. To ensure that the battery is not drained, the MP2733 does not enter OTG mode if the battery is below its under-voltage lockout (UVLO) threshold. To enable OTG mode, the input voltage at the IN pin must be below 1V.

Boost operation can be enabled when the CHG_CONFIG bit = 11 (REG04h, bits[5:4] = 11) and the OTG pin is high. The OTG output current limit can be configured by the IIN_DSCHG bit (REG03h, bits[1:0]). During boost mode, status register VIN_STAT (REG0Ch, bits[7:5]) changes to 111.

The following conditions must be met to enable boost operation:

- $V_{BATT} > V_{BATT\_UVLO\_OTG}$ (rising 3V)
- $V_{IN} < 1V$
- The OTG pin is high and CHG_CONFIG (REG04h, bits[5:4]) is set to 11

Boost mode is enabled after a 200ms delay.

Once OTG is enabled, the MP2733 boosts the PMID to 5V. Then the block FET (Q1) is linearly regulated with a 3A output current limit. If V_{IN} is charged above 4.4V within 6ms, the block FET fully turns on. Otherwise, the block FET turns off and the part goes into hiccup mode. After a 600ms off period, PMID tries to charge V_{IN} again.

The MP2733 provides OTG output short protection. If V_{IN} falls below 4V, the block FET and boost turn off, and the part enters hiccup mode. After a 600ms recovery time, OTG starts up again. When the OTG output is short, the fault register's OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host.

The device also provides OTG output voltage protection. Once V_{IN} exceeds V_{INOVP_DSCHG}, the MP2733 stops switching, the fault register OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host.

In boost mode, the MP2733 employs a fixed, 1.35MHz, PWM step-up switching converter. It switches from PWM mode to pulse-skip mode under light-load conditions.

Analog-to-Digital Converter (ADC)

The MP2733 integrates an 8-bit analog-to-digital converter (ADC), which is available in charge mode, OTG mode, or battery standby mode.

In charge mode, the ADC monitors the input voltage, input current, system voltage, battery voltage, charge current, and NTC voltage alternately. In OTG mode, the ADC monitors the input voltage, input current, system voltage, battery voltage, and NTC voltage alternately.

The ADC has two modes that can be selected by ADC_RATE (REG03h, bit[6]). If ADC_RATE is set to 0, the ADC starts working once ADC_START bit is set to 1. If ADC_RATE is set to 1, the ADC is always working.

In battery standby mode, the ADC is available by first setting EN_ADC_DSG (REG08h, bit[6]) to 1. Then the ADC can be controlled by the ADC_RATE and ADC_START bits.

Serial Interface

The IC uses an I²C-compatible interface to set the charging parameters and instantaneously report the device status. The I²C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbits/s) and fast mode (up to 400kbits/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. Start and stop conditions are always generated by the master. A start condition is defined as a high-to-

low transition on the SDA line while SCL is high. A stop condition is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 11).

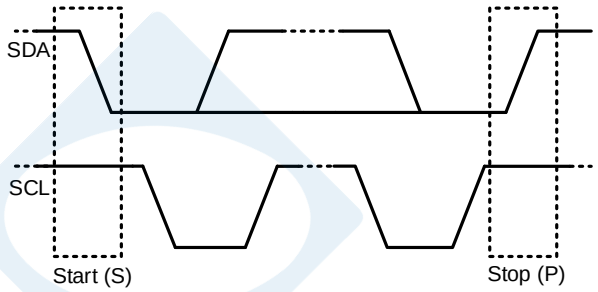


Figure 11: Start and Stop Conditions

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 12). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB).

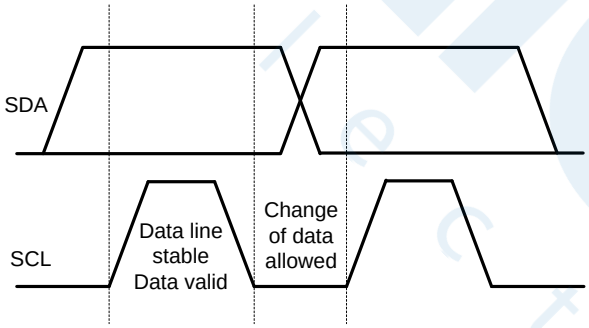


Figure 12: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the ninth clock, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start (Sr) condition to start a new transfer.

After the start condition, a slave address is sent. This address is 7 bits long, followed by the 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 13 shows the address bit arrangement.

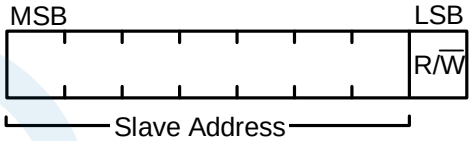


Figure 13: 7-Bit Address

Figure 14, Figure 15, Figure 16, Figure 17, and Figure 18 show the complete data transfer sequence.

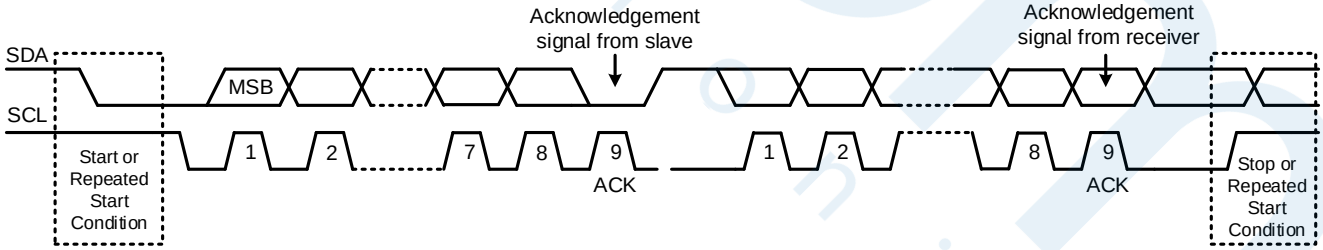


Figure 14: Data Transfer on the I²C Bus

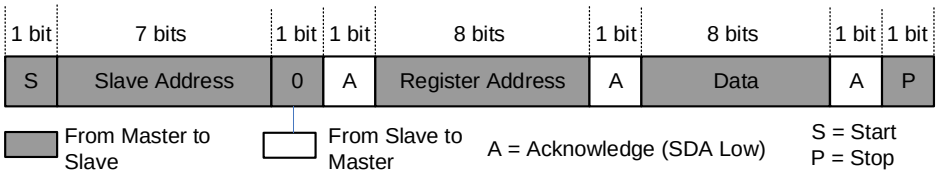


Figure 15: Single Write

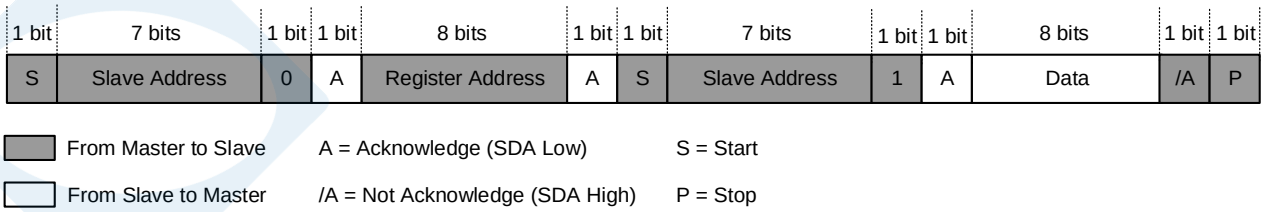


Figure 16: Single Read

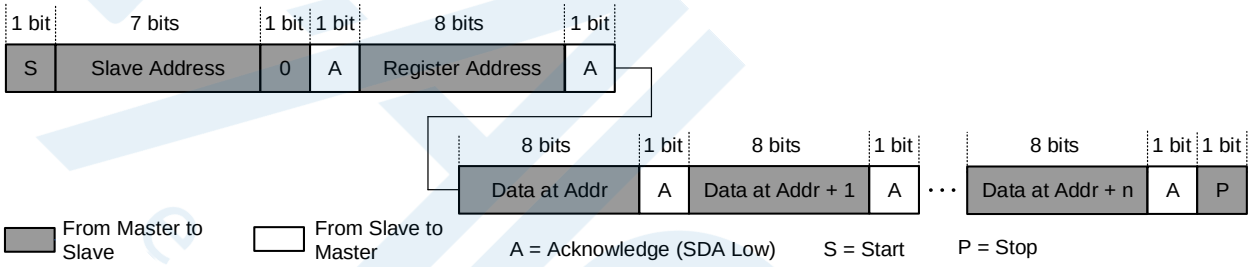


Figure 17: Multi-Write

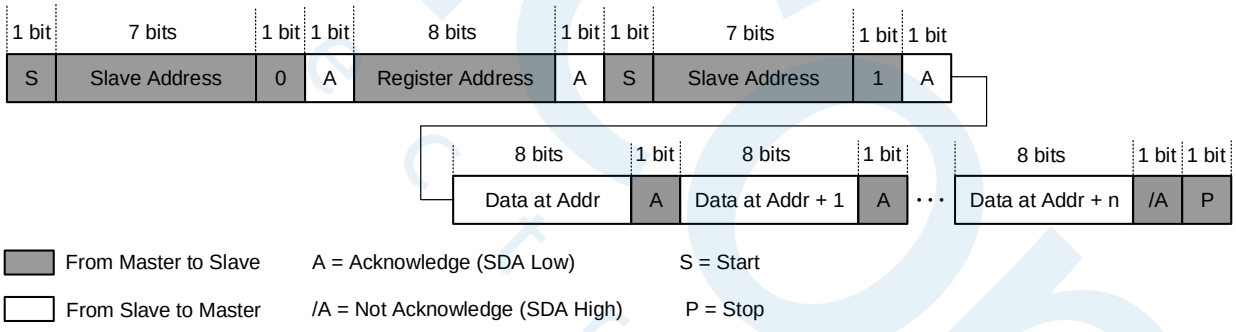


Figure 18: Multi-Read

I²C REGISTER MAP

IC Address 4Bh Register Name	Address	R/W	Description
REG00h	0x00	R/W	Input current limit setting.
REG01h	0x01	R/W	Input voltage regulation setting.
REG02h	0x02	R/W	NTC configuration and thermal regulation setting.
REG03h	0x03	R/W	ADC control and OTG configuration.
REG04h	0x04	R/W	Charge control and VSYS configuration.
REG05h	0x05	R/W	Charge current configuration.
REG06h	0x06	R/W	Pre-charge and termination current.
REG07h	0x07	R/W	Charge voltage regulation.
REG08h	0x08	R/W	Timer configuration.
REG09h	0x09	R/W	Bandgap setting.
REG0Ah	0x0A	R/W	BATTFET configuration.
REG0Bh	0x0B	R/W	INT mask and USB detection setting.
REG0Ch	0x0C	R	Status indicator.
REG0Dh	0x0D	R	Fault indicator.
REG0Eh	0x0E	R	Battery voltage ADC.
REG0Fh	0x0F	R	System voltage ADC.
REG10h	0x10	R	NTC voltage ADC.
REG11h	0x11	R	Input voltage ADC.
REG12h	0x12	R	Charge current ADC.
REG13h	0x13	R	Input current ADC.
REG14h	0x14	R	Power management status.
REG15h	0x15	R/W	DPM mask setting.
REG16h	0x16	R/W	JEITA configuration.
REG17h	0x17	R	Safety timer status and part number setting.

REG00h: Input Current Limit

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_HIZ	0	Y	Y	R/W	0: Disabled 1: Enabled	Enables Hi-Z mode. Set to 0 by default. This bit only turns off the DC/DC converter.
6	EN_LIM	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables the ILIM pin. This bit is set to 1 by default. The charger input current limit is the lower value between the IIN_LIM register setting and ILIM pin setting.
5	IIN_LIM[5]	0	Y	N	R/W	1600mA	This bits set the input current limit threshold. They have a 100mA offset, a 500mA default, and a 100mA to 3.25A range via the one-time programmable (OTP) memory. V_{IN} POR can reset I_{IN_LIM} to the default OTP threshold.
4	IIN_LIM[4]	0	Y	N	R/W	800mA	
3	IIN_LIM[3]	1	Y	N	R/W	400mA	
2	IIN_LIM[2]	0	Y	N	R/W	200mA	
1	IIN_LIM[1]	0	Y	N	R/W	100mA	
0	IIN_LIM[0]	0	Y	N	R/W	50mA	

REG01h: Input Voltage Regulation

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	REGISTER_ RESET	0	Y	N	R/W	0: Keep current setting 1: Reset	This bit is set to 0 by default.
6	VIN_MIN[6]	0	Y	N	R/W	6400mV	These bits set the input voltage limit threshold. They have a 3.7V offset, 3.7V to 15.2V range, and is set to 0000110 (4.3V) by default via the OTP. V_{IN} POR can reset V_{IN_MIN} to its default value via the OTP.
5	VIN_MIN[5]	0	Y	N	R/W	3200mV	
4	VIN_MIN[4]	0	Y	N	R/W	1600mV	
3	VIN_MIN[3]	0	Y	N	R/W	800mV	
2	VIN_MIN[2]	1	Y	N	R/W	400mV	
1	VIN_MIN[1]	1	Y	N	R/W	200mV	
0	VIN_MIN [0]	0	Y	N	R/W	100mV	

REG02h: NTC Configuration and Thermal Regulation

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	tSM_DLY	1	Y	Y	R/W	0: No delay 1: 10s delay	This bit sets the shipping mode entry delay time. It is set to 1 by default.
6	NTC_TYPE	1	Y	Y	R/W	0: Standard 1: JEITA	This bit is set to 1 by default.
5	EN_OTG_NTC	0	Y	Y	R/W	0: Disabled 1: Enabled	Enables OTG NTC. This bit is set to 0 by default.
4	EN_CHG_NTC	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables charge NTC. This bit is set to 1 by default.
3	TJ_REG[1]	1	Y	Y	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	These bits set the thermal regulation threshold. These bits are set to 11 by default.
2	TJ_REG[0]	1	Y	Y	R/W		
1	NTC_OPTION	0	Y	Y	R/W	0: Battery OTP 1: PCB OTP	NTC OTP selection bit. This bit is set to 0 by default via the OTP.
0	AICO_EN	0	Y	N	R/W	0: Disable AICO 1: Enable AICO	Enables automatic input current optimization (AICO). This bit is set to 0 by default.

REG03h: ADC Control and OTG Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ADC_START	0	Y	Y	R/W	0: Disable the ADC 1: Enable the ADC	Enables the ADC. This bit is set to 0 by default, and is read-only when ADC_RATE = 1. It remains high during ADC conversion.
6	ADC_RATE	0	Y	Y	R/W	0: One-shot conversion 1: Start continuous conversion	This bit sets the ADC conversion rate. It is set to 0 by default.
5	VIN_DSCHG[2]	0	Y	Y	R/W	400mV	This bit sets the On-the-Go (OTG) voltage. The offset is 4.8V, the default is 5.0V (010), and the range is 4.8V to 5.5V.
4	VIN_DSCHG[1]	1	Y	Y	R/W	200mV	
3	VIN_DSCHG[0]	0	Y	Y	R/W	100mV	
2	IIN_DSCHG[2]	0	Y	Y	R/W	000: 0.5A 001: 0.8A 010: 1.1A 011: 1.5A 100: 1.8A 101: 2.1A 110: 2.4A 111: 3.0A	These bits set the On-the-Go (OTG) current limit. They are set to 000 by default.
1	IIN_DSCHG[1]	0	Y	Y	R/W		
0	IIN_DSCHG[0]	0	Y	Y	R/W		

REG04h: Charge Control and VSYS Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	BAT_LOADEN	0	Y	Y	R/W	0: Disable $I_{BATLOAD}$ 1: Enable $I_{BATLOAD}$	Enables the battery load. This bit is set to 0 by default.
6	STAT_EN	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables the STAT pin. This bit is set to 1 by default.
5	CHG_ CONFIG[1]	0	Y	Y	R/W	00: Charge disabled 01: Charge enabled 10: Reserved 11: On-the-Go (OTG)	Charge configuration bit. It is set to 01 by default.
4	CHG_ CONFIG[0]	1	Y	Y	R/W		
3	VSYS_MIN[2]	1	Y	N	R/W	000: 3V 001: 3.15 010: 3.3V 011: 3.45V 100: 3.525V 101: 3.6V 110: 3.675V 111: 3.75V	These bits set the minimum system voltage. They have a 3V offset, 3V to 3.75V range, and are set to 101 by default.
2	VSYS_MIN[1]	0	Y	N	R/W		
1	VSYS_MIN[0]	1	Y	N	R/W		
0	VTRACK[0]	1	Y	N	R/W	0: 100mV 1: 150mV	Battery track voltage bit. It is set to 1 by default.

REG05h: Charge Current Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT_PRE	1	Y	Y	R/W	0: 2.8V 1: 3.0V	This bit sets the pre-charge to fast charge threshold. It is set to 1 by default.
6	ICC[6]	0	Y	Y	R/W	2560mA	These bits set the fast charge current. They have a 320mA offset, 320mA to 4520mA range, and are set to 0100110 (1840mA) by default.
5	ICC[5]	1	Y	Y	R/W	1280mA	
4	ICC[4]	0	Y	Y	R/W	640mA	
3	ICC[3]	0	Y	Y	R/W	320mA	
2	ICC[2]	1	Y	Y	R/W	160mA	
1	ICC[1]	1	Y	Y	R/W	80mA	
0	ICC[0]	0	Y	Y	R/W	40mA	

REG06h: Pre-Charge and Termination Current

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IPRE[3]	0	Y	Y	R/W	320mA	These bits set the pre-charge current. They have a 150mA offset, 150mA to 750mA range, and are set to 0010 (230mA) by default.
6	IPRE[2]	0	Y	Y	R/W	160mA	
5	IPRE[1]	1	Y	Y	R/W	80mA	
4	IPRE[0]	0	Y	Y	R/W	40mA	
3	ITERM[3]	0	Y	Y	R/W	320mA	These bits set the termination current. They have a 120mA offset, 120mA to 720mA range, and are set to 0010 (200mA) by default.
2	ITERM[2]	0	Y	Y	R/W	160mA	
1	ITERM[1]	1	Y	Y	R/W	80mA	
0	ITERM[0]	0	Y	Y	R/W	40mA	

REG07h: Charge Voltage Regulation

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT_REG[5]	1	Y	Y	R/W	640mV	These bits set the battery regulation voltage. They have a 3.4V offset, 3.4V to 4.67V range, and are set to 1010000 (4.2V) by default.
6	VBATT_REG[5]	0	Y	Y	R/W	320mV	
5	VBATT_REG[4]	1	Y	Y	R/W	160mV	
4	VBATT_REG[3]	0	Y	Y	R/W	80mV	
3	VBATT_REG[2]	0	Y	Y	R/W	40mV	
2	VBATT_REG[1]	0	Y	Y	R/W	20mV	
1	VBATT_REG[0]	0	Y	Y	R/W	10mV	
0	VRECH	0	Y	Y	R/W	0: 100mV 1: 200mV	Sets the battery recharge threshold (below V_{BATT_REG}). This bit is set to 0 by default.

REG08h: Timer Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_TERM	1	Y	Y	R/W	0: Disabled 1: Enabled	Termination enable bit. It is set to 1 by default.
6	EN_ADC_DSG	0	Y	Y	R/W	0: Disabled 1: Enabled	Enables the ADC function in standby mode. This bit is set to 0 by default.
5	WATCHDOG[1]	0	Y	N	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	These bits set the I²C watchdog timer limit. They are set to 01 by default. The watchdog function is not available when a battery is present.
4	WATCHDOG[0]	1	Y	N	R/W		
3	WATCHDOG_ TIMER_RESET	0	Y	Y	R/W	0: Normal 1: Reset	This bit is set to 0 by default, and returns to 0 after the timer resets.
2	CHG_TMR[1]	1	Y	Y	R/W	00: 5hrs 01: 8hrs 10: 12hrs 11: 20hrs	Constant current charge timer. These bits are set to 10 by default via the OTP.
1	CHG_TMR[2]	0	Y	Y	R/W		
0	EN_TIMER	1	Y	Y	R/W	0: Disabled 1: Enabled	Enables the safety timer. This bit is set to 1 by default.

REG09h: Bandgap

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	BG_EN	0	Y	Y	R/W	0: Enabled 1: Disabled	This bit is set to 0 by default. Setting this bit from 1 to 0 resets the input plug-in detection and safety timer.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG0Ah: BATTFET Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	SW_FREQ	0	Y	Y	R/W	0: 1.35MHz 1: 1MHz	Sets the switching frequency. This bit is set to 0 by default.
6	TMR2X_EN	1	Y	Y	R/W	0: Disable 2x extended safety timer 1: Enable 2x extended safety timer	2x timer enable bit. It is set to 1 by default.
5	BATTFET_DIS	0	N	N	R/W	0: Allow the BATTFET to turn on 1: Force the BATTFET off	This bit is set to 0 by default.
4	SYSRST_SEL	1	Y	N	R/W	0: Hardware reset 1: Software reset	System reset selection bit. If this bit is set to 0, the DISC pin is pulled low for a time. Bits[1:0] of this register turn off the BATTFET for a time until bits[3:2] turn on the BATTFET. If this bit is set to 1, the off time is selected by bits[3:2]. This bit is set to 1 by default.
3	tDISC_H[1]	1	Y	Y	R/W	00: 0.5s 01: 2s 10: 4s 11: 8s	These bits determine how long the DISC pin should be pulled low (BATTFET off time) to reset the BATTFET. These bits are set to 10 by default.
2	tDISC_H[0]	0	Y	Y	R/W		
1	tDISC_L[1]	0	Y	Y	R/W	00: 8s 01: 10s 10: 12s 11: 16s	These bits determine how long the DISC pin should be pulled low to turn off the BATTFET. These bits are set to 00 by default.
0	tDISC_L[0]	0	Y	Y	R/W		

REG0Bh: INT Mask and USB Detection

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	INT_MASK[1]	1	Y	Y	R/W	0: No INT during safety timer fault 1: INT during safety timer fault	This bit is set to 1 by default.
6	INT_MASK[0]	1	Y	Y	R/W	0: No INT during BAT_FAULT 1: INT in BAT_FAULT	This bit is set to 1 by default.
5	USB_DET_EN	0	Y	Y	R/W	0: No DP/DM detection 1: Force DP/DM detection	Enables USB DP/DM detection. This bit is set to 0 by default.
4	DM	0	Y	N	R/W	0: 3.3V 1: 0.6V	This bit is set to 0 by default, and is valid when REG0Bh, bits[2:1] = 11. It resets to 0 after 1 is written.
3	DP	0	Y	N	R/W	0: 0.6V 1: 3.3V	This bit is set to 0 by default, and is valid when REG0Bh, bits[2:1] = 11. It resets to 0 after 1 is written.
2	USB_FAST_CHG[1]	0	Y	N	R/W	00: DP = 0.6V, DM = Hi-Z 01: DP = 3.3V, DM = 0.6V 10: DP = 0.6V, DM = 0.6V 11: DP = 0.6V, DM = 3.3V	These bits set the fast charge value. They are set to 00 by default. After V_{IN} POR, these bits return to 00.
1	USB_FAST_CHG[0]	0	Y	N	R/W		
0	USB_FAST_CHG_RESET	0	Y	N	R/W	0: D+ recovers to V_{DP_SRC} 1: D+ is pulled down to zero	Resets USB fast charge by forcing the DP pin to 0V. This bit is set to 0 by default. It is valid in fast charge mode.

REG0Ch: Status Indicator

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VIN_STAT[2]	0	N	N	R	D+/D- version 000: No input 001: Unknown adapter 010: Apple 1.0A 011: Apple 2.1A 100: Apple 2.4A 101: SDP 110: CDP 111: DCP	These bits select the input source. They are set to 000 by default. V_{IN} POR resets VIN_STAT.
6	VIN_STAT[1]	0	N	N	R		
5	VIN_STAT[0]	0	N	N	R		
4	CHG_STAT[1]	0	N	N	R	00: Not charging 01: Trickle charge 10: Constant current charge 11: Charge done	These bits are set to 00 by default.
3	CHG_STAT[0]	0	N	N	R		
2	NTC_FLOAT_STAT	0	N	N	R	0: No NTC float 1: NTC float	This bit is set to 0 by default.
1	THERM_STAT	0	N	N	R	0: Normal 1: Thermal regulation	This bit is set to 0 by default.
0	VSYS_STAT	1	N	N	R	0: In V_{SYSMIN} regulation (BAT < V_{SYSMIN}) 1: Not in V_{SYSMIN} regulation (BAT > V_{SYSMIN})	This bit is set to 1 by default.

REG0Dh: Fault Indicator

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_ FAULT	0	N	N	R	0: Normal 1: Watchdog timer expiration	This bit is set to 0 by default.
6	OTG_FAULT	0	N	N	R	0: Normal 1: V_{IN} overload, or V_{IN} over-voltage protection (OVP), or the battery has an under-voltage condition	This bit is set to 0 by default.
5	INPUT_FAULT	0	N	N	R	0: Normal 1: Input OVP or no input	This bit is set to 0 by default.
4	THERMAL_ SHUTDOWN	0	N	N	R	0: Normal 1: Thermal shutdown	This bit is set to 0 by default.
3	BAT_FAULT	0	N	N	R	0: Normal 1: Battery OVP	This bit is set to 0 by default.
2	NTC_FAULT[2]	0	N	N	R	Buck mode 000: Normal 010: NTC warm 011: NTC cool 101: NTC cold 110: NTC hot Boost mode 000: Normal 101: NTC cold 110: NTC hot	These bits are set to 000 by default.
1	NTC_FAULT[1]	0	N	N	R		
0	NTC_FAULT[0]	0	N	N	R		

REG0Eh: Battery Voltage ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT[7]	0	N	N	R	2560mV	These bits set the analog-to-digital conversion (ADC) of the battery cell voltage. They have a 0V offset, and a 0V to 5.1V range.
6	VBATT[6]	0	N	N	R	1280mV	
5	VBATT[5]	0	N	N	R	640mV	
4	VBATT[4]	0	N	N	R	320mV	
3	VBATT[3]	0	N	N	R	160mV	
2	VBATT[2]	0	N	N	R	80mV	
1	VBATT[1]	0	N	N	R	40mV	
0	VBATT[0]	0	N	N	R	20mV	

REG0Fh: System Voltage ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VSYS[7]	0	N	N	R	2560mV	These bits set the analog-to-digital conversion (ADC) of the system voltage. They have a 0V offset, and a 0V to 5.1V range.
6	VSYS[6]	0	N	N	R	1280mV	
5	VSYS[5]	0	N	N	R	640mV	
4	VSYS[4]	0	N	N	R	320mV	
3	VSYS[3]	0	N	N	R	160mV	
2	VSYS[2]	0	N	N	R	80mV	
1	VSYS[1]	0	N	N	R	40mV	
0	VSYS[0]	0	N	N	R	20mV	

REG10h: NTC Voltage ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	NTC[7]	0	N	N	R	50.176%	These bits set the analog-to-digital conversion (ADC) of the NTC voltage. They have a 0% offset, and a 0% to 100% range.
6	NTC[6]	0	N	N	R	25.088%	
5	NTC[5]	0	N	N	R	12.544%	
4	NTC[4]	0	N	N	R	6.272%	
3	NTC[3]	0	N	N	R	3.136%	
2	NTC[2]	0	N	N	R	1.568%	
1	NTC[1]	0	N	N	R	0.784%	
0	NTC[0]	0	N	N	R	0.392%	

REG11h: Input Voltage ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VIN[7]	0	N	N	R	7680mV	These bits set the analog-to-digital conversion (ADC) of the input voltage. They have a 0V offset, and a 3.6V to 15.3V range.
6	VIN[6]	0	N	N	R	3840mV	
5	VIN[5]	0	N	N	R	1920mV	
4	VIN[4]	0	N	N	R	960mV	
3	VIN[3]	0	N	N	R	480mV	
2	VIN[2]	0	N	N	R	240mV	
1	VIN[1]	0	N	N	R	120mV	
0	VIN[0]	0	N	N	R	60mV	

REG12h: Charge Current ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ICHG[7]	0	N	N	R	2240mA	These bits set the analog-to-digital conversion (ADC) of the charge current. They have a 0A offset, and a 0A to 5.66A range.
6	ICHG[6]	0	N	N	R	1120mA	
5	ICHG[5]	0	N	N	R	560mA	
4	ICHG[4]	0	N	N	R	280mA	
3	ICHG[3]	0	N	N	R	140mA	
2	ICHG[2]	0	N	N	R	70mA	
1	ICHG[1]	0	N	N	R	35mA	
0	ICHG[0]	0	N	N	R	17.5mA	

REG13h: Input Current ADC

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IIN[7]	0	N	N	R	1702.4mA	These bits set the analog-to-digital conversion (ADC) of the input current. They have a 0A offset, and a 0A to 3.39A range.
6	IIN[6]	0	N	N	R	851.2mA	
5	IIN[5]	0	N	N	R	425.6mA	
4	IIN[4]	0	N	N	R	212.8mA	
3	IIN[3]	0	N	N	R	106.4mA	
2	IIN[2]	0	N	N	R	53.2mA	
1	IIN[1]	0	N	N	R	26.6mA	
0	IIN[0]	0	N	N	R	13.3mA	

REG14h: Power Management Status

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VINPPM_STAT	0	N	N	R	0: No PPM 1: VINPPM	This bit is set to 0 by default.
6	IINPPM_STAT	0	N	N	R	0: No PPM 1: IINPPM	This bit is set to 0 by default.
5	IIN_DPM[5]	0	N	N	R	1600mA	These bits have a 100mA offset, a 100mA to 3.25A range, and are set to 001000 by default.
4	IIN_DPM[4]	0	N	N	R	800mA	
3	IIN_DPM[3]	1	N	N	R	400mA	
2	IIN_DPM[2]	0	N	N	R	200mA	
1	IIN_DPM[1]	0	N	N	R	100mA	
0	IIN_DPM[0]	0	N	N	R	50mA	

REG15h: DPM Mask

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	AICO_STAT	0	N	N	R	0: No operation 1: AICO action	This bit is set to 0 by default.
6	VINPPM_INT_MASK[1]	1	Y	Y	R/W	0: No INT during VINPPM 1: INT during VINPPM	This bit is set to 1 by default.
5	IINPPM_INT_MASK[1]	1	Y	Y	R/W	0: No INT during IINPPM 1: INT during IINPPM	This bit is set to 1 by default.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG16h: JEITA Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	JEITA_VSET	1	Y	Y	R/W	0: V_{BATT_REG} minus 100mV 1: V_{BATT_REG} minus 200mV	This bit is set to 1 by default.
6	JEITA_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: 16.7% of I_{CHG}	This bit is set to 1 by default.
5	VTH_HOT	1	Y	Y	R/W	0: 34.0% (60°C) 1: 36.0% (55°C)	Sets the hot threshold, which is a percentage of VNTC. This bit is set to 1 by default. The thermistor is 103AT.
4	VTH_WARM[1]	0	Y	Y	R/W	00: 43.0% (40°C) 01: 40.0% (45°C) 10: 38.0% (50°C) 11: 36.0% (55°C)	These bits set the warm threshold, which is a percentage of VNTC. They are to 01 by default. The thermistor is 103AT.
3	VTH_WARM[0]	1	Y	Y	R/W		
2	VTH_COOL[1]	1	Y	Y	R/W	00: 72.0% (0°C) 01: 68.0% (5°C) 10: 64.0% (10°C) 11: 60.0% (15°C)	These bits set the cool threshold, which is a percentage of VNTC. They are to 11 by default. The thermistor is 103AT.
1	VTH_COOL[0]	1	Y	Y	R/W		
0	VTH_COLD	0	Y	Y	R/W	0: 72.0% (0°C) 1: 68% (5°C)	Sets the cold threshold, which is a percentage of VNTC. This bit is set to 0 by default. The thermistor is 103AT.

REG17h: Safety Timer Status and Part Number

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	SAFETY_TIMER	0	N	N	R	0: Normal 1: Safety timer expiration	This bit is set to 0 by default.
6	FAST_ CHARGE_ ADAPTER	0	N	N	R	0: Normal 1: Fast charge adapter	This bit is set to 0 by default.
5	OTG	0	N	N	R	0: Normal 1: On-the-Go (OTG)	This bit is set to 0 by default.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG18h (7)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IINLIM/VINMIN_ RESET_EN	0	N	N	N	0: I_{IN_LIM} and V_{IN_MIN} do not reset when V_{IN} POR 1: I_{IN_LIM} and V_{IN_MIN} reset when V_{IN} POR	This bit is set to 0 by default.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	VINOVP_CS	0	N/A	N/A	N/A	0: 16.8V 1: As per USB_FAST_CHG, bits[1:0] setting	This bit is set to 0 by default.
2	ADDRESS	0	N/A	N/A	N/A	0: 4Bh 1: 21h	This bit is set to 0 by default.
1	PFM_EN	0	N/A	N/A	N/A	0: Enabled 1: Disabled	Enables PFM when charging is disabled. This bit is set to 0 by default.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

Note:

7) This register is for the one-time programmable (OTP) memory. It is not accessible.

OTP MAP

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00	N/A		I_{IN_LIM}: 100mA to 3250mA/50mA step					
01	N/A	V_{IN_MIN}: 3.7V to 15.2V/100mV step						
05	N/A	I_{CC}: 320mA to 4520mA/40mA step						
07	V_{BATT_REG}: 3.4V to 4.67V/10mV step							N/A
08	N/A					CHG_TMR		N/A
18	IINLIM/VINMIN RESET_EN	N/A	N/A	N/A	VINOVP_CS	ADDRESS	PFM_EN	N/A

OTP DEFAULT

OTP Items	Default
I_{IN_LIM}	500mA
V_{IN_MIN}	4.3V
I_{CC}	1.84A
V_{BATT_REG}	4.2V
CHG_TMR	12hrs
INLIM/VINMIN RESET_EN	IIN_LIM and VIN_MIN not reset when VIN POR
VINOVP_CS	16.8V
ADDRESS	4Bh
PFM_EN	Enabled

APPLICATION INFORMATION

Setting the Input Current Limit

The input current limit (I_{IN_LIM}) is set according to the input power source. I_{IN_LIM} can be set through the I²C using the MP2733's GUI. If a user wants to set a current limit that cannot be set by the I²C, it can be set using the ILIM pin. Connect a resistor from the ILIM pin to AGND to program I_{IN_LIM}. The MP2733 selects the lower value between the I²C setting and the resistor setting. The ILIM pin resistance can be calculated with Equation (1) on page 22.

See Table 1 on page 22 to determine how to set I_{IN_LIM} for USB inputs.

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A smaller-value inductor is physically small, but results in higher ripple current, magnetic hysteretic loss, and output capacitance. A larger-value inductor provides lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

For the best results, the inductor ripple current should not exceed 30% of the maximum load current under the worst-case conditions. For the MP2733 to operate with a typical 5V input voltage, the maximum inductor current ripple occurs at the corner point between pre-charge and constant current charge. The inductance (L) can be estimated with Equation (2):

$$L=\frac{V_{IN}-V_{SYS}}{\Delta I_{L\_MAX}}\frac{V_{SYS}}{V_{IN}\times f_{SW}(MHz)}(\mu H) \quad (2)$$

Where V_{IN} is the input voltage, V_{SYS} is the system voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum inductor ripple current, (usually 30% of the CC charge current).

I_{PEAK} can be calculated with Equation (3):

$$I_{PEAK}=I_{LOAD(MAX)}\times\left(1+\frac{\Delta I_{L\_MAX}}{2}\right)(A) \quad (3)$$

The maximum charge current can be set to 4.5A, but the real charge current cannot reach this value due to the input current limit. For typical applications, the maximum inductor current ripple is set to 0.5A with a 5V input voltage, and the inductance is 1.5µH. Select a 1µH inductor for low-profile operation.

To optimize efficiency, choose an inductor with a low DC resistance.

Selecting the Input Capacitor

The converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are sufficient. Choose ceramic capacitors with X5R or X7R dielectrics.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{SYS}}{V_{IN}}\times\left(1-\frac{V_{SYS}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs when V_{IN} = $2V_{SYS}$, and I_{CIN} = I_{SYS} / 2. For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

For the MP2733, the RMS current in the input capacitor is from PMID to GND. This means a small, high-quality ceramic capacitor (e.g. 10µF) should be placed from VPMID to PGND, as close to the IC as possible. The remaining capacitor should be placed from VIN to GND.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge that prevents excessive voltage ripple at the input.

Selecting the Output Capacitor

In the typical application circuit, the output capacitor (C_{SYS}) is in parallel with the SYS load. C_{SYS} absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be below that of the system load to ensure that it properly absorbs the ripple current.

It is recommended to use a ceramic capacitor because its lower ESR and smaller size allow the ESR of the output capacitor to be ignored.

The output voltage ripple can be calculated with Equation (5):

$$\Delta R = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8\times C_{SYS}\times f_{SW}{}^{2}\times L}\% \quad (5)$$

To guarantee a ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g. 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

The output capacitance (C_{SYS}) can be calculated with Equation (6):

$$C_{SYS} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8\times f_{SW}{}^{2}\times L\times \Delta R} \quad (6)$$

For example, if V_{IN} = 5V, V_{SYS} = 3.7V, L = 1µH, f_{SW} = 1.35MHz, and ΔR = 0.1%, choose a 22µF ceramic capacitor.

Selecting the NTC Resistor

Figure 7 on page 24 shows an external resistor divider reference circuit that limits the low-temperature threshold (V_{COLD}) and high-temperature threshold (V_{HOT}). For a given NTC thermistor, select the appropriate R_{T2} and R_{T1} values to set the NTC window, calculated with Equation (7) and Equation (8), respectively:

$$R_{T2} = \frac{R_{NTC\_HOT}\times V_{COLD}\times(1-V_{HOT})-R_{NTC\_COLD}\times V_{HOT}\times(1-V_{COLD})}{V_{HOT}-V_{COLD}} \quad (7)$$

$$R_{T1} = \frac{(1-V_{COLD})\times(R_{NTC\_COLD}+R_{T2})}{V_{COLD}} \quad (8)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the high temperature of the required temperature operation range, and R_{NTC_COLD} is the value of the NTC resistor at the low temperature.

R_{T1} and R_{T2} allow the high-temperature limit and low-temperature limit to be configured independently. With this feature, the MP2733 can operate within most NTC resistor and temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of NTC resistor. For example, a 103AT thermistor must have the following electrical characteristics:

- At 0°C, R_{NTC_COLD} = 27.28kΩ
- At 60°C, R_{NTC_HOT} = 3.02kΩ

V_{HOT} is selected to be 34% of VNTC and V_{COLD} is selected to be 72% of VNTC via the REG16h register. Using Equation (7) and Equation (8), R_{T1} = 11.8kΩ and R_{T2} = 3.06kΩ.

PCB Layout Guidelines

Proper PCB layout is critical to meet specified noise rejection requirements and high efficiency. For the best results, follow the guidelines below:

1. Route the power stages adjacent to their grounds. Minimize the high-side switching node (SW and inductor), the trace lengths in the high-current paths, and the current-sense resistor trace.
2. Keep the switching node short, and route it away from all small control signals, especially the feedback network.
3. Place the input capacitor as close as possible to the PMID and PGND pins.
4. Place the output inductor close to the IC, and connect the output capacitor between the inductor and PGND of the IC.
5. For high-current applications, the pins for the power pads (IN, SW, SYS, BATT, and PGND) should be connected to as much copper on the board as possible. This improves thermal performance by conducting heat away from the IC.
6. Connect a ground plane directly to the return of all components through via holes. It is also recommended to put via holes inside the PGND pads for the IC, if possible. A star ground design approach is recommended to keep the circuit block currents isolated (high-power PGND and low-power, small signal AGND) which reduces noise coupling and ground-bounce issues. A single ground plane for this design offers good results. With a small layout and a single ground plane, there is no ground-bounce, and having the components separated minimizes coupling between signals and stability requirements.
7. Pull the connection wire from the MCU (I²C) far from the SW mode and copper regions.
8. Place SCL and SDA in close parallel.

TYPICAL APPLICATION CIRCUIT

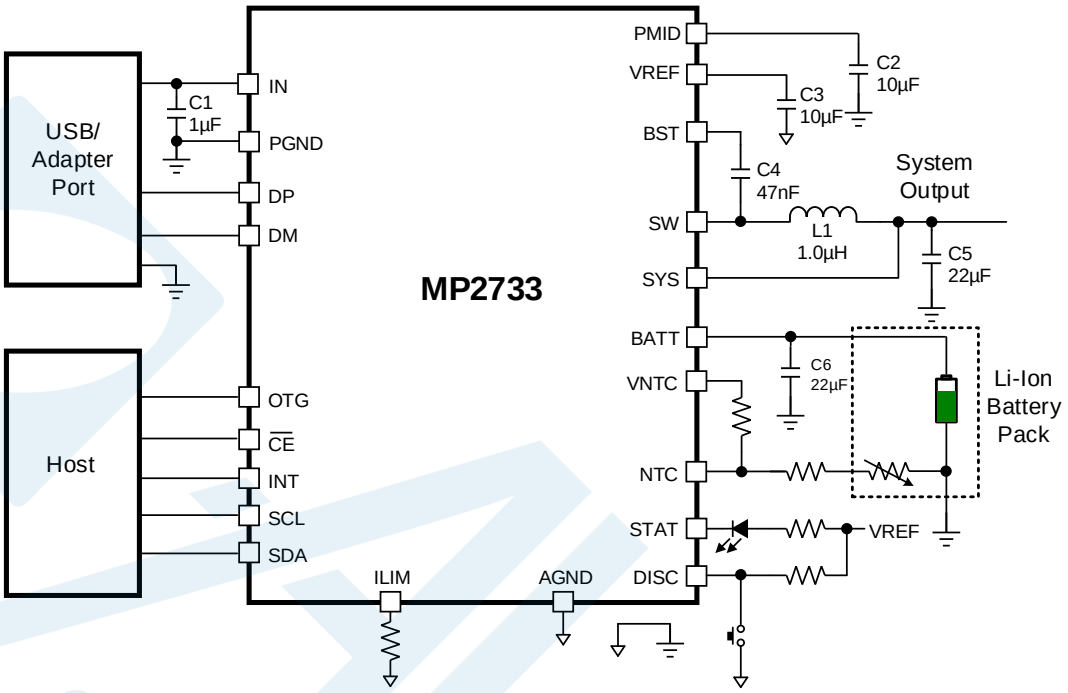


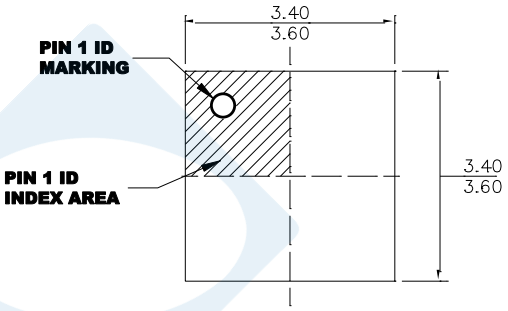
Figure 19: Typical Application Circuit

Table 3: Key BOM of Figure 19

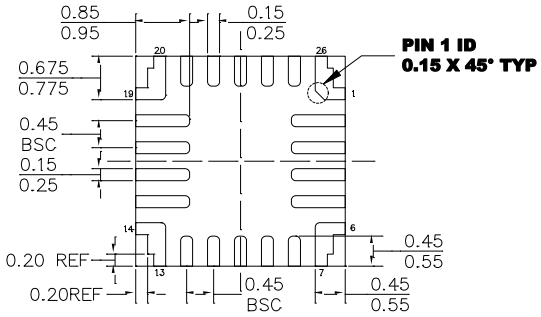
Qty	Ref	Value	Description	Package	Manufacturer
1	C1	1µF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C2	10µF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C3	10µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C4	47nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C5	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C6	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	L1	1.0µH	>9.6A	N/A	Any

PACKAGE INFORMATION

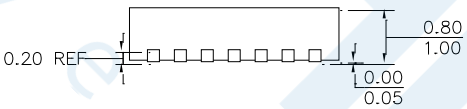
QFN-26 (3.5mmx3.5mm)



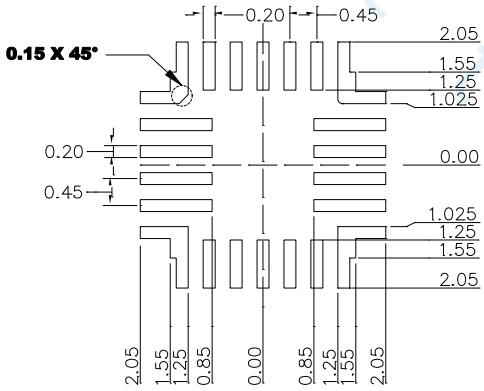
TOP VIEW



BOTTOM VIEW



SIDE VIEW

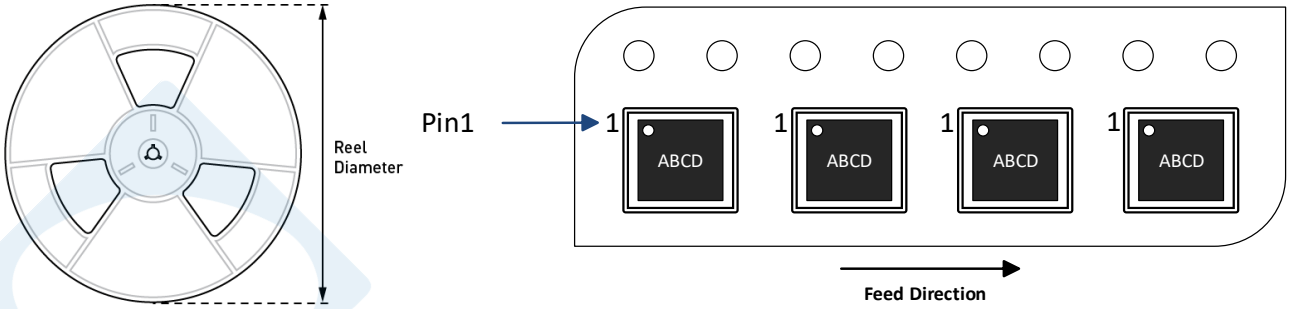


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader/ Reel
MP2733GQC -xxxx–Z	QFN-26 (3.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm	125 & 125

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/7/2021	Initial Release	-