KTB8375/KTB8376

4.5V - 24V Input, 6A Synchronous Buck Regulator with I²C Interface

Features

- Wide VIN Range: 4.5V to 24V
- Continuous Output Current: 6A
- I²C Control Interface
- Adjustable Output Voltage from 0.55V to 6V
- Integrated High-side / Low-side FETs
- Advanced Adaptive On-Time Control
- Fast Transient Response
- ±1% Feedback Voltage Reference 0.5V (at 25°C)
- Low Shutdown Supply Current
- Low Quiescent Current
- High Efficiency in Light Load and Heavy Load
- Adjustable Switching Frequency up to 2MHz
- Programmable Mode Forced-PWM or Auto-Skip
- Built-in Cycle-by-Cycle Current Limit, Short Circuit Protection, Input UVLO, Output Under-Voltage Protection, Output Over-Voltage Protection, and Thermal Shutdown Protection
- Flip Chip 12-pin QFN (2.5mm x 3.0mm) Package

Applications

- Telecom & Networking, Point-of-Load (POL)
- Tablets, PCs, notebooks, Mobile Internet Devices, Docking Stations
- Servers, Cloud-Computing, Storage
- Drones, Gaming Consoles

Brief Description

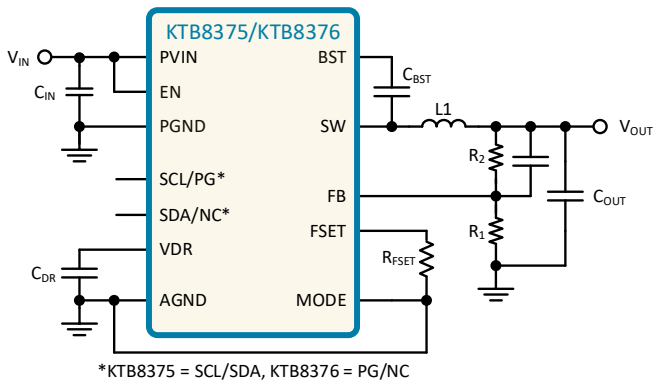
The KTB8375 and KTB8376 are 6A synchronous buck regulators with integrated high-side and low-side power MOSFETs. The device operates over a wide input voltage range from 4.5V to 24V to support a variety of applications.

The KTB8375/KTB8376 employs Kinetic proprietary advanced adaptive on-time (AOT) control for fast transient response and high output voltage accuracy. This control technique eliminates external loop compensation network and allows the use of ceramic output capacitors without ripple-generating circuitry. This feature enables a very small total solution size and makes the KTB8375/KTB8376 easy to use.

The KTB8375/KTB8376 device features an internal soft-start function to limit inrush current during start-up. The output voltage can be adjusted with a feedback resistor divider connected to the FB pin. The device has comprehensive built-in protection features including input voltage UVLO, high-side cycle-by-cycle peak current limit, reverse current protection, short-circuit protection, output over-voltage protection, and thermal shutdown.

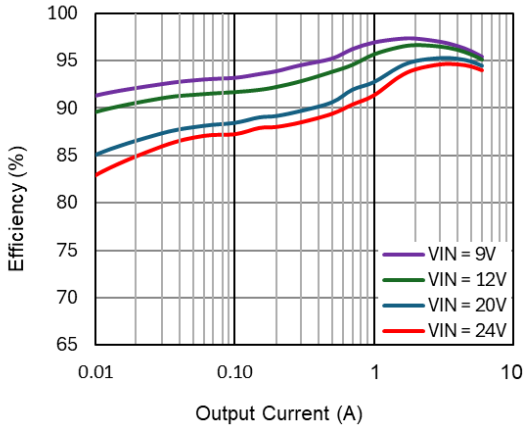
The KTB8375/KTB8376 is available in a thermal-enhanced flip chip QFN (2.5mm x 3.0mm x 0.55mm) Package.

Typical Application



*KTB8375 = SCL/SDA, KTB8376 = PG/NC

Efficiency vs Load (VOUT = 5V, f_{SW} = 500KHz)



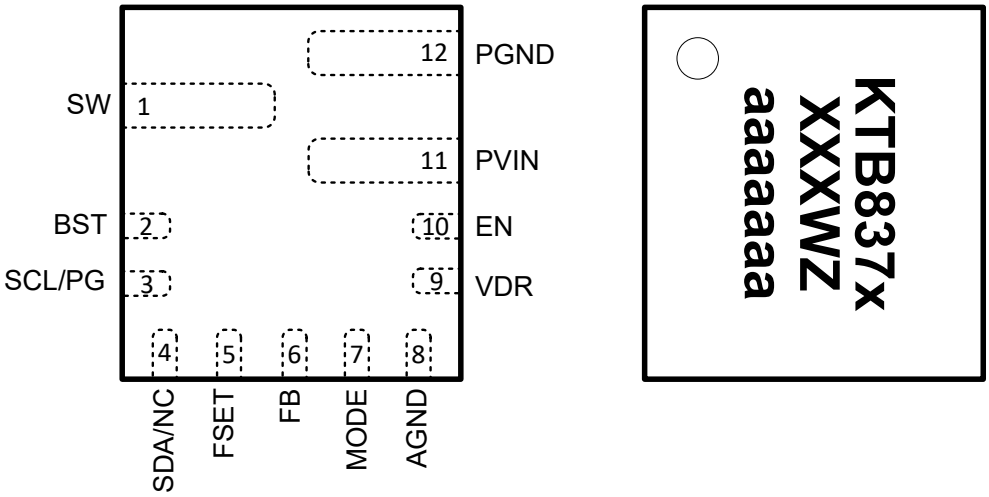
Ordering Information

Part Number	Marking[1]	Interface	Output Discharge	Package
KTB8375EUFB-TA	TIXWZ aaaaaaa	I²C, with SDA & SCL pins	Yes	QFN-12FC
KTB8375EUFB-1-TA[2]	XXXWZ aaaaaaa		No	
KTB8376EUFB-TA[2]	XXXWZ aaaaaaa	No I²C, with PG pin	Yes	
KTB8376EUFB-1-TA[2]	XXXWZ aaaaaaa		No	

Pinout Diagram

Flip Chip QFN-12

Top View



12-Pin 2.5mm x 3.0mm
FC-QFN Package, 0.4mm pitch

Top Mark
XX = Device ID, XWZ = Wafer Date Code
aaaaaaa = Assembly Tracking Code

1. XX = Device ID, XWZ = Wafer Date Code, aaaaaaa = Assembly Tracking Code.
2. Future version – consult Kinetic Technologies authorized representative for availability.

Pin Descriptions

Pin #	Name	Function
1	SW	Switching Node pin – Internally Connected to the High-side MOSFET Source and Low-side MOSFET Drain. This pin is connected to the buck regulator inductor.
2	BST	Boost Capacitor – Use for charge pump gate driver. Place a 0.1µF capacitor between BST pin and SW pin.
3	SCL/PG	For KTB8375: SCL Clock – I^2C digital Input. For KTB8376: PG Power Good, Open-drain output indicating VOUT is within set limits.
4	SDA/NC	For KTB8375: SDA Data – I^2C Data digital I/O. For KTB8376: No Connection.
5	FSET	Frequency Setting pin – Adjust switching frequency f_{SW} using a resistor to ground.
6	FB	Feedback pin – Output voltage feedback based on resistor divider.
7	MODE	MODE option selection input: 1. MODE pin is tied high for Forced-PWM (FPWM). 2. MODE pin is tied to ground for Auto-Skip Mode.
8	AGND	Analog Ground – Used for analog circuit.
9	VDR	Driver LDO output voltage – Power stage driver supply voltage. Place a 1µF capacitor between VDR pin and AGND.
10	EN	Enable pin – Chip enable logic input.
11	PVIN	Power Voltage Input – Input voltage for buck regulator. Connect to a power rail voltage. Place a 20µF capacitor or higher between PVIN pin and PGND.
12	PGND	Power Ground – Used for buck regulator.

Absolute Maximum Ratings[3]

Symbol	Description	Value	Units
V_{PVIN}, V_{EN}	PVIN, EN to PGND	-0.3 to 28	V
	PGND to AGND	-0.3 to 0.3	V
V_{SW}	SW to PGND	-0.3 to (PVIN +0.3)	V
V_{BST}	BST to SW	-0.3 to 5.5	V
V_{FB}	FB to AGND	-0.3 to 5.5	V
V_{VDR}	VDR to AGND	-0.3 to 5.5	V
V_{IO}	FSET, MODE to AGND	-0.3 to 5.5	V
	SCL, SDA to AGND	-0.3 to 5.5	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{STO}	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[4]

Symbol	Description	Value	Units
V_{ESD_HBM}	Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001-2017 (all pins)	±2000	V
V_{ESD_CDM}	Charged device model (CDM), JEDEC JESD22C101, (all pins)	±500	V

Thermal Capabilities[5]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	34	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ ($T_J = 125°C$)	2.9	W

Recommended Operating Conditions

Symbol	Description	Value	Units
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_{J_MAX}	Recommended Maximum Operating Junction Temperature	-40 to 125	°C

3. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
4. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied for T_J = -40°C to +125°C, and V_{IN} = 4.5V to 24V. Typical values are specified at T_A = +25°C and V_{IN} = 12V.

Supply Specifications (PVIN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PVIN}	Input Voltage Operating Range		4.5		24	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} rising threshold	3.9	4.2	4.45	V
		Hysteresis		150		mV
I_{PVIN}	PVIN Supply Current	EN = High, VIN=12V, Non-switching		45		µA
		EN = High, VIN = 12V, Auto-Skip, VOUT = 3.3V		65		µA
		EN = High, VIN = 12V, FPWM, VOUT = 3.3V, f_{SW} = 500kHz		23		mA
I_{SHDN}	PVIN Shutdown Current	EN = Low, T_A = 25°C Auto Discharge enabled[7]		4.5		µA
		EN = Low, T_A = 25°C Auto Discharge disabled		1.3		µA

Supply Specifications (VDR)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DR}	Driver output voltage	V_{IN} > 5V, I_{VDR} ≤ 10mA load		4.0		V

Logic Pin Specifications (EN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN)		2.0			V
V_{IL}	Input Logic Low (EN)				0.4	V
I_{I_LK}	Input Logic Leakage (EN)	T_A = 25°C, V_{EN} = 5V		5		µA

Logic Pin Specifications (MODE)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH_MODE}	Input Logic High (MODE)		2.5			V
V_{IL_MODE}	Input Logic Low (MODE)				1.0	V

6. Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization and correlation with statistical process controls.

7. Please see Ordering Information for Auto Discharge option part numbers.

Electrical Characteristics (continued)[8]

Unless otherwise noted, the *Min* and *Max* specs are applied for T_J = -40°C to +125°C, and V_{IN} = 4.5V to 24V. Typical values are specified at T_A = +25°C and V_{IN} = 12V.

I2C-Compatible Interface Specifications (SCL, SDA), for KTB8375 only

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High Threshold		1.1			V
V_{IL}	Input Logic Low Threshold				0.4	V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
T_1	SCL clock period		2.5			µs
T_2	Data out stable after SCL high		100			ns
T_3	Data out stable after SCL low		0			ns
T_4	SDA high hold time after SCL high (Start)		100			ns
T_5	SDA low setup time to SCL low (Stop)		100			ns

Logic Pin Specifications (PG), for KTB8376 only

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PG_OL}	Output Logic Low (PG)	I_{PG_SINK} = 100µA			0.4	V
I_{PG_LK}	Output Logic Leakage (PG)	T_A = 25°C, V_O = 5.5V		0.01	1	µA
V_{PG_UV}	Output Voltage Power-Good Under-Voltage Threshold	Percentage of nominal V_{OUT}		80		%
V_{PG_OV}	Output Voltage Power-Good Over-Voltage Threshold	Percentage of nominal V_{OUT}		120		%

Thermal Shutdown Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{J_SHDN}	IC Junction Thermal Shutdown	T_J rising		160		°C
		Hysteresis		15		

8. Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied for T_J = -40°C to +125°C, and V_{IN} = 4.5V to 24V. Typical values are specified at T_A = +25°C and V_{IN} = 12V.

Buck Regulator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Output voltage setting range		0.55		6	V
V_{FB}	Feedback regulation voltage	T_A = 25°C, FPWM	495	500	505	mV
V_{FB_DET}	Feedback 40% Under-voltage threshold detection			200		mV
I_{OUT_max}	Maximum Continuous Output Current		6			A
T_{on-min}	Minimum ON Time			50		ns
$T_{off-min}$	Minimum OFF Time			130		ns
I_{peak}	High-Side Switch Peak-Current Limiting Threshold		8.3	9.7		A
I_{valley}	Low-Side Switch Valley-Current Limiting Threshold		6.2	7.3		A
t_{-Hoff}	Hiccup OFF Time			12		ms
I_{ZCD}	Current threshold to detect Auto Skip			0		mA
I_{rev}	Low-Side Reverse Current Limiting Threshold		-2			A
R_{dson_HSD}	High-Side Switch On-Resistance			19		mΩ
R_{dson_LSD}	Low-Side Switch On-Resistance			11		mΩ
R_{sw_DIS}	SW Active Discharge Resistance	Auto Discharge enabled[10] (EN low)		140		Ω
f_{SW_RANGE}	Switching Frequency Setting		500		2000	kHz
f_{SW}	Switching Frequency	R_{FSET} = 150kΩ[11], CCM mode		500		kHz
V_{OUT_TR}	Load Transient	V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 500kHz, FPWM mode, Load step = 0 to 6A, Slew rate = 1A/µs (check BOM)		50		mV
t_{SS_DELAY}	Soft-Start Delay	Delay from EN high to Soft-Start starts		1		ms
t_{SS}	Soft-Start Time	Time duration from VOUT start rising to 90% of VOUT regulation		1.4		ms

9. Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization, and correlation with statistical process controls.

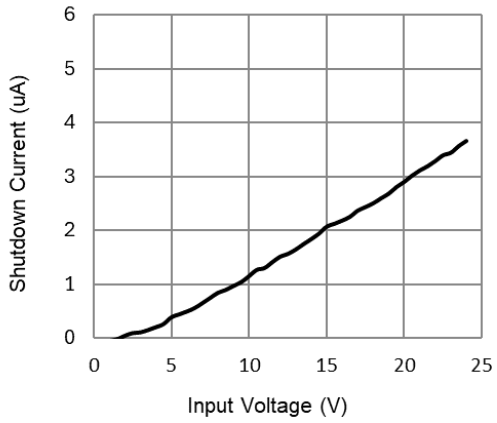
10. Please see Ordering Information for Auto Discharge option part numbers.

11. Please see Applications Information section for setting the switching frequency.

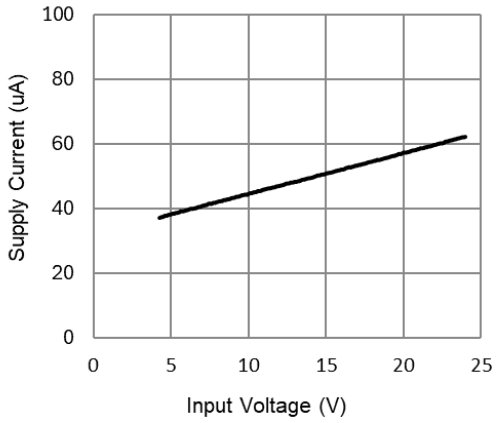
Typical Characteristics

VIN = 12V, VOUT = 3.3V, f_{SW} = 500kHz, EN = High, MODE = AGND, COUT = 22µF + 22µF and T_A = 25°C, unless otherwise specified.

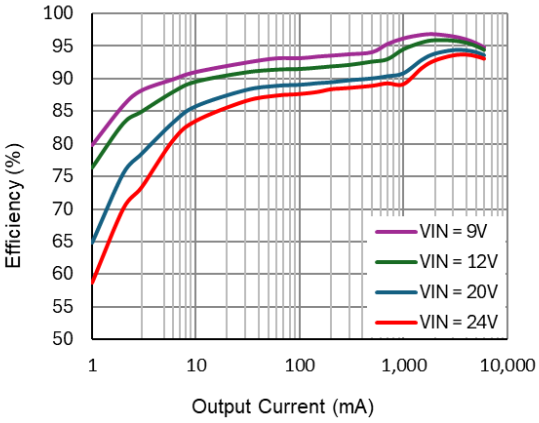
Shutdown Current vs VIN (Auto Discharge off)
(EN = GND)



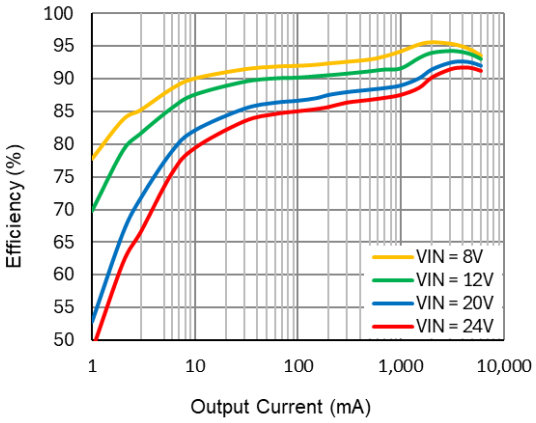
VIN Supply Current vs VIN
(no load, EN = High, non-switching VOUT)



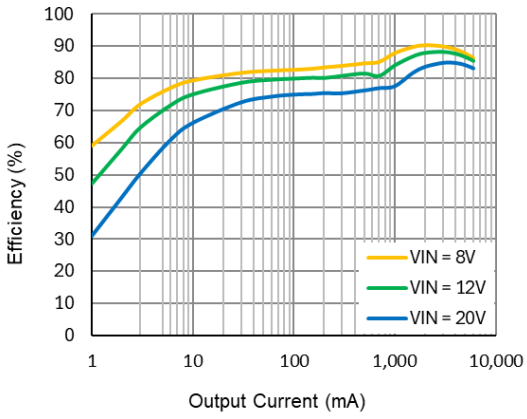
Efficiency vs. Output Current (VOUT = 5.0V)
L = 3.3µH, fsw = 500kHz, Auto-Skip mode



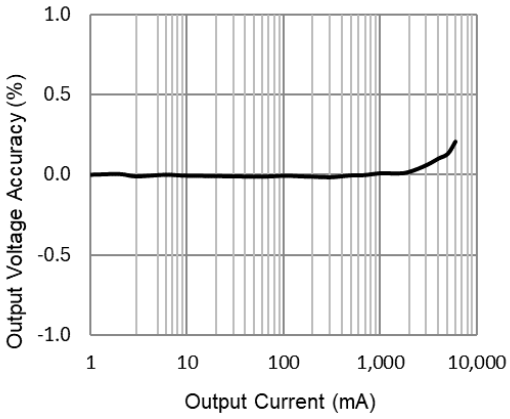
Efficiency vs. Output Current (VOUT = 3.3V)
L = 2.2µH, fsw = 500kHz, Auto-Skip mode



Efficiency vs. Output Current (VOUT = 1.0V)
L = 1.0µH, fsw = 500kHz, Auto-Skip mode



Load Regulation (FPWM, VOUT = 5V)
VIN = 12V

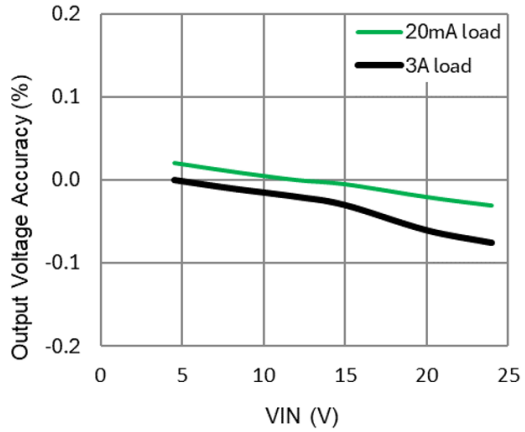


Typical Characteristics

VIN = 12V, VOUT = 3.3V, f_{SW} = 500kHz, EN = High, MODE = AGND, COUT = 22µF + 22µF and T_A = 25°C, unless otherwise specified.

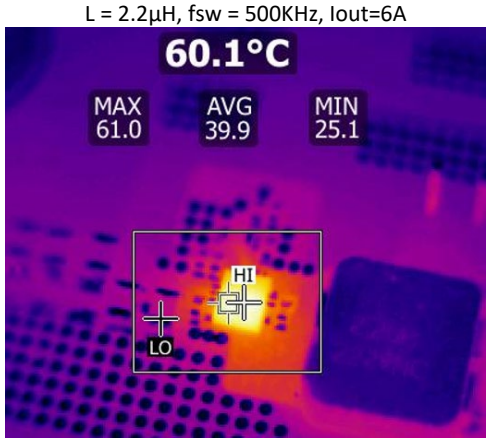
Line Regulation (VOUT = 1.0V)

L = 1.0µH, fsw = 500kHz, FPWM mode



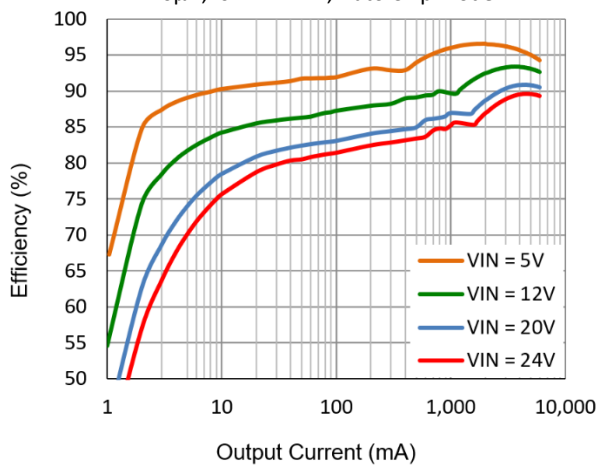
Thermal Performance at Full Load (Vin=12V VOUT = 3.3V)

L = 2.2µH, fsw = 500KHz, Iout=6A



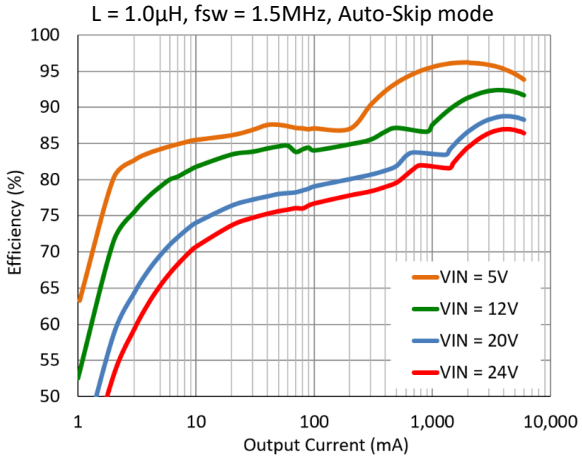
Efficiency vs. Output Current (VOUT = 3.3V)

L = 1.0µH, fsw = 1MHz, Auto-Skip mode



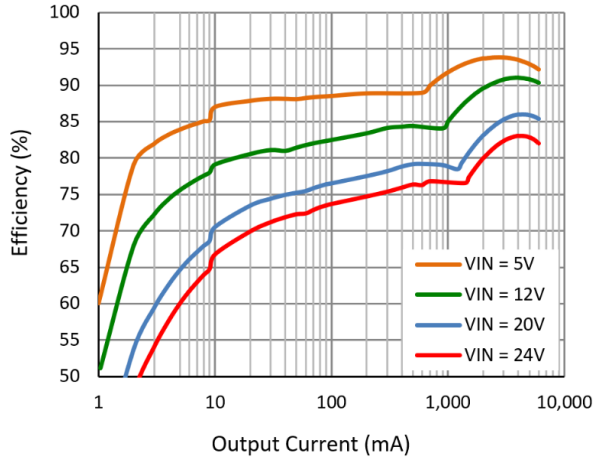
Efficiency vs. Output Current (VOUT = 3.3V)

L = 1.0µH, fsw = 1.5MHz, Auto-Skip mode



Efficiency vs. Output Current (VOUT = 3.3V)

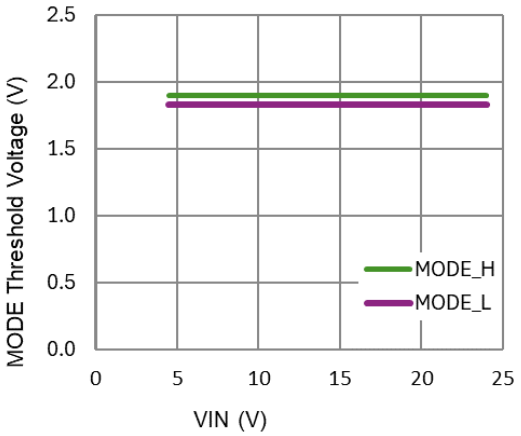
L = 0.82µH, fsw = 2MHz, Auto-Skip mode



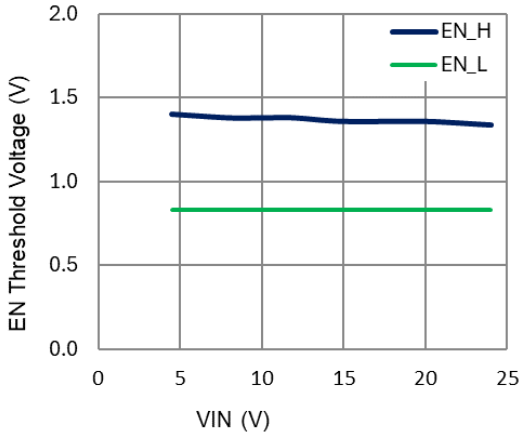
Typical Characteristics

VIN = 12V, VOUT = 5.0V, f_{SW} = 500kHz, EN = High, MODE = AGND, COUT = 22µF + 22µF and T_A = 25°C, unless otherwise specified.

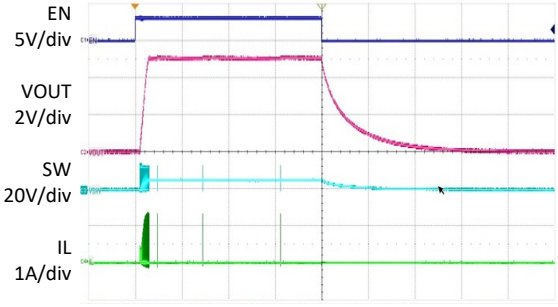
MODE pin Threshold Voltage vs VIN



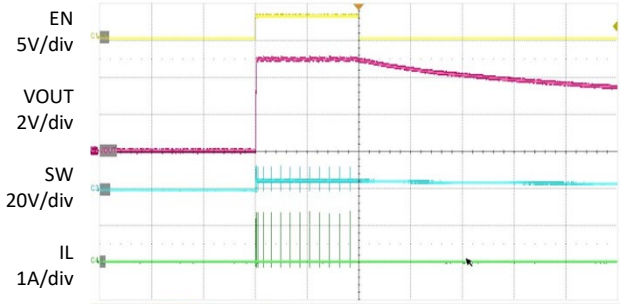
EN pin Threshold Voltage vs VIN



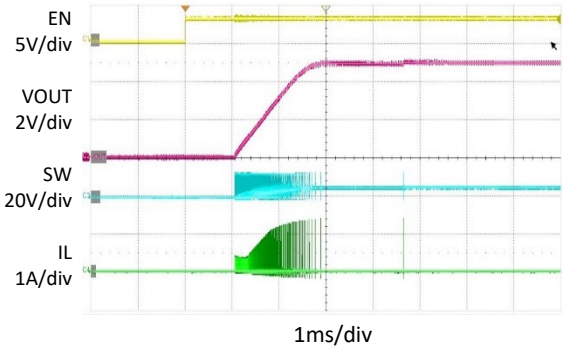
Turn-on with Enable in Auto-Skip Mode
No load (VOUT Discharge Enabled)



Turn-on and off with Enable in Auto-Skip Mode
No Load (VOUT Discharge Disabled)



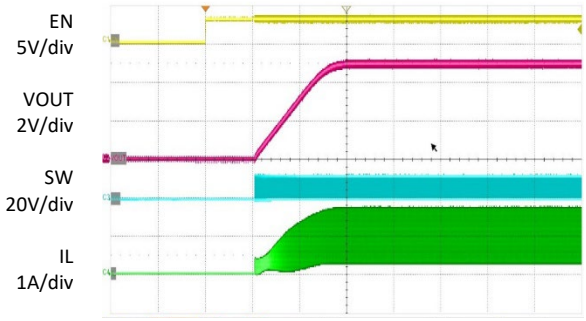
Turn-on with Enable in Auto-Skip Mode
No load



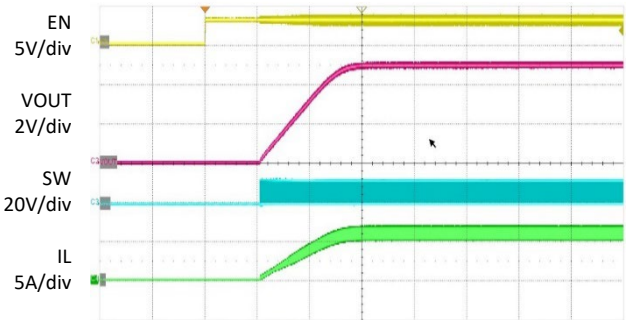
Typical Characteristics

VIN = 12V, VOUT = 5.0V, f_{SW} = 500kHz, EN = High, MODE = AGND, COUT = 22µF + 22µF, L = 3.3µH and T_A = 25°C, unless otherwise specified.

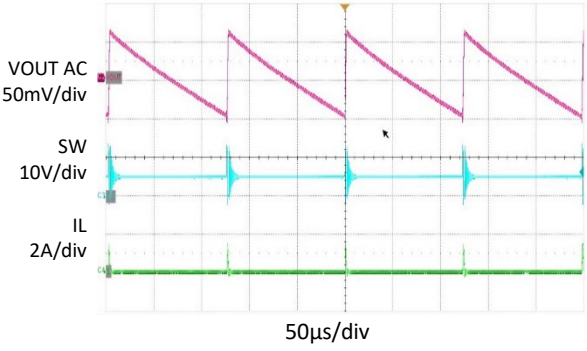
Turn-on with Enable in FPWM Mode
1A Load



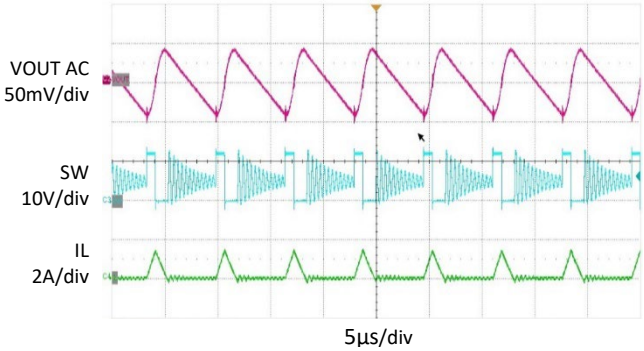
Turn-on with Enable in FPWM Mode
6A Load



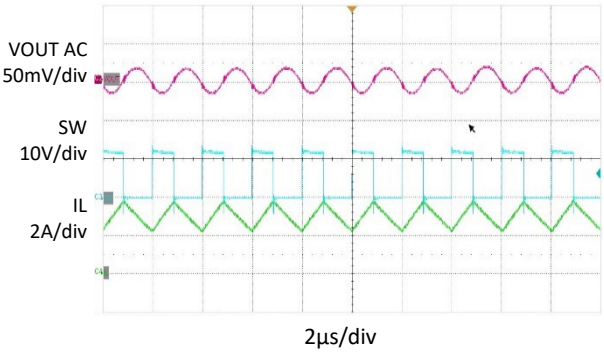
Switching Waveform 10mA Load
in Auto-Skip



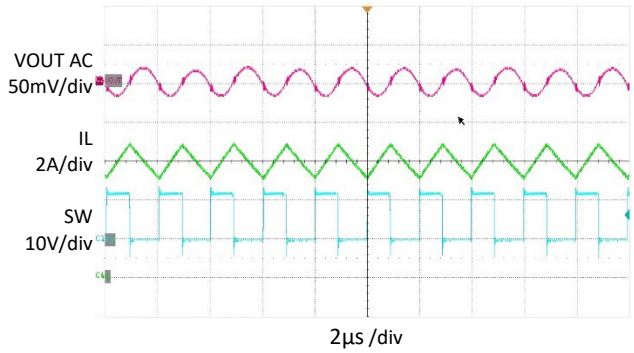
Switching Waveform 200mA Load
in Auto-Skip



Switching waveform 3A load



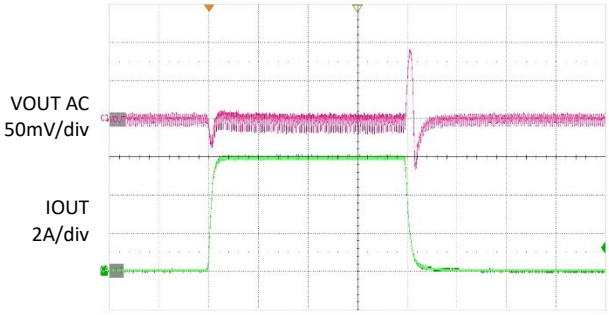
Switching waveform 6A load



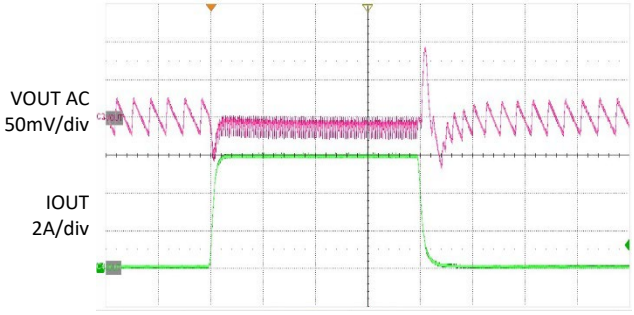
Typical Characteristics

VIN = 12V, VOUT = 5.0V, f_{SW} = 500kHz, EN = High, MODE = AGND, COUT = 22µF + 22µF and T_A = 25°C, unless otherwise specified.

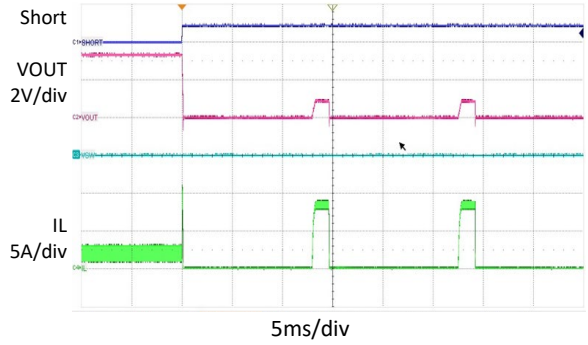
Load Step Response from 0.1A to 6A, 1A/µs SR
FPWM Mode, VOUT = 1.0V



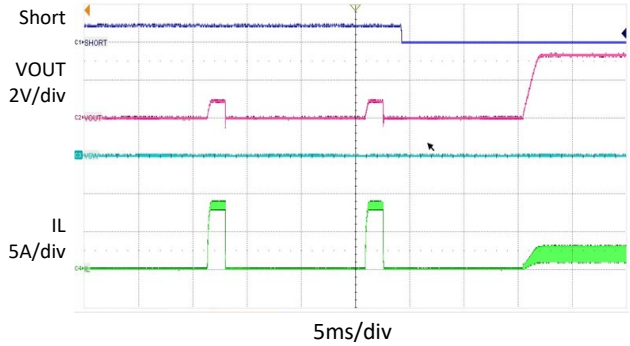
Load Step Response from 0.1A to 6A, 1A/µs SR
Auto-Skip Mode, VOUT = 1.0V



Output Short Current Limiting with Hiccup
2A Load to Output Short, VOUT = 3.3V



Output Short Recovery
Output Short to 2A Load, VOUT = 3.3V



Functional Block Diagram

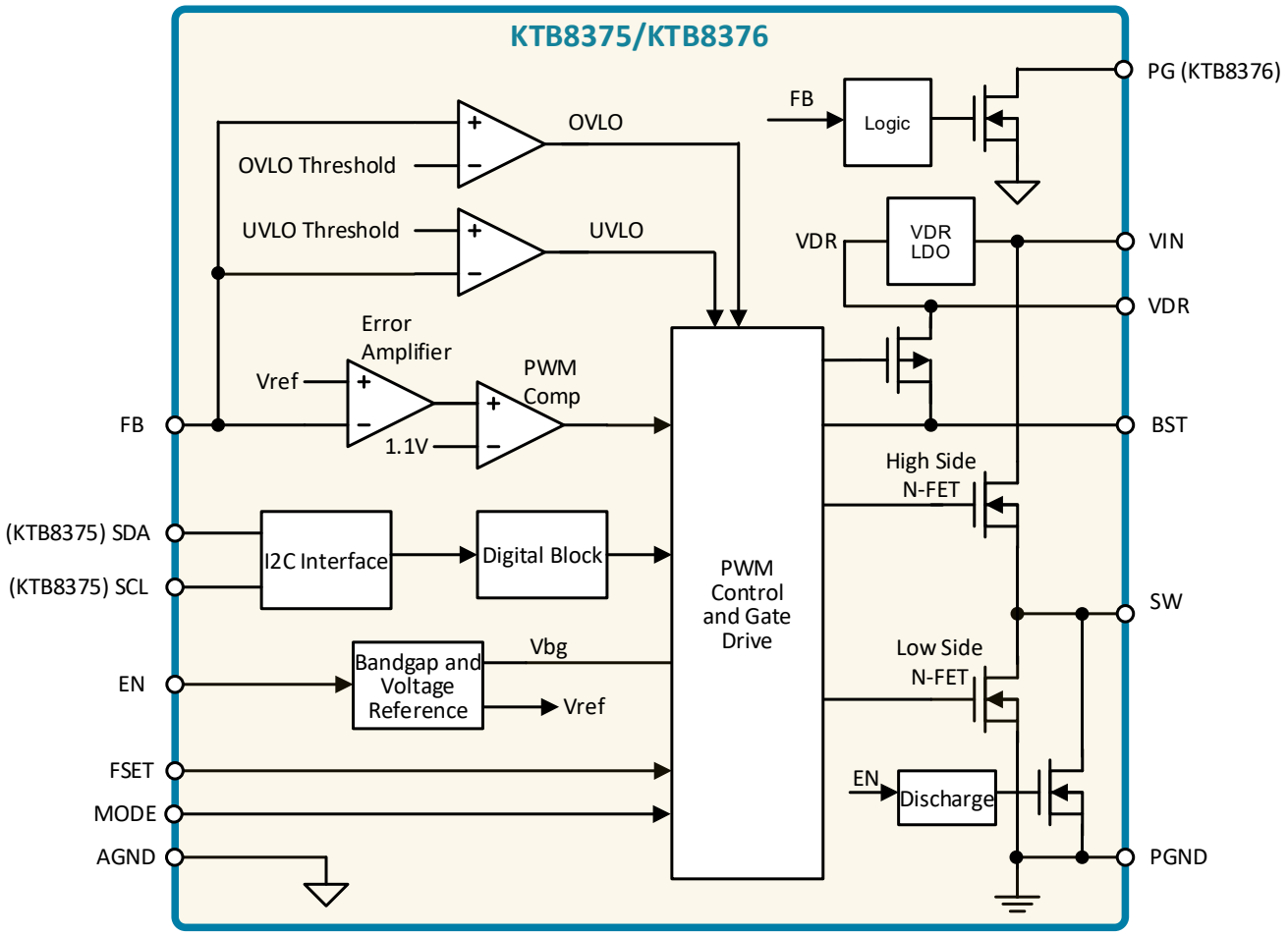


Figure 1. Functional Block Diagram

Functional Description

KTB8375/KTB8376 is a highly efficient, high-performance, monolithic buck regulator that operates from an input voltage of 4.5V to 24V and can output load up to 6A. It integrates the main switch, synchronous rectifier switch, PWM control circuitry, adjustable switching frequency, and various protection features.

Control Scheme

KTB8375/KTB8376 uses a proprietary adaptive on-time (AOT) PWM control scheme. Compared to typical current-mode PWM schemes, the AOT control scheme provides quick response to line and load transients with excellent stability and wide bandwidth, thereby minimizing output voltage droop and soar for dynamic loads, even with minimal output capacitance. The adaptive on-time approximates fixed-frequency switching without using a fixed clock oscillator, which eliminates the need to wait for the next clock before responding to a load transient.

KTB8375/KTB8376 feedback loop also adds a proprietary, internally compensated, integrating error amplifier to remove the output voltage offset normally associated with other AOT, constant on-time (COT), and hysteretic architectures.

Shutdown Mode

When the EN pin is low, KTB8375/KTB8376 is in shutdown mode and draws extremely low supply current.

Enable

KTB8375/KTB8376 buck regulator is turned on and off using the Enable high-voltage pin. Pull EN pin high to enable the buck regulator and pull the EN pin low to disable the buck regulator.

KTB8375 Buck Enable selection:

EN Pin	Control Register BUCK_ENB Bit (for KTB8375 only)	Operating Mode
L	X	Buck is Off (Shutdown mode)
H	0	Buck is On
H	1	Buck is Off

VDR

The VDR pin is the output of the internal 4V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VDR pin must be bypassed with a minimum 1µF, 10V X5R rated capacitor. VDR pin is for internal use only, no external load is allowed on the VDR pin. VDR output voltage is regulated when EN pin is High. VDR voltage is zero when the device is disabled (EN = Low).

KTB8375 has a register setting to set VDR voltage to 5V by I^2C.

Soft-Start

KTB8375 contains soft-start circuitry to ramp up V_{OUT} slowly in order to reduce inrush current at V_{IN} and prevent the inductor current from reaching the peak current limit during startup. After EN pin is toggled from Low to High, the buck soft start is initiated after a fixed Soft Start delay (t_{SS_DELAY}) of 1ms. During soft start, the ramp up rate of the Feedback voltage V_{FB}, hence V_{OUT}, is controlled to increase linearly until it reaches regulation during an internally fixed soft start time (t_{SS}) of 1.5ms.

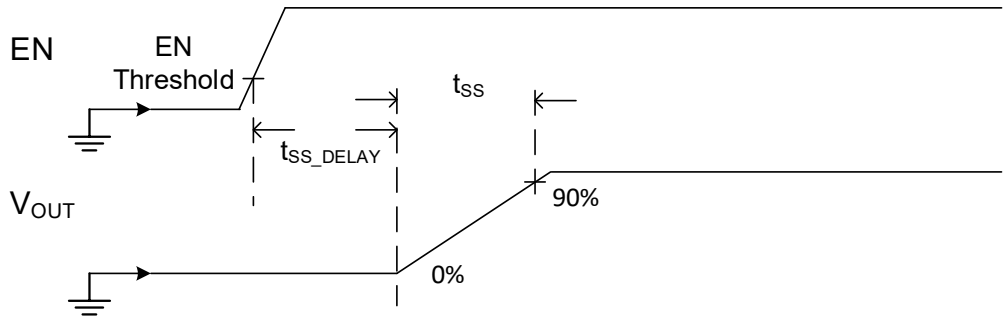


Figure 2. Power-up Timing Diagram

Auto-Skip Mode and Forced-PWM

KTB8375/KTB8376 can operate either in Automatic Skip (Auto-skip) mode or Forced-PWM (FPWM) mode depending on the MODE input pin set to logic High or Low. When the MODE pin is tied High or to VDR regulated voltage pin (4V typical), the buck operates in FPWM mode.

For KTB8376, the Auto-Skip mode is selected by connecting the MODE pin to GND.

For KTB8375, the mode can also be selected by the Control register MODE bit as shown in the table below.

KTB8375 Mode selection:

MODE Pin	Control Register MODE Bit (for KTB8375 only)	Operating Mode
L	0	Auto-Skip
L	1	FPWM
H	0	FPWM
H	1	FPWM

In Auto-Skip mode, KTB8375/KTB8376 transits automatically between constant frequency PWM mode at heavy loads and PFM mode at light loads. Auto-Skip mode is helpful for applications that need high efficiency at light loads. While skipping, single pulses are evenly spaced, resulting in the lowest output ripple and noise when compared to competing “pulse-grouping” or “burst mode” devices.

In noise-sensitive applications, even under light load conditions, fixed switching frequency is also desired and the KTB8375/KTB8376 needs to operate in forced-PWM (FPWM) mode.

Active Discharge Option

KTB8375/KTB8376 has an option[12] with an Active Discharge feature where a 180Ω on-chip pull-down is connected internally between the SW and PGND pins. This internal resistor discharges the output capacitor through the inductor once the device is disabled (EN pin Low).

Input Under-Voltage Lockout (UVLO)

When the input voltage (V_{IN}) is below the under-voltage lockout threshold (V_{UVLO}), the buck is disabled. When V_{IN} rises above V_{UVLO}, and if the buck is enabled, the default soft-start ramp begins.

Current Limit Protection (CLP)

KTB8375/KTB8376 features high-side switch peak-current limit and low-side switch valley-current limit, which protect the integrated FETs and inductor during over-current faults. The current limits control the buck switching on a cycle-by-cycle basis and have a higher priority than the regulation threshold and adaptive on-time.

Every cycle when high-side turns on, after the minimum On-time of 50ns, the device monitors Peak current limit. If the limit is reached, the high-side turns off immediately and the low side turns on. The low side remains on until the inductor current goes below the Valley current limit.

Every cycle, the device ensures that the inductor current is lower than the Valley current limit before the high-side is turned on. During sustained over-current faults, the output voltage typically droops below the regulation threshold.

Output Short-Circuit Protection

During normal operation after Soft-start, if an over-current event happens then the device has a cycle-by-cycle Valley current limit protection and once the output voltage droops by 40% of regulation then KTB8375/KTB8376 will enter hiccup mode and pause all switching.

12. Please see Ordering Information for Auto Discharge option part numbers.

The buck regulator attempts to soft-start after Hiccup Off Time t_{Hoff} of 12ms. If the output short persists, the buck regulator once again enters Hiccup mode and the cycle repeats until the short is removed. The low duty-factor during Hiccup mode prevents the IC from over-heating.

Thermal Shutdown

KTB8375/KTB8376 is turned off by an internal thermal shutdown when the junction temperature exceeds the thermal shutdown threshold (160°C typical). The device restarts when the junction temperature drops by 15°C.

Output Voltage Power Good (for KTB8376 only)

KTB8376 includes an output voltage Power-Good (PG) open-drain output monitoring the VOUT voltage. When VOUT voltage is below the Under-Voltage threshold or above the Over-Voltage threshold, PG output is pulled low.

When VOUT voltage is within the under-voltage and over-voltage thresholds, PG output is set High by the pull-up resistor connected to VDR supply pin.

Applications Information

The typical application schematic in the figure below is configured for 3.3V output, 500kHz switching frequency, Auto-Skip mode, and load up to 6A.

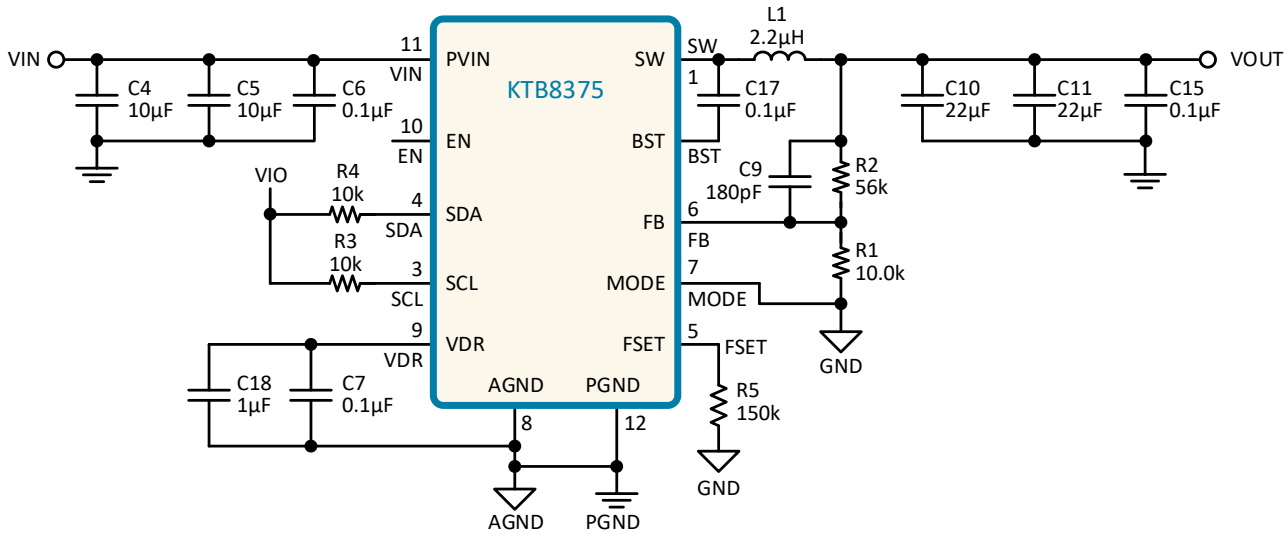


Figure 3. Typical Application Schematic

Output Voltage Setting

The output voltage is set by an external resistor divider (R1, R2) connected between VOUT, FB pin and GND and follows the formula below.

$$VOUT = 0.5V \times (1 + R2/R1)$$

In order to choose resistor R2 after selecting R1:

$$R2 = R1 \times (VOUT/0.5V - 1)$$

For various output voltage settings, with 10kΩ bottom resistor (R1), the top resistor (R2) values are listed in the table below. For VOUT output voltage best accuracy, 1% tolerance resistors should be used.

VOUT Setting (V)	R2 (kΩ)	R1 (kΩ)
5.0	90	10
3.3	56	10
2.5	40	10
1.8	26	10
1.2	14	10
1.0	10	10

Switching Frequency Setting

The buck switching frequency is set by an external resistor connected between the FSET pin and AGND pin. The switching frequency setting is between 500kHz and 2MHz.

Depending on the targeted switching frequency, the FSET resistor R_{FSET} value is selected as follows. For switching frequency best accuracy, 1% tolerance resistor is recommended.

$$R_{FSET}\ (k\Omega) = 75000 / f_{SW}\ (kHz)$$

Switching Frequency f_{SW} (kHz)	FSET Resistor R_{FSET} (kΩ)
500	150
600	125
750	100
1000	75
1200	62.5
1500	50
2000	37.5

Recommended Inductor

The selection of the inductor affects the steady-state operation as well as transient behavior and loop stability. The three most important inductor specifications to consider are inductor value, DC resistance (DCR), and saturation current rating. Higher inductance gives lower inductor current ripple, while lower inductance usually gives faster load transient response. KTB8375/KTB8376 is trimmed for inductors with nominal inductance of 0.8µH to 6.5µH. Select an inductor with a saturation current rating that is higher than KTB8375/KTB8376 peak current limit. Also, choose an inductor with sufficient temperature-rise current rating to satisfy the RMS load-current of the application. Consider the inductor resistance, since these will affect the efficiency. Larger physical case-sizes, good winding designs, and better magnetic materials can increase efficiency.

Recommended Capacitors

Ceramic input and output capacitors with X5R or X7R are recommended due to their low ESR, low ESL, low temperature coefficients, and small physical sizes. Consider the voltage rating, size, and DC bias derating characteristic of the capacitor.

Input Capacitor

Total input capacitors of 20µF or more are recommended on the PVIN pin to GND. Choose an input capacitor with voltage rating greater than the maximum input voltage, for example of 35V or more. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor. If the application input voltage is supplied through a connector or a cable, add additional bypass capacitance where V_{IN} first arrives to the PCB.

Output Capacitors

Choose output capacitors with voltage rating of 10V or more, 22µF total nominal capacitance or more. Consider the V_{OUT} setting of the regulator and how case size has a significant impact on DC bias derating. At high V_{OUT} settings, more total nominal capacitance is needed to achieve the same effective capacitance compared to lower V_{OUT} settings.

Recommended External Component Values

VOUT (V)	R top = R2 (kΩ)	R bottom = R1 (kΩ)	f_{SW}(kHz)*	R FSET = R5 (kΩ)	L1 (µH)	COUT Typical (µF)	Cff = C9 (pF)
5	90	10	500	150	3.3	44	180
3.3	56	10	500	150	2.2	44	180
1.0	10	10	500	150	1.0	44	180
5.0	90	10	1000	75	1.5	44	100
5.0	90	10	2000	37.5	0.82	44	82

Note: * switching frequency set by FSET resistor. For example, for f_{SW} at 500kHz, FSET resistor = R5 = 150kΩ.

Inductor part numbers

Inductor part number	Inductance (µH)	Manufacturer	Current Rating (A)	Ron Typical (mΩ)	Dimensions (mm)
IHLP3232DZER3R3M11	3.3	Vishay	10.5	14.0	8.18 x 8.64 x 4
IHLP3232DZER2R2M11	2.2	Vishay	14.5	8.8	
IHLP3232DZER1R0M11	1.0	Vishay	18.2	4.33	

I²C Interface Description

I²C Serial Data Bus

The KTB8375 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The KTB8375 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The KTB8375 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol are defined in Figure 4:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy
Both data and clock lines remain HIGH.

Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

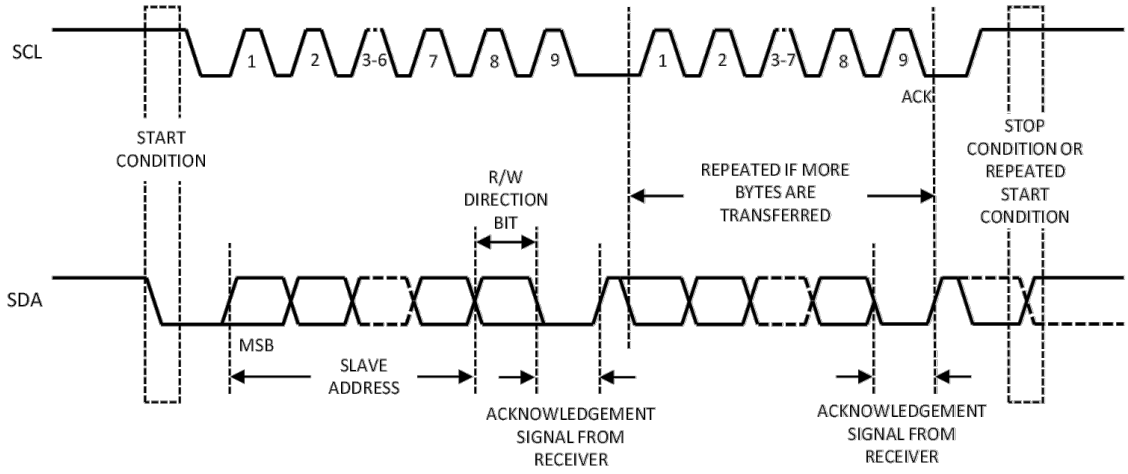


Figure 4. Data Transfer on I²C Serial Bus

The device 7-bit slave device address is 1110111 binary (0x77).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure shows the sequence of the I²C write cycle.

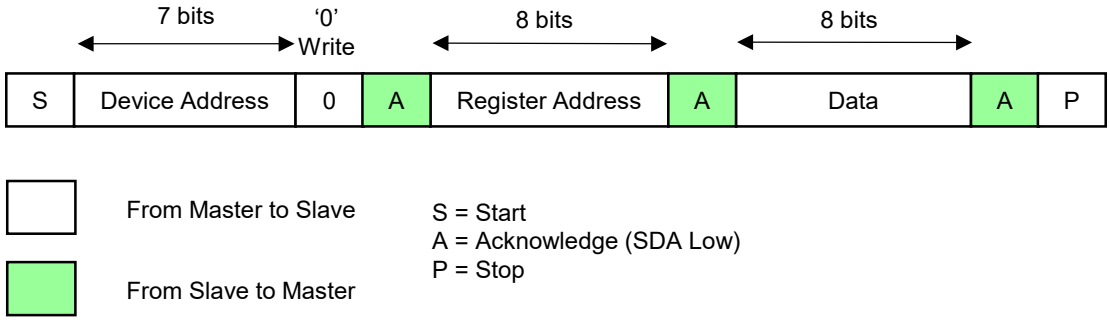


Figure 5. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generates stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure shows the steps of the I²C read cycle.

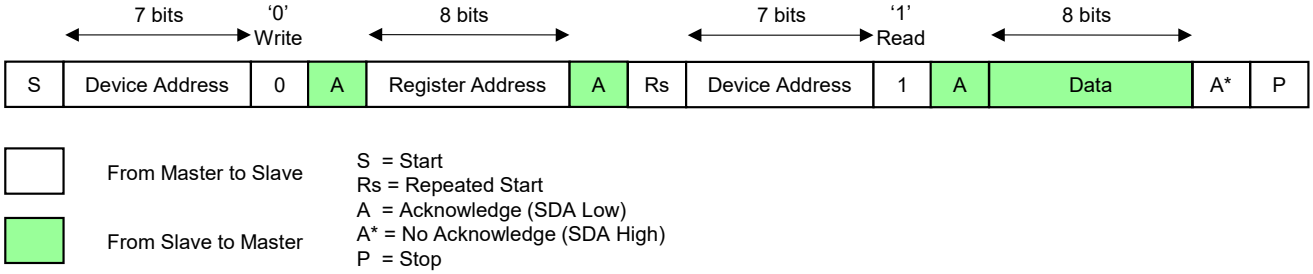


Figure 6. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (1110111 binary) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (1110111 binary) and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generates stop condition to finish the read cycle.

I²C Register Map

Register Address	Register Name	Access Read / Write	Default Binary Value
0x00	VREF	R/W	00100000
0x01	CONTROL	R/W	00110000
0x0A	STATUS	R	00000001

The registers are reset in hardware to their default values by V_{IN} power-on reset or by toggling EN input pin. Additionally, the registers can be reset via I²C by writing 1 to the CONTROL register (0x01) RESET bit[7].

VREF Register

Register Address 0x00

Bit	Name	Access	Default Reset	Description
0	VREF	R/W	0	VFB regulation voltage selection 0 = 500mV reference and 1 = 1V reference.
1:7	-	-	0010000	Reserved.

CONTROL Register

Register Address 0x01

Bit	Name	Access	Default Reset	Description
0	BUCK_ENB	R/W	0	Buck software enable/disable bit, 0 = Buck enabled, 1 = Buck disabled
1	-	-	0	Reserved.
2	MODE	R/W	0	MODE bit to select FPWM mode, 1 = FPWM 0 = Auto-Skip mode
3	-	-	0	Reserved.
4	OV_LOOSE	R/W	1	To select VOUT Over-Voltage threshold level at 110% or 120% of VOUT setting. • for OV_LOOSE = 1, if VOUT >= 120% Vout_set, then Reg0x0A bit[5] OV_STAT = 1 and bit[0] VO_GOOD = 0 • for OV_LOOSE = 0, if VOUT >= 110% Vout_set, then Reg0x0A bit[5] OV_STAT = 1 and bit[0] VO_GOOD = 0
5	UV_LOOSE	R/W	1	To select VOUT Under-Voltage threshold level at 90% or 80% of VOUT setting. • for UV_LOOSE = 1, if VOUT <= 80% Vout_set, then Reg0x0A bit[4] UV_STAT = 1 and bit[0] VO_GOOD = 0 • for UV_LOOSE = 0, if VOUT <= 90% Vout_set, then Reg0x0A bit[4] UV_STAT = 1 and bit[0] VO_GOOD = 0
6	VDR	R/W	0	VDR regulation voltage selection, 1 = VDR set to 5V, 0 = VDR set to 4V
7	RESET	R/W	0	When RESET bit set to 1, all registers are reset to their default values

STATUS Register

Register Address 0x0A

Bit	Name	Access	Default Reset	Description
0	VO_GOOD	R	1	VOUT/VFB regulation voltage status bit, 1 when VFB is in regulation (not Under-Voltage and not in Over-Voltage condition)
1	PVIN_BAD	R	0	PVIN Voltage Valid status, 1 indicates PVIN voltage is not valid and is above 30V.
2	-	-	0	Reserved.
3	OC_STAT	R	0	Over-Current indicator status, 1 when current exceeds the over-current threshold.
4	UV_STAT	R	0	VREF Under-Voltage status indicator, 1 when VREF voltage is too low below the under-voltage threshold. Please refer to the CONTROL register UV_LOOSE bit description.
5	OV_STAT	R	0	VREF Over-Voltage status indicator, 1 when VREF voltage is too high above the over-voltage threshold. Please refer to the CONTROL register OV_LOOSE bit description.
6	OVER_TEMP	R	0	Die over-temperature status, 1 when T_J > 160°C
7	FAULT	R	0	Fault flag status, 1 when Over-temperature, PVIN (30V detection) and Over-Voltage fault is present. For example, when OV_STAT status bit is 1, FAULT status equals 1.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents and keep efficiency high. To dissipate heat from the buck IC and the inductor, large copper areas allow to spread the heat away from these components.

The KTB8375/KTB8376 evaluation board is designed with a similar layout as the Recommended PCB Layout figure.

Minimize high current switching trace length between the device, the inductor and the input and output bypass capacitors.

Place PVIN bypass capacitors and VDR capacitors as close as possible to the device. Place the output capacitors close to the inductor.

Route a separate trace from the inductor VOUT side to the Feedback resistor divider top resistor directly.

Place the FSET resistor close to the FSET pin.

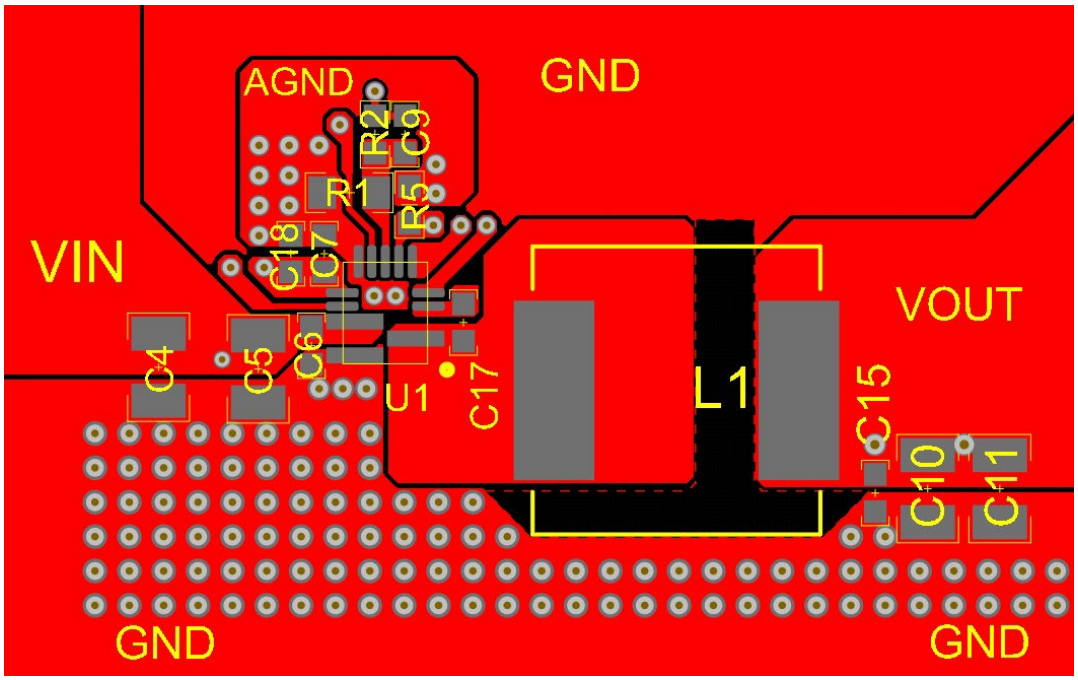
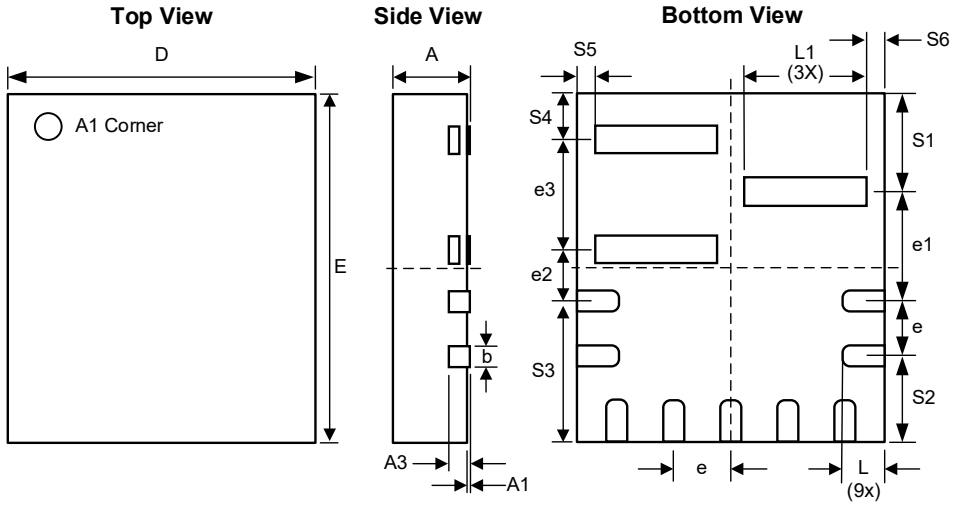


Figure 7. Recommended PCB Layout

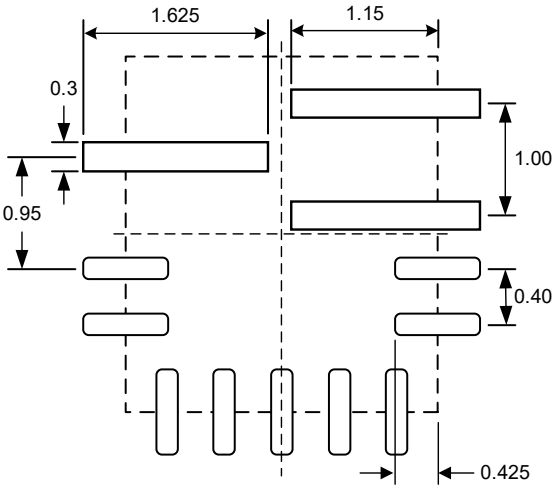
Packaging Information

FCQFN2.5x3-12 (2.50mm x 3.00mm x 0.55mm)



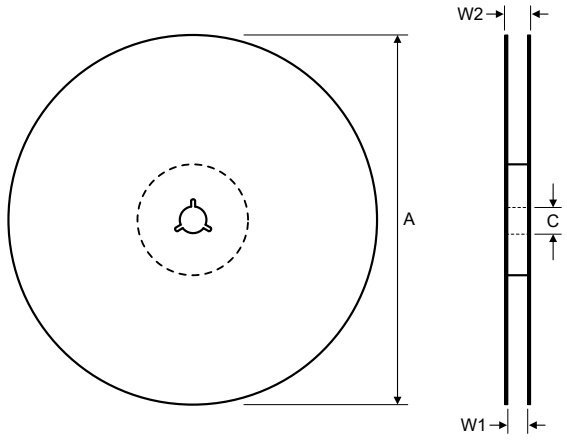
Dimension	mm		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.15	0.20	0.25
D	2.40	2.50	2.60
E	2.90	3.00	3.10
e	0.40 BSC		
e1	0.95 BSC		
e2	0.45 BSC		
e3	1.00 BSC		
L	0.35	0.40	0.45
L1	0.90	0.95	1.00
S1	0.85 REF.		
S2	0.80 REF.		
S3	1.20 REF.		
S4	0.35 REF.		
S5	0.20 REF.		
S6	0.20 REF.		

Recommended Footprint



Packaging Material Information

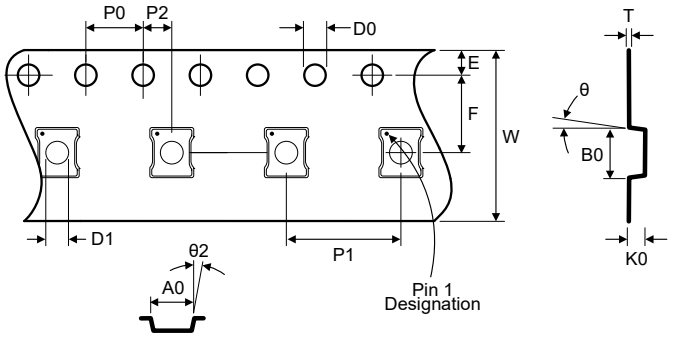
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	179	180	180
C	12.8	13.0	13.2
W1	13	13	14
W2	13	13	14.5

43-00003-038

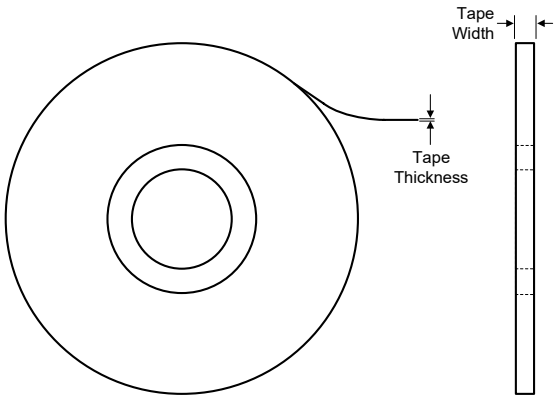
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	2.70	2.80	2.90
B0	3.20	3.30	3.40
K0	1.00	1.10	1.20
P0	3.90	4.00	4.10
P1	7.90	8.00	8.10
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	1.50	1.60	1.70
E	1.65	1.75	1.85
F	5.45	5.50	5.55
10P0	39.0	40.0	41.0
W	11.70	12.00	12.30
T	0.25	0.30	0.35
Θ	0°		5°
Θ2	0°		5°

43-010X0-21L

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.047	0.052	0.057
12mm	Tape Width	9.2	9.3	9.4

43-00002-057

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