KTD2037/2037B

I²C Programmable RGB LED Driver with AutoBlinQ™

Features

- Ultra low dropout regulated 3-channel current sinks
  - 40mV typ. at 10mA per channel
- Programmable LED setting by I²C compatible interface
- Individual channel control
  - On/Off Interval Time Control
  - Dimming Up/Down Time
  - RGB LED Color Control
- 191 current level setting
  - 24mA max, 0.125mA step
  - ±5% current matching at max current
- AutoBlinQ LED1 (D1 pin) mode
  - Blinking period: 2s
  - Current setting: 8mA
- No noise, non-pulsating LED current
- Fast, smooth start-up
- VIN Range: 2.7V to 5.5V
- 0.1µA Shutdown Current
- Pb-free Package: UTDFN-8 1.5x1.5mm
- -40°C to +85°C Temperature Range

Applications

- RGB indicator LEDs
- Mobile Phones and Handheld Devices
- Digital Cameras

Brief Description

The KTD2037/2037B is a fully programmable, constant current RGB LED driver with a flexible control interface. The device is ideally powered from one-cell lithium-ion/polymer, 3-cell NiCd/NiMH/Alkaline batteries, or systems with 3.3V or 5V supplies. It provides three independent programmable constant current sinks without requiring any external components.

With an on-chip timing control unit, LED blink rate, fade-in and fade-out are user-adjustable resulting in unique color lighting patterns.

Ten internal registers are programmed via the I²C control interface with a built-in decoder allowing individual control of the LED channels' On/Off state and current level. A total of 191 current levels are available for each channel from 0.125mA to 24mA with a 0.125mA step.

An AutoBlinQ mode automatically turns on and off LED1 (on D1 pin) at 8mA every 2s after EN pin goes high. In this mode, a phone with a discharged battery connected to a charger can have LED1 blink to notify that the battery is charging.

In shutdown mode, the quiescent current is reduced to less than 1µA.

The device is available in a low profile 8-pin 1.5mm x 1.5mm x 0.5mm Ultra-Thin DFN package. The package is Pb-free and RoHS compliant.

Typical Application

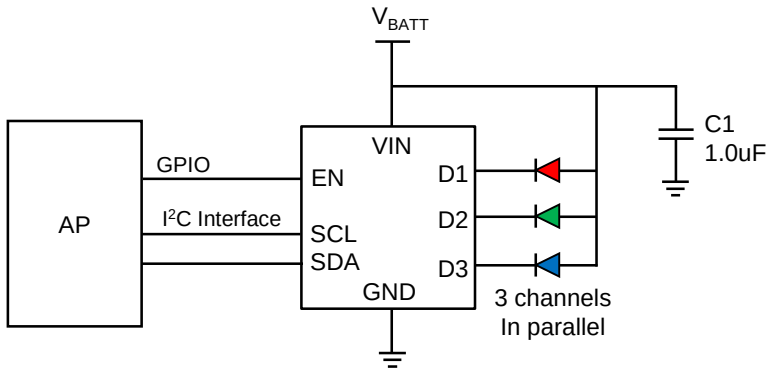


Figure 1. Typical Application Circuit

Typical Application (continued)

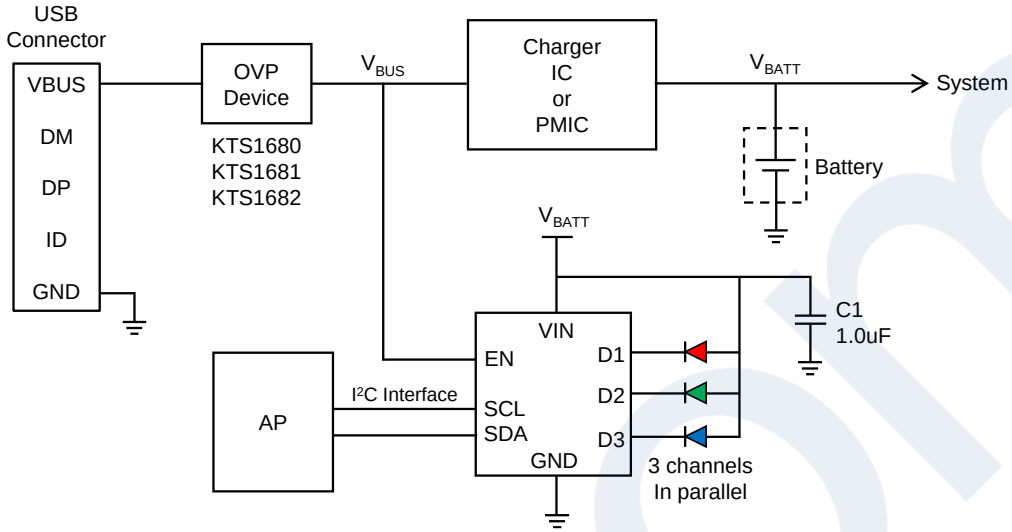


Figure 2. Application Circuit with External Charger and VBUS Detection

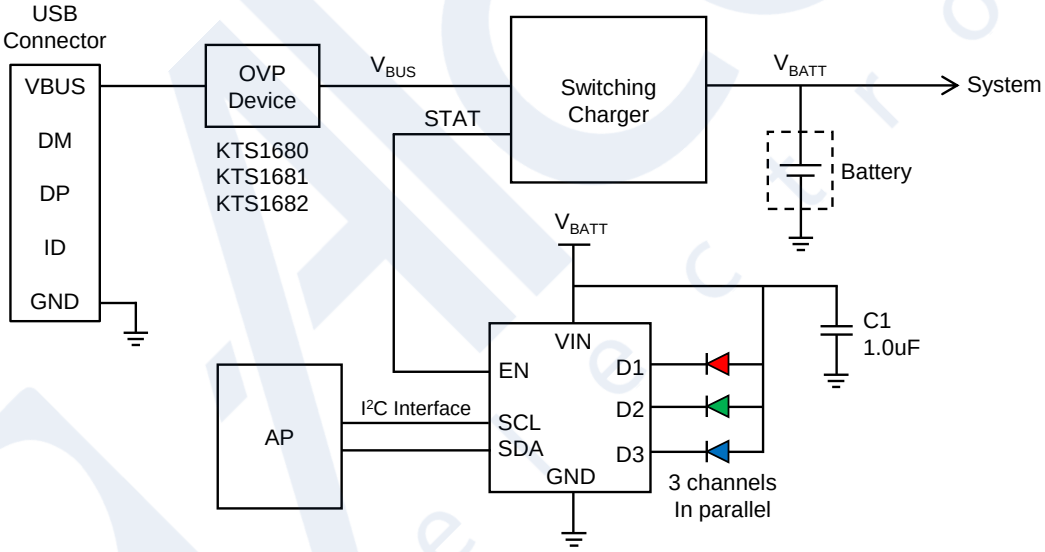
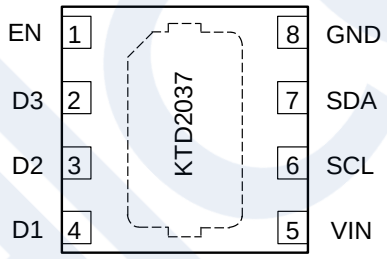


Figure 3. Application Circuit with Internal Charger IC Status Detection

Pin Descriptions

Pin #	Name	Function
1	EN	AutoBlinQ mode enable input pin. For KTD2037B only, the leakage current can be reduced further by disabling I²C interface when EN is low.
2	D3	Regulated output current sink D3. Current level and ON/OFF selections are controlled by serial interface.
3	D2	Regulated output current sink D2. Current level and ON/OFF selections are controlled by serial interface.
4	D1	Regulated output current sink D1. Current level and ON/OFF selections are controlled by serial interface.
5	VIN	Input power for the IC.
6	SCL	Clock of the I²C interface.
7	SDA	Data of the I²C interface.
8	GND	Ground pin.

UTDFN-8 1.5x1.5
(Top View)



Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VIN, D2, D3	Input voltage, Output pins	-0.3 to 6.0	V
EN	Enable Control pin	-0.3 to 6.0	V
SCL, SDA, D1	Control Interface pins and D1 sink pin	-0.3 to VIN+0.3	V
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C
V_{ESD}	HBM electrical static discharge	2.0	kV

Thermal Capabilities

Symbol	Description	Value	Units
UTDFN1.5x1.5-8			
θ_{JA}	Thermal Resistance – Junction to Ambient[2]	190	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	0.526	W
$\Delta P_D/°C$	Derating Factor Above T_A = 25°C	-5.26	mW/°C

Ordering Information

Part Number	IOUT max Per channel	I²C Input Active	Marking[3]	Operating Temperature	Package
KTD2037EWE-TR	24mA	EN = High or Low	IJYYZ	-40°C to +85°C	UTDFN-8 1.5x1.5
KTD2037BEWE-TR	24mA	EN = High	HWYYZ	-40°C to +85°C	UTDFN-8 1.5x1.5

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
3. "YYZ" is the date code and assembly code.

Electrical Characteristics[4]

Unless otherwise noted, the Min and Max specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). VIN = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	Input operating range		2.7		5.5	V
V_{D_MIN}	Sink pin (Dx) dropout voltage (90% of nominal current)	All Channels set to 20mA, VIN = 3.6V		75	120	mV
I_{SINK}	Output current accuracy	All Channels set to 20mA, VIN = 3.6V	-5.0		+5.0	%
		All channels set 0.125mA, VIN = 3.6V	-5.0		+5.0	%
	Output current matching	$\|I_D$ - Iavg| max / Iavg All Channels set to 20mA, VIN = 3.6V	-5.0		5.0	%
I_{IN}	IC supply Current	All Channels set to 20mA, VIN = 3.6V		300		µA
		1 Channel set to 20mA Other channels OFF		260		
I_Q	IC quiescent Current	Device on, All LEDs OFF, Reg4 = 0		190		µA
I_{SHDN}	Shutdown current	V_{IN} = 5.5V EN = GND (shutdown)		0.1	1.0	µA
Control and I²C-Compatible Pin Voltage Specifications (EN, SCL, SDA)[5]						
V_{IL}	Input Logic Low Threshold	SDA, SCL, EN			0.4	V
V_{IH}	Input Logic High Threshold	SDA, SCL, EN	1.2			V
I²C-Compatible Timing Specifications (SCL, SDA), see Figure 1						
t_1	SCL (Clock Period)		2.5			µs
t_2	Data In Setup Time to SCL High		100			ns
t_3	Data Out Stable After SCL Low		0			ns
t_4	SDA Low Setup Time to SCL Low (Start)		100			ns
Thermal Shutdown						
T_{J-TH}	IC junction thermal shutdown threshold			140		°C
	IC junction thermal shutdown hysteresis			15		°C

4. KTD2037/2037B is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

5. SCL and SDA must be glitch-free in order for proper brightness control to be realized.

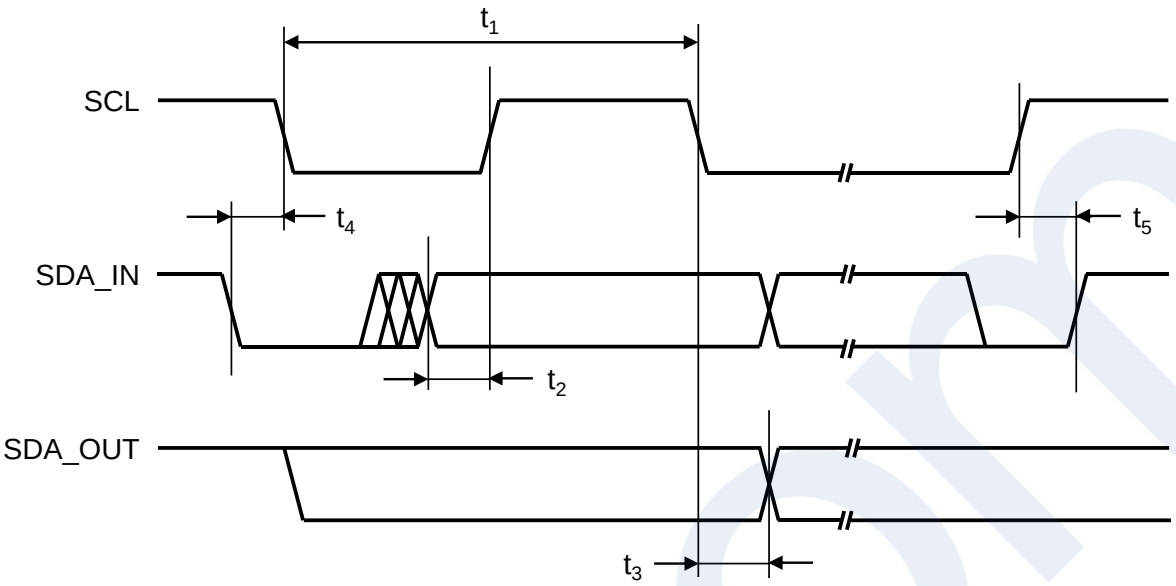
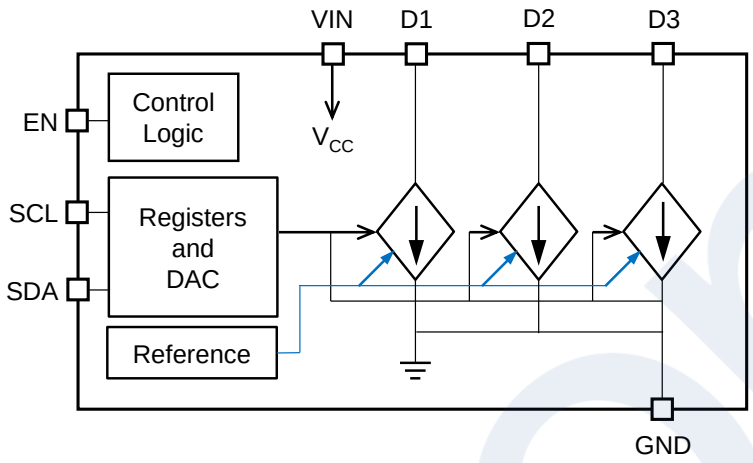


Figure 4. I²C Compatible Interface Timing

Functional Block Diagram



Functional Description

The KTD2037/2037B is a 3-channel output current sink device, offering constant current regulation with high efficiency and ultralow internal voltage drop. High integration and small size makes it ideal for driving RGB LEDs from a one-cell lithium-ion/polymer battery. With a supply voltage range of 2.7V to 5.5V, KTD2037/2037B is equally suitable for 3- or 4-cell NiCd/NiMH/Alkaline devices or systems with 3.3V or 5V supplies.

The KTD2037/2037B can be programmed via an I^2C compatible interface. It is programmable control to 192-step current levels for all the current sinks, and individual control the On/Off states of the output channels.

KTD2037 SDA and SCL input pins are active when EN pin is high or low whereas the KTD2037B EN input pin must be high for the I^2C interface to be enabled. When KTD2037B EN pin is low, the I^2C interface is disabled (not possible to write to registers) and the AutoBlinQ mode is disabled.

LED Current Programming

The individual channel brightness is controlled by the LEDx Iout registers Reg 6 to Reg 8. Each channel has a dedicated 8-bit register for setting the current value. The LED channel current is constant, non-pulsing, except when it is being ramped-up and down.

The ramp up and down are automatically generated using a PWM scheme where the duty cycle is continuously changing (either increasing or decreasing) to provide a smooth LED current transition between the ON and OFF states. The ramp times, for rise and fall, are separately programmable through an internal Ramp register Reg 5 with 4 bits for rise and 4 bits for fall. The ramping can be configured to linear or quasi-logarithmic/s-curve by setting register Reg 1 bit 7 to 1 or 0 respectively.

Flashing LEDs can be performed by programming the time period (Tflash) between two consecutive flashes in the Flash Period register Reg 1. Two Flash On Timer 1/2 registers, Reg 2 and Reg 3, allow to set the LED on time as a percentage of the Flash period. The on time (Ton), shown in Figure 2, includes the ramp-up Trise and the full on time. Two timer registers are available to support two or more LEDs to flash independently.

Each channel can be configured to timer1 or timer2 with the Channel Control register Reg 4.

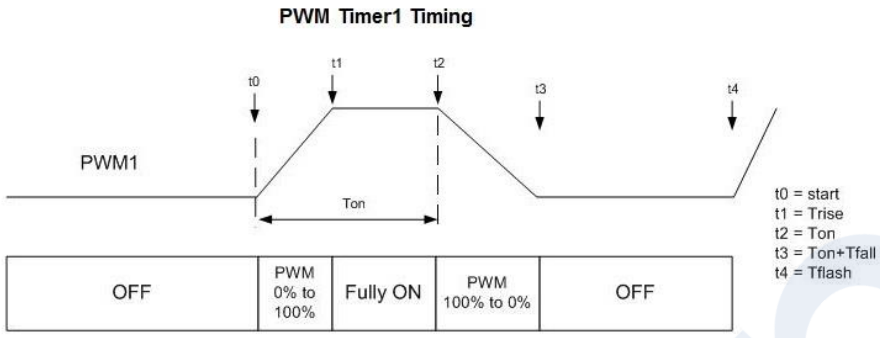


Figure 5. Channel Timing Diagram

Timer Slot Control

The timing diagrams for the four time slots are illustrated below.

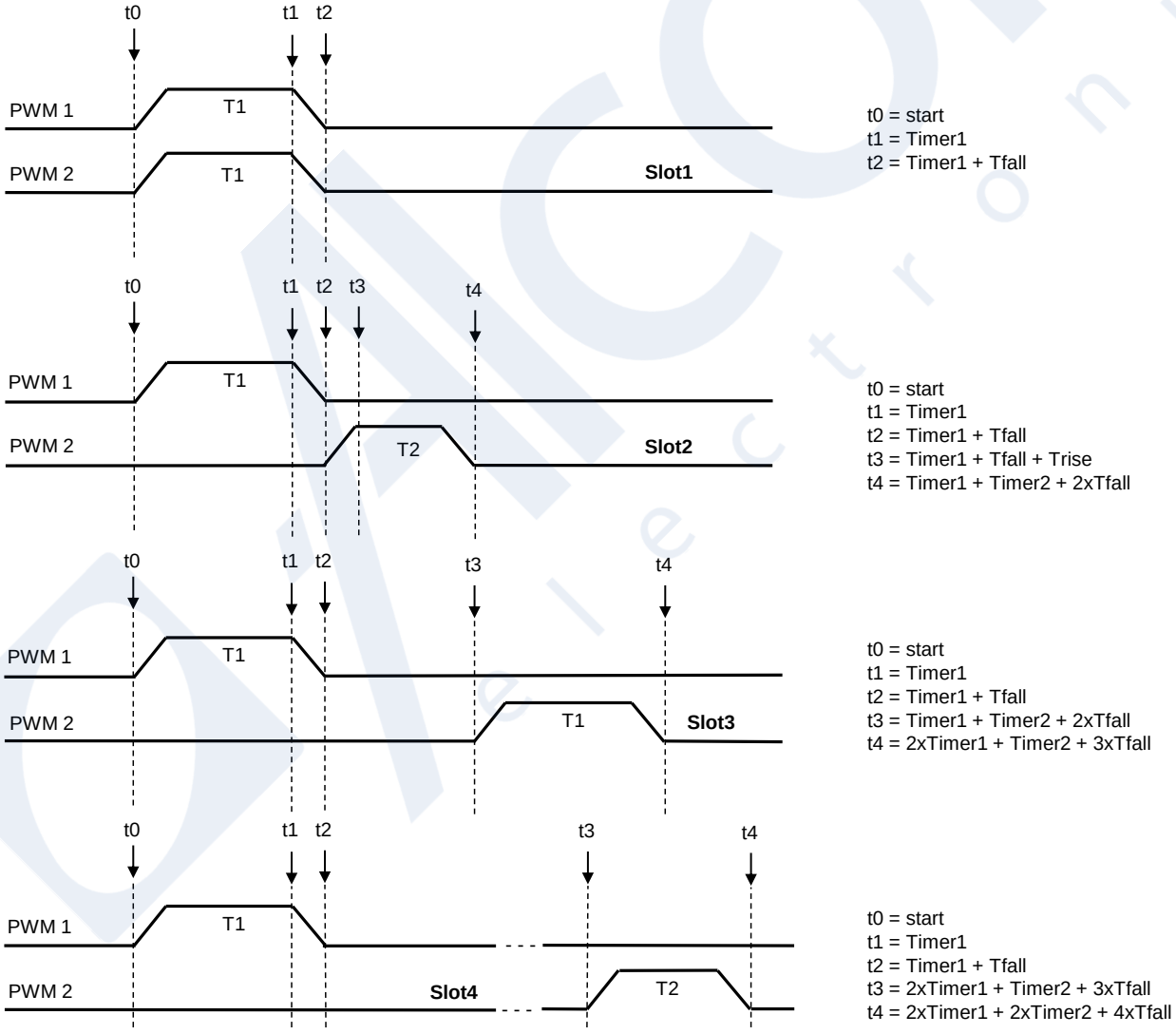


Figure 6. Timer Slot Timing Diagram

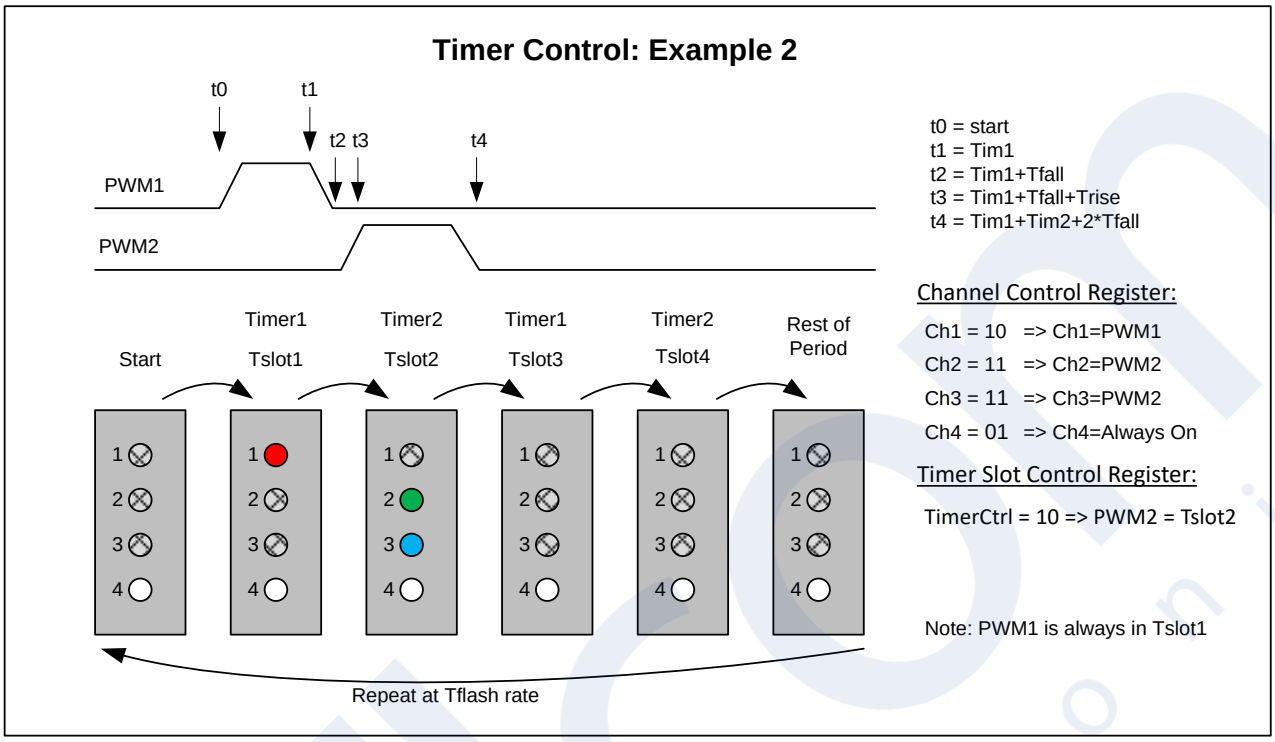


Figure 7. Timer Slot2 Example*

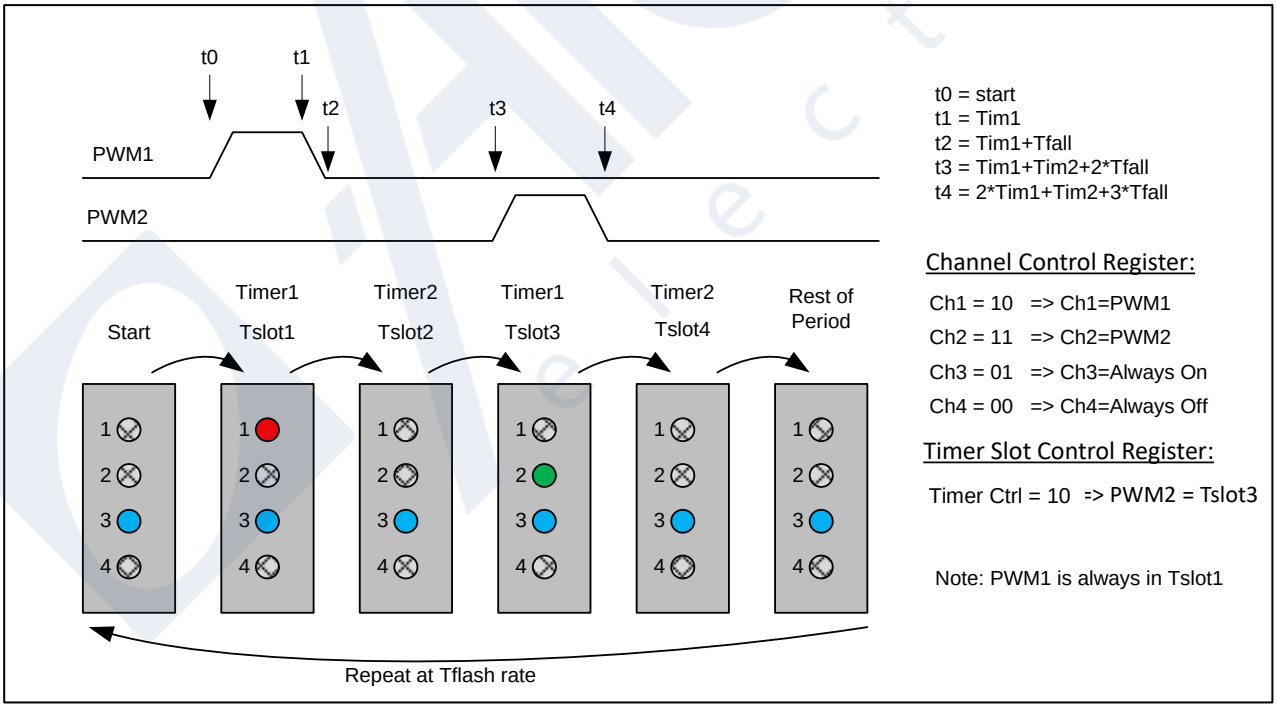


Figure 8. Timer Slot3 Example*

*Programming these patterns requires to write to several registers and therefore involves multiple I^2C commands.

Each channel can be assigned to one of the 2 time slots, or always OFF or always ON. The Timer Slot Control register bits define the timing of the second PWM waveform.

The Duty Cycle of each flash waveform is set by the timer and can be set with 8-bit resolution (256 steps) between 0 and 100%. The period of the flash repetition rate can also be set with a 7-bit resolution up to 8 seconds (256ms steps starting at 64ms). The Flash repetition period is the same for all outputs. If the programmed total time of the Timers exceed the Flash repetition rate then the PWM2 slot will be terminated and the Timers reset to start position. This may cause the PWM2 signal to be instantly reduced to zero.

Rise/Fall Times

The Ramp-Up and Ramp-Down can be linear or S-shaped profile. The S-shape is the default. The ramp-up transitions from 0% to 100% of the Iset value (ON state) and ramp-down to 0% (OFF state).

LED Basic Control

The brightness setting of each channel is internally controlled by 48 current units of 0.5mA. Output current resolution is increased to an effective 0.125mA steps by interpolation based time division multiplexing (similar to PWM) by a digital interpolator and works on the 2 LSB units of the current setting.

The Stay-Alive/Control Enable Bits are used to permit the Flash pattern to continue or be a one-shot.

Table 1. Register Map

	Reg #	Name	Reset Values (hexa)
Register Bank	0	Register/Control	x00
	1	Flash Period	X00
	2	Flash On Time1	X81
	3	Flash On Time2	x01
	4	Channel Control	x82
	5	Ramp Rate	x00
	6	LED1 I_{OUT}	X3F
	7	LED2 I_{OUT}	x9F
	8	LED3 I_{OUT}	x9F
	9	AutoBlinQ	xAF

Reset/Control: Reg 0	
0 (LSB)	Timer Slot Control / Reset Control
1	
2	Reset/Offset Cancel
3	EN Ctrl
4	
5	Rise/Fall Scaling
6	
7 (MSB)	Reserved (Test only)

Flash Period: Reg 1	
0 (LSB)	Flash Period
1	
2	
3	
4	
5	
6	
7 (MSB)	Ramp Linear

Flash On Time1: Reg 2	
0	PWM1 Timer Percentage of Period
1	
2	
3	
4	
5	
6	
7	

Flash On Time2: Reg 3	
0	PWM2 Timer Percentage of Period
1	
2	
3	
4	
5	
6	
7	

Channel Control: Reg 4	
0 (LSB)	LED1 Enable/Timer1/2
1	
2	LED2 Enable/Timer1/2
3	
4	LED3 Enable/Timer1/2
5	
6	Device Enable
7 (MSB)	Not Used

Ramp Rate: Reg 5	
0	Trise
1	
2	
3	
4	Tfall
5	
6	
7	

LED1 I_{OUT}: Reg 6	
0	I_{OUT} 0.125mA to 24mA in 0.125mA steps
1	
2	
3	
4	
5	
6	
7	

LED2 I_{OUT}: Reg 7	
0 (LSB)	I_{OUT} 0.125mA to 24mA in 0.125mA steps
1	
2	
3	
4	
5	
6	
7 (MSB)	

LED3 I_{OUT}: Reg 8	
0	I_{OUT} 0.125mA to 24mA in 0.125mA steps
1	
2	
3	
4	
5	
6	
7	

AutoBlinQ : Reg 9	
0	Enable AutoBlinQ Mode
1	1*
2	1*
3	Not used
4	
5	
6	
7	Auto Started (Read only)

Note *: The two bits Reg9 [2:1] must be always 1.

Register Description

Reg0 EN/RST

Reg0 [2:0] Timer Slot Control / Reset Control

TCtrl / Reset Modes			
Reg0[2:0]			Function
D2	D1	D0	
0	0	0	TCtrl: Tslot1
0	0	1	TCtrl: Tslot2
0	1	0	TCtrl: Tslot3
0	1	1	TCtrl: Tslot4
1	0	0	Do Nothing (bit cleared)
1	0	1	Reset Registers only
1	1	0	Reset Main Digital only
1	1	1	Reset Complete Chip

After power-up or VIN dropping below 2.7V, the device should be reset by writing Reg0 = 111 binary. All registers are then restored to their default reset values.

Reg0 [4:3] Enable Control

The device enable condition is defined by the two bits Reg0[4:3]. Four different conditions can trigger the device to turn ON depending on the SDA or SCL inputs.

Enable Control				
Reg0[4:3]		**Device ON Condition**		**Device Enters Shutdown Mode Condition**
D1	**D0**	**SCL**	**SDA**	
0	0	High	High	Either SDA or SCL goes low
0	1	High	SDA toggling[6]	Either SCL goes low or SDA stops toggling[6]
1	0	High	Don't care	SCL goes low
1	1	Always ON		Device always ON

Reg0 [6:5] Rise/Fall Time Scaling

These two bits allow to scale the rise and fall time defined in Reg5 ramp rate register.

For example, Reg0[6,5] = 01 (2x slower scaling) and Reg5 = 1, then the rise time = 96ms x 2 = 192ms.

Rise/Fall Time Scaling[7]		
Reg0[6:5]		
D1	D0	Scaling factor
0	0	1x Normal
0	1	2x Slower
1	0	4x Slower
1	1	8x Faster

6. Device enters shutdown/sleep mode with a delay t_{SHDN} (600µs typ.) after the last falling edge of SDA.

7. Bit Reg0[7] must be kept to 0 and is not used in normal operation (reserved for factory test).

Reg1 Flash Period and Reg2/Reg3 ON Timer 1/2

The three registers Reg1, Reg2 and Reg3 allow configuration of the blinking time for the two timers 1/2, associated with PWM1 and PWM2. Reg2 and Reg3 define the LED ON time as a percentage of the period defined in Reg1. The ON time (Ton) includes the ramp rise time as shown in Figure 2.

For example, for Reg1 = 4 and Reg2 = 5, ON timer 1 is equal to 2% of 0.64s = 12.8ms

Reg1[6-0] Flash Period		
Dec	**Binary**	**Period[s]**
0	0000000	0.128
1	0000001	0.384
2	0000010	0.512
3	0000011	0.640
4	0000100	0.768
5	0000101	0.896
6	0000110	1.024
7	0000111	1.152
8	0001000	1.28
9	0001001	1.408
10	0001010	1.536
11	0001011	1.664
12	0001100	1.792
13	0001101	1.92
111	1101111	14.46
112	1110000	14.59
113	1110001	14.72
114	1110010	14.85
115	1110011	14.98
116	1110100	15.10
117	1110101	15.23
118	1110110	15.36
119	1110111	15.49
120	1111000	15.62
121	1111001	15.74
122	1111010	15.87
123	1111011	16.0
124	1111100	16.13
125	1111101	16.26
126	1111110	16.38
127	1111111	One Shot

Reg2/Reg3 Flash ON Timer 1/2		
Dec	**Binary**	**Percentage of Period[%]**
0	00000000	0.0%
1	00000001	0.4%
2	00000010	0.8%
3	00000011	1.2%
4	00000100	1.6%
5	00000101	2.0%
6	00000110	2.3%
7	00000111	2.7%
8	00001000	3.1%
9	00001001	3.5%
10	00001010	3.9%
11	00001011	4.3%
12	00001100	4.7%
13	00001101	5.1%
239	11101111	93.4%
240	11110000	93.8%
241	11110001	94.1%
242	11110010	94.5%
243	11110011	94.9%
244	11110100	95.3%
245	11110101	95.7%
246	11110110	96.1%
247	11110111	96.5%
248	11111000	96.9%
249	11111001	97.3%
250	11111010	97.7%
251	11111011	98.0%
252	11111100	98.4%
253	11111101	98.8%
254	11111110	99.2%
255	11111111	99.6%

Reg1 [7] Ramp Linear

The default setting, bit Reg1[7] = 0, provides with a logarithmic-like S ramp up and down curve. By setting this bit to 1, the ramp becomes a simple linear up and down waveform.

Reg4 [5:0] LED Enable Control

Register Reg4 sets the mode of each LED channel to either always ON/OFF or PWM1/PWM2.

For example Reg4 = 00000001(binary), sets LED1 ON and other channels OFF.

LED Enable (1/2/3)		
Dec	Binary	Function
0	00	Always OFF
1	01	Always ON
2	10	PWM1
3	11	PWM2

Reg4 [6] Device Enable

To shutdown the device, EN pin must be low and the device enable bit Reg4[6] must be set to 0. By default, the bit is 0.

EN pin	Device Enable bit Reg4 [6]	Device Mode Description	
		KTD2037	KTD2037B
Low	0	Device off, I^2C enabled	Device off (zero current shutdown mode), I^2C disabled
Low	1	Device on according to register setting (not in AutoBlinQ mode)	Device on according to register setting but I^2C disabled (not in AutoBlinQ mode)
High	0	AutoBlinQ mode if Reg9[0] = 1	AutoBlinQ mode if Reg9[0] = 1
High	1	Device on according to register setting (AutoBlinQ is possible)	Device on according to register setting (AutoBlinQ is possible)

Reg5 Ramp Times

The register Reg5 sets the rise and fall time durations for the LED current ramp transitioning between 0mA and the nominal current. The rise and fall ramp times are defined by 4 bits Reg5[3-0] and Reg5[7-4] respectively.

For example, Reg5 = 4 and Reg 0[6,5] = 0 (1x ramp scaling), the rise time is equal to 512ms.

Trise Reg5[3-0] Tfall Reg5[7-4]		Ramp Time [ms]			
		Ramp Scaling[8]			
Dec	Binary	00 1x	01 2x slower	10 4x slower	11 8x faster
0	**0000 (Default)**	**2**	**2**	**2**	**2**
1	0001	128	256	512	16
2	0010	256	512	1024	32
3	0011	384	768	1536	48
4	0100	512	1024	2048	64
5	0101	640	1280	2560	80
6	0110	768	1536	3072	96
7	0111	896	1792	3584	112
8	1000	1024	2048	4096	128
9	1001	1152	2304	4608	144
10	1010	1280	2560	5120	160
11	1011	1408	2816	5632	176
12	1100	1536	3072	6144	192
13	1101	1664	3328	6656	208
14	1110	1792	3584	7168	224
15	1111	1920	3840	7680	240

8. There is only one Tramp Scaling register for both the rise and fall times.

Reg6, Reg7, Reg8 LED Current Setting

Registers Reg6 to Reg8 define the LED current setting for the channels D1 to D3 respectively. The LED current can be programmed with 192 steps between 0.125mA minimum and 24mA maximum.

For example, 24mA is set by the code BF hexadecimal (191 decimal, 1011 1111 binary) or any higher code value. 10mA current is set by the code 4F hexadecimal (79 decimal, 0100 1111 binary)

Iout (mA)	Data Dec	Data Hexa	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0[9]
0.125	0 (default)	00h (default)	0	0	0	0	0	0	0	0
0.25	1	01h	0	0	0	0	0	0	0	1
0.38	2	02h	0	0	0	0	0	0	1	0
0.50	3	03h	0	0	0	0	0	0	1	1
10.00	79	4Fh	0	1	0	0	1	1	1	1
10.13	80	50h	0	1	0	1	0	0	0	0
20.00	159	9Fh	1	0	0	1	1	1	1	1
20.13	160	A0h	1	0	1	0	0	0	0	0
23.88	190	BEh	1	0	1	1	1	1	1	0
24.00	191	BFh	1	0	1	1	1	1	1	1
24.00	192	C0h	1	1	0	0	0	0	0	0
24.00	254	FEh	1	1	1	1	1	1	1	0
24.00	255	FFh	1	1	1	1	1	1	1	1

9. The 2 LSB's are timed division multiplexed (similar to PWM) by a digital interpolator. Minimum I_{OUT} unit is 0.5mA.

AutoBlinQ Mode Operation

AutoBlinQ mode automatically turns on and off LED1 (on D1 pin) after EN pin goes high without the need to send an I²C command. When a phone with a discharged battery is connected to a charger, the phone is off (black screen) and LED1 is blinking to notify that the battery is charging.

Without this feature, during a deeply discharged battery charge stage, the battery indicator light may be off and it appears as though the battery is not charging.

Figure 5 illustrates LED1 (connected to D1 pin) pulsing on/off with 2s period (1s on, 1s off) and 8mA max current (I_{MAX}), all other channels are turned off. Other LED1 current options can be requested at the factory for 2mA, 4mA and 6mA.

Once EN input pin is set low, the AutoBlinQ mode stops.

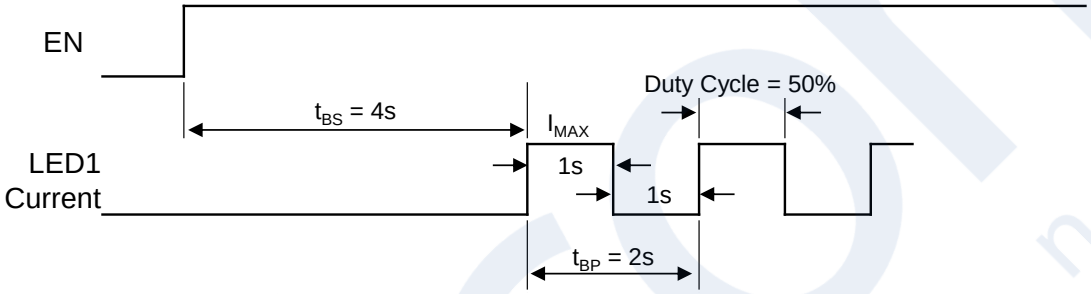


Figure 9. AutoBlinQ Mode Timing Diagram

Reg9 AutoBlinQ

AutoBlinQ mode is controlled by the Enable AutoBlinQ mode bit Reg9[0]. By default, AutoBlinQ mode is enabled with Reg9[0] = 1. By setting this bit to 0, the AutoBlinQ mode can be disabled.

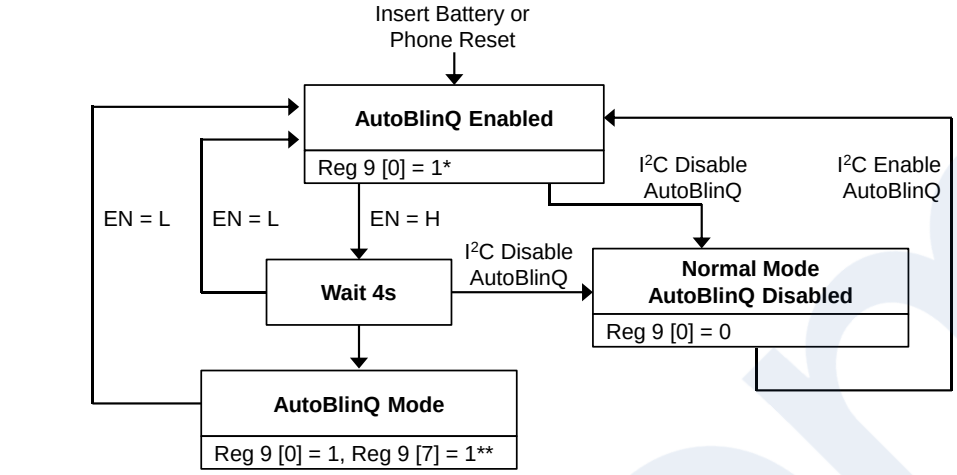
To disable AutoBlinQ mode, write Reg9 = 0x06 to set the Enable AutoBlinQ bit Reg9[0] to 0. Next time EN input goes high, the device will not enter AutoBlinQ mode.

Important note: The two bits Reg9 [2:1] must be always 1.

To enable AutoBlinQ mode, write Reg9 = 0x07 to set the Enable AutoBlinQ bit Reg9[0] to 1 (default setting). When EN input goes high, the device enters AutoBlinQ mode.

Once the AutoBlinQ mode starts, 4s after EN goes high, the Auto Started bit Reg9[7] is set to 1. Reg9[7] is a read only bit.

Important Note: It is recommended that KTD2037/2037B should be put into the reset state (default state after power-up) before the AutoBlinQ mode is activated. Data 111b should be written to Reg0 [2:0] before enabling AutoBlinQ mode. If the KTD2037/2037B registers were modified and the AutoBlinQ mode is activated without a register reset, the blinking operation may be incorrect.



notes: * Enable AutoBlinQ bit Reg 9 [0]
** AutoBlinQ Started bit Reg 9 [7]

Figure 10. AutoBlinQ Mode

Initial Condition	
Phone Operation	KTD2037/KTD2037B Interface
Battery discharged (Vbat < 3.2V) Phone turned off (LCD off) Reset KTD2037/KTD2037B KTD2037/KTD2037B AutoBlinQ Mode is enabled (default)	Set KTD2037/KTD2037B EN pin high Write Reg 0 = 0x07 Set KTD2037/KTD2037B EN pin low Reg 9 [0] = 1*
Plug in the charger ↓ after 4s LED1 starts blinking ↓ AutoBlinQ Mode on ↓ Battery recharged (Vbat > 3.6V) Phone turns on KTD2037/KTD2037B AutoBlinQ Mode is disabled ↓ LED1 stops blinking	Set KTD2037/KTD2037B EN pin high Reg 9 [0] = 1, Reg 9 [7] = 1** To disable AutoBlinQ Mode Write Reg 9 [0] = 0 or set EN pin low

* Enable AutoBlinQ bit Reg 9 [0]
** AutoBlinQ Started bit Reg 9 [7

Figure 11. Smartphone AutoBlinQ Mode Operation

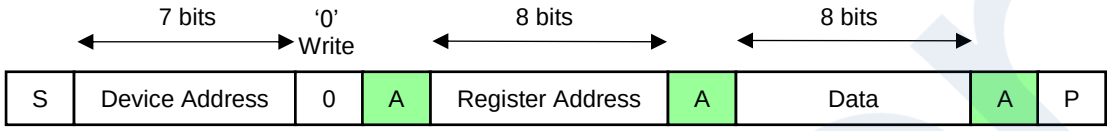
Application Information

I²C Interface Protocol

On the KTD2037/2037B, the ten internal registers Reg0 to Reg9 can be accessed via the I²C interface. The I²C device address is 0x30 hexadecimal or 110000 binary. The read and write commands allow to modify the content of each register. For further details on the I²C protocol, please refer to the I²C−Bus Specification, document number 9398 393 40011, from Philips Semiconductors.

The protocol for Write and Read is the following.

Write:



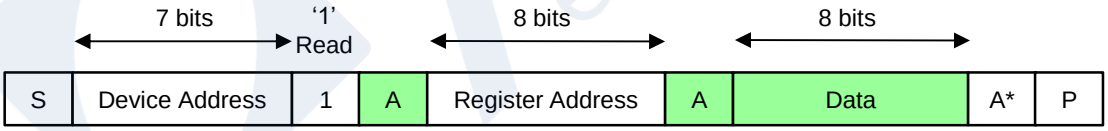
where S = START condition
P = STOP condition
Device Address = 0110000 (7 bits, MSB first)
Register Address = Reg0 - Reg9 address (8 bits)
Data = data to read or write (8 bits)
1 = Read command bit
0 = Write command bit
A = acknowledge (SDA low)
A* = not acknowledge (SDA high)

For example, the command to write KTD2037/2037B register Reg4 (address 4) = 0, LEDs always OFF:

S	0110000	0	A	00000100	A	00000000	A	P

Note: For the I²C Reset commands ("Reset Register only" and "Reset Complete Chip"), the last byte is followed by a "not acknowledge" (SDA high). For these two commands, the lack of acknowledge at the end of the command is to be ignored.

Read:



Power Saving, Sleep Mode

When the KTD2037/2037B is not driving LEDs, for example when all LEDs are off, the driver current consumption can be set to “zero current” by putting the device into shutdown or sleep mode.

The register content is preserved while the device goes into shutdown/sleep mode. To restart with LEDs off, LEDs should be turned off by writing zero into the LED Enable Control register Reg4 before entering the sleep mode.

This can be done by writing into the Enable Control mode register Reg0[4:3] = 01 and select the option “SCL=High & SDA Toggling”. The device remains in sleep mode while there is no activity on the SDA line.

The following sequence shows an example where LED3 is flashing initially, then the device is set to sleep mode, then the part is restarted.

LED3 (blue) is flashing. KTD2037/2037B VIN pin current (I_{IN}) = 260μA

To enter sleep mode: Write Enable Control mode register Reg0[4:3] = 01, for option “SCL=High & SDA Toggling”.

LEDs are off. I_{IN} = “zero” when there is no activity on the SDA line.

To restart the driver: Write Enable Control mode register Reg0[4:3] = 00, for option “SCL & SDA High”.

LED3 (blue) is flashing. I_{IN} = 260μA.

Voltage Headroom

The lowest headroom voltage is critical for systems with supply voltages nearing 3V, such as battery operated or regulated 3.3V systems. The advancement of LED technologies has made possible lower LED current and lower forward voltage drop (VF). For example, the majority of vendors’ Blue LED’s VF at 5mA is 3.15V or below. With the cut-off voltage for most 1-cell Li+ powered systems set to 3.3V~3.5V, it is possible to drive RGB LEDs without voltage step-up as long as the internal voltage drop for the driver circuit is specially designed for the lowest voltage possible.

Each current sink of the KTD2037/2037B is designed to allow the lowest operating input voltage without voltage step-up while maintaining current regulation, thus extending the battery run time. When input voltage is low, the internal low impedance current sink adds merely 75mV (typical) headroom on top of the LED forward voltage at 24mA per channel.

The formula is: $$V_{IN(MIN)} = V_{F(MAX)} + V_{SINK(MIN)},$$

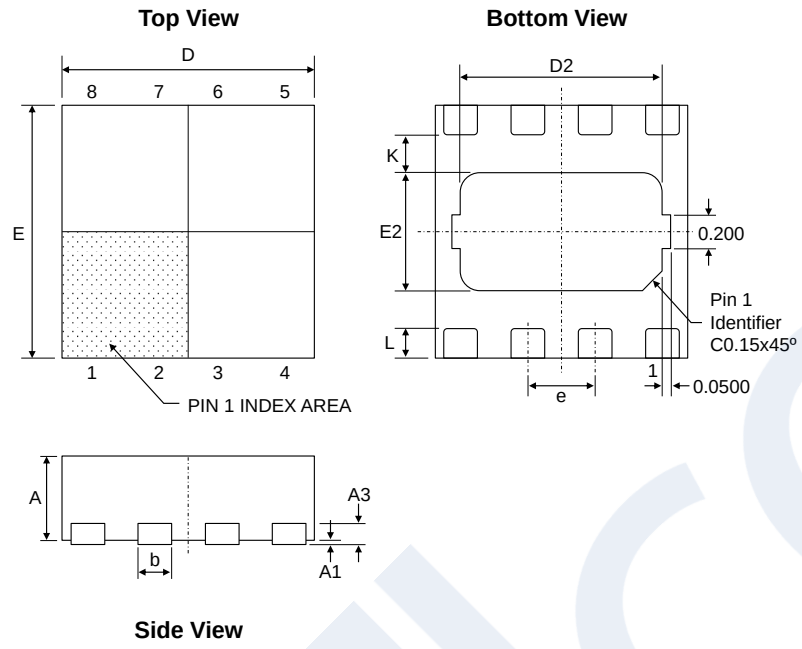
where VIN is the driving voltage applied to the anode of each LED, VF is the forward voltage drop of the LED, and VSINK is the voltage at each Dx. When VIN is high (fully charged battery), VSINK is internally regulated to take the voltage difference between VIN and VF. For instance, if VIN is 4V and VF for LED1 is 3.1V, then VSINK at D1 pin is 0.9V.

When VIN decreases (as the battery discharges), VIN(MIN) governs the lowest supply voltage for the LEDs without losing regulation. The design rule of thumb is to make sure the cut-off voltage is higher than VIN(MIN) for all conditions. It is important to emphasize the definition of “losing regulation”; in this datasheet it is defined as when the LED current drops to 90% of the nominal programmed current level.

At 24mA, the typical VSINK can be as low as 75mV for each Dx pin. Since every LED has a slightly different VF at a given current, the minimum VIN is determined by the highest VF plus 75mV typical. For the case of 24mA programmed current and highest VF of 3.2V, VIN in can go as low as 3.275V without losing LED current regulation. When VIN drops further while the VSINK(MIN) remains constant, VF will be forced lower. As a result, the LED current will reduce according to each LED’s V-I curve.

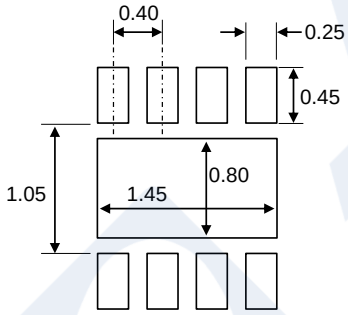
Packaging Information

UTDFN 1.5x1.5 – 8 pin



Dimension	mm		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A3		0.127 REF.	
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.45	1.50	1.55
D2	1.15	1.20	1.25
E	1.45	1.50	1.55
E2	0.65	0.70	0.75
e		0.40 BSC	
L	0.125	0.175	0.225
K	0.200	-	-

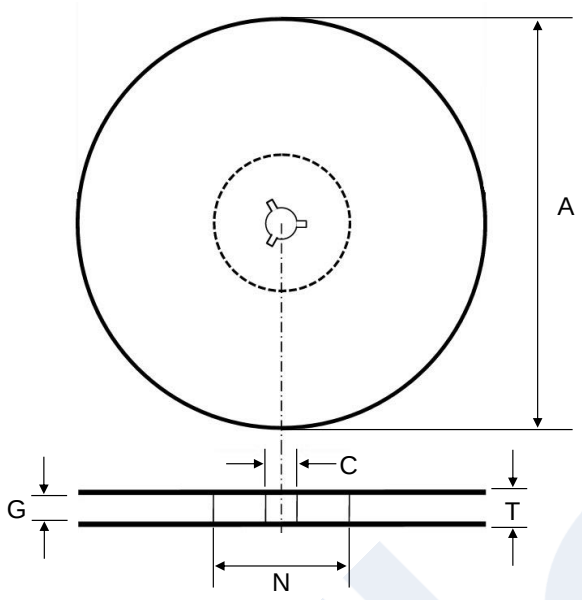
Recommended Footprint



* Dimensions are in millimeters.

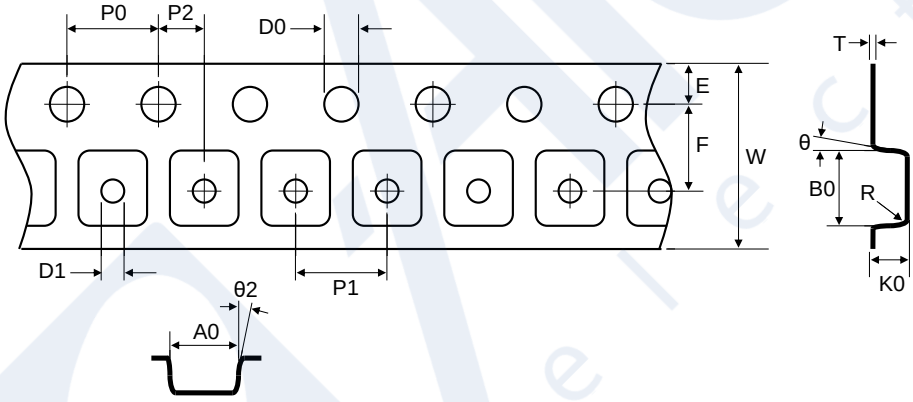
Tape and Reel Specifications

Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	180
C	12.8	13.0	13.5
G	7.9	–	10.9
N	50	55	60
T	–	–	14.4

Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	1.65	1.70	1.75
B0	1.65	1.70	1.75
K0	0.65	0.70	0.75
P0	3.9	4.0	4.1
P1	3.9	4.0	4.1
P2	1.95	2.00	2.05
D0	1.5	1.55	1.6
D1	1.00	–	–
E	1.65	1.75	1.85
F	3.45	3.50	3.55
10P0	39.8	40.0	40.2
W	7.9	8.0	8.3
T	0.18	0.20	0.22
Θ	0°	–	5°
Θ2	0°	–	5°