Version: Reference only

TECHNICAL SPECIFICATION

MODEL: 28 inch Color EPD

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TECHNICAL SPECIFICATION

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1. General Description

28 inch color EPD is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. The diagonal length of active area is 28” and contains 3840 x 1080 pixels and 32:9 aspect ratio. The display is capable to display multiple colors image depending on the display controller and the associated lookup table used.

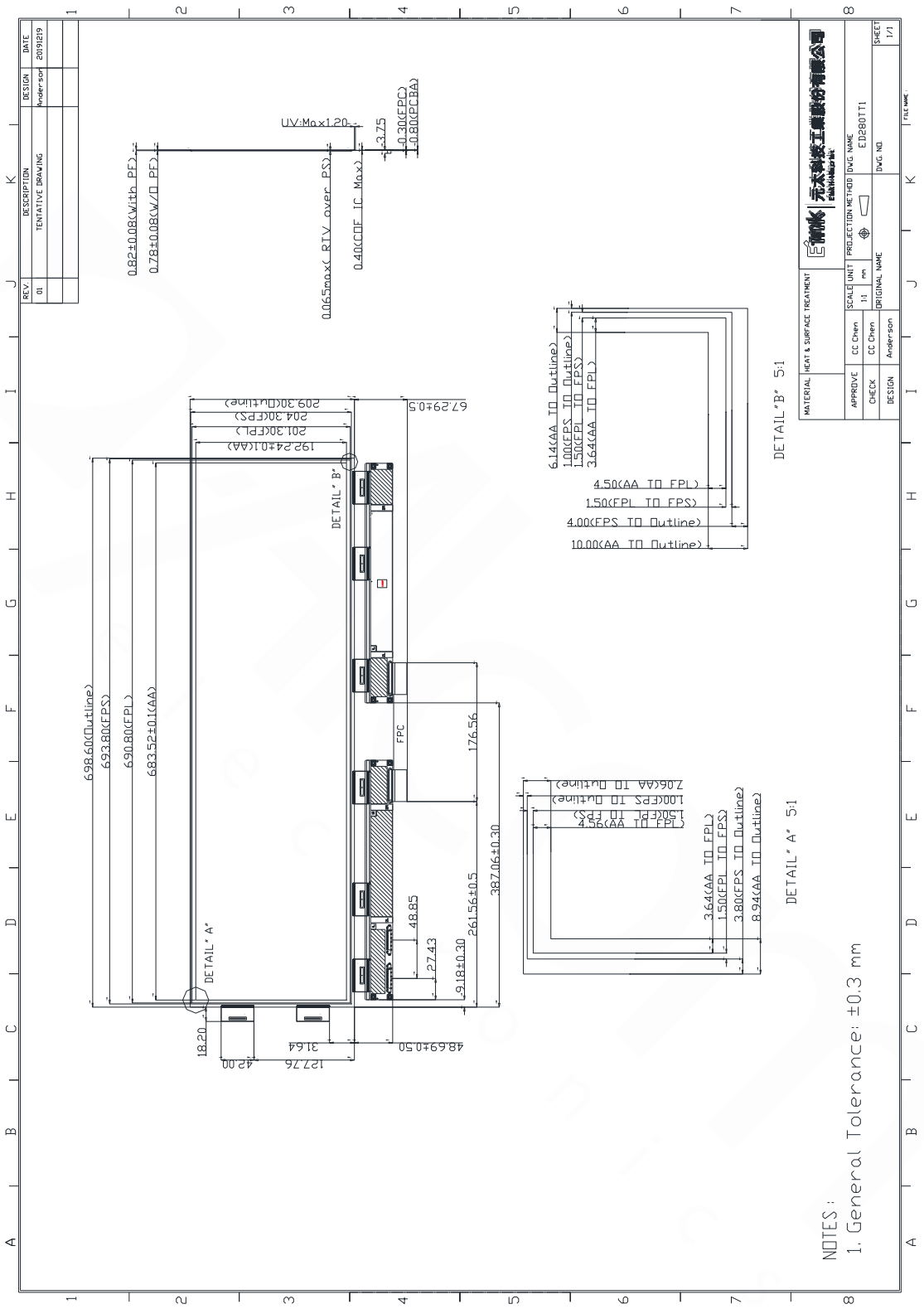
2. Features

- Color display
- Ultra-wide viewing angle
- Pure reflective mode
- Bi-stable
- Commercial temperature range (15 ~ 35 °C)
- Antiglare hard-coated front-surface

3. Mechanical Specifications

Parameter	Design	Unit	Remark
Screen size	28	inch	
Display Resolution	3840 (H) x 1080 (V)	Pixel	Aspect: 32:9
DPI	143	dpi	
Active Area	683.52(H) × 192.24(V)	mm	
Outline dimension	698.6(W) × 209.3(H) × 0.953(D)	mm	
Pixel Pitch	0.178 (H) x 0.178 (V)	mm	
Pixel Configuration	Square		
Border Size	8.0/7.08/7.06/8.0	mm	(L/R/U/D)
Display operation mode	Reflective mode		
FPL	E Ink Gallery™ 4000		
Surface Treatment	Anti-glare		
Driver IC	Source COF: Himax HX-5271 Gate COF: Solomon SPD1652		

4. Mechanical Drawing of Display Module



5. Input / Output Interface

5-1) Connector type:

Item	Pin numbers	Pitch (mm)	Connector	Note
CN1	51	0.5	P-TWO 187059-51221-1	LVDS Type
CN2	51	0.5	P-TWO 187059-51221-1	LVDS Type

5-2) Pin Assignment

Connector CN1

Pin #	Signal	Description	Remark
1	FPL_VCOM	Common Voltage.	
2	FPL_VCOM	Common Voltage.	
3	FPL_VCOM	Common Voltage.	
4	NC	NO Connection	
5	TFT_VCOM	Common Voltage.	
6	TFT_VCOM	Common Voltage.	
7	NC	NO Connection	
8	NC	NO Connection	
9	NC	NO Connection	
10	VGH	Positive power supply gate driver.	
11	VGH	Positive power supply gate driver.	
12	NC	NO Connection	
13	VP3	Positive power supply source driver.	
14	VP3	Positive power supply source driver.	
15	VP3	Positive power supply source driver.	
16	NC	NO Connection	
17	VP2	Positive power supply source driver.	
18	VP2	Positive power supply source driver.	
19	VP2	Positive power supply source driver.	
20	NC	NO Connection	
21	VP1	Positive power supply source driver.	
22	VP1	Positive power supply source driver.	
23	VP1	Positive power supply source driver.	
24	NC	NO Connection	
25	VDD	Logic power.	
26	VDD	Logic power.	
27	NC	NO Connection	
28	VSS	Ground	
29	VSS	Ground	
30	NC	NO Connection	
31	VN1	Negative power supply source driver.	
32	VN1	Negative power supply source driver.	
33	VN1	Negative power supply source driver.	
34	NC	NO Connection	
35	VN2	Negative power supply source driver.	
36	VN2	Negative power supply source driver.	
37	VN2	Negative power supply source driver.	
38	NC	NO Connection	
39	VN3	Negative power supply source driver.	
40	VN3	Negative power supply source driver.	
41	VN3	Negative power supply source driver.	
42	NC	NO Connection	
43	VGL	Negative power supply gate driver.	
44	VGL	Negative power supply gate driver.	
45	NC	NO Connection	
46	NC	NO Connection	
47	NC	NO Connection	
48	NC	NO Connection	
49	STBYB	mini-LVDS enable.	
50	XON	XON signal gate driver	

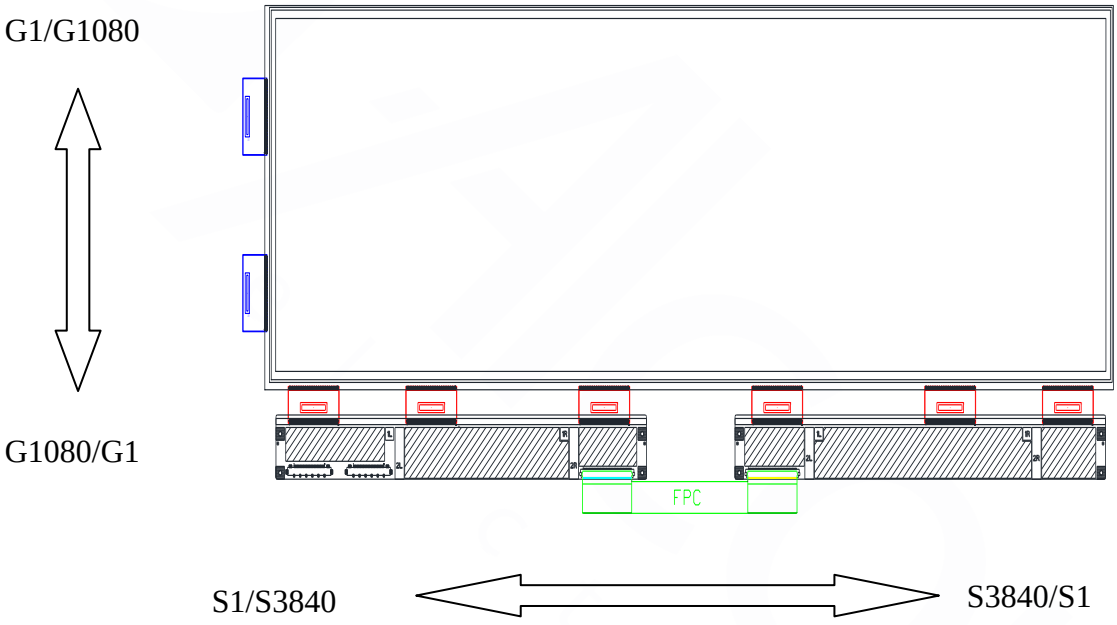
51	MODE	Output enable gate driver	

Connector CN2

Pin #	Signal	Description	Remark
1	DSEL	Data Input select	
2	LEH	Latch enable source driver	
3	OEH	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”.	
4	UD	Shift direction control pin gate driver UD = H: Data shift direction from G1 to G800. UD = L: Data shift direction from G800 to G1.	
5	SHR	Shift direction control pin source driver SHR =H: Data inputs read sequentially from S800 to S1. SHR =L: Data inputs read sequentially from S1 to S800.	
6	SPV2	Start pulse gate driver UD / Start pulse input / Start pulse output H / SPV1 / SPV2 L / SPV2 / SPV1	
7	SPV1	Start pulse gate driver UD / Start pulse input / Start pulse output H / SPV1 / SPV2 L / SPV2 / SPV1	
8	SPH2	Start pulse source driver SHR / Start pulse input / Start pulse output H / SPH2 / SPH1 L / SPH1 / SPH2	
9	SPH1	Start pulse source driver SHR / Start pulse input / Start pulse output H / SPH2 / SPH1 L / SPH1 / SPH2	
10	VSS	Ground	
11	CKV	Clock gate driver	
12	VSS	Ground	
13	LV11N	Data signal source driver	
14	LV11P	Data signal source driver	
15	VSS	Ground	
16	LV10N	Data signal source driver	
17	LV10P	Data signal source driver	
18	VSS	Ground	
19	LV9N	Data signal source driver	
20	LV9P	Data signal source driver	
21	VSS	Ground	
22	LV8N	Data signal source driver	
23	LV8P	Data signal source driver	
24	VSS	Ground	
25	LV7N_D15	Data signal source driver	
26	LV7P_D14	Data signal source driver	
27	VSS	Ground	
28	LV6N_D13	Data signal source driver	
29	LV6P_D12	Data signal source driver	
30	VSS	Ground	
31	CLKN_GLOSTL	Data signal source driver	
32	CLKP_CKH	Data signal source driver	
33	VSS	Ground	
34	LV5N_D11	Data signal source driver	
35	LV5P_D10	Data signal source driver	
36	VSS	Ground	
37	LV4N_D9	Data signal source driver	
38	LV4P_D8	Data signal source driver	

39	VSS	Ground	
40	LV3N_D7	Data signal source driver	
41	LV3P_D6	Data signal source driver	
42	VSS	Ground	
43	LV2N_D5	Data signal source driver	
44	LV2P_D4	Data signal source driver	
45	VSS	Ground	
46	LV1N_D3	Data signal source driver	
47	LV1P_D2	Data signal source driver	
48	VSS	Ground	
49	LV0N_D1	Data signal source driver	
50	LV0P_D0	Data signal source driver	
51	VSS	Ground	

5-3) Panel Scan Directions



6. Display Module Electrical Characteristics

6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5	V	
Positive Supply Voltage	VP3	-0.3 to +18	V	
	VP2	-0.3 to +18	V	
	VP1	-0.3 to +18	V	
Negative Supply Voltage	VN1	-18 to + 0.3	V	
	VN2	-18 to + 0.3	V	
	VN3	-18 to + 0.3	V	
Max .Drive Voltage Range	VPx - VNx	36	V	
Supply Voltage	VGH	-0.3 to +55	V	
Supply Voltage	VGL	-32 to +0.3	V	
Supply Range	VGH-VGL	-0.3 to +55	V	
Operating Temp. Range	TOTR	+15 to +35	℃	
Storage Temperature	TSTG	-25 to +50	℃	

6-2) Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V			TBD	mA
Gate negative supply	VGL		-22	-20	-19	V
	IGL	VGL=-20V			TBD	mA
Gate Positive supply	VGH		26	27	29	V
	IGH	VGH=27V			TBD	mA
Source negative supply	VN1		-13.5	Adjusted	-7.5	V
	IN1				TBD	mA
Source negative supply	VN2		-2.65	-2.5	-2.25	V
	IN2				TBD	mA
Source negative supply	VN3		-16.5	-15	-12.5	V
	IN3				TBD	mA
Source Positive supply	VP1		8.5	Adjusted	18	V
	IP1				TBD	mA
Source Positive supply	VP2		8.5	10	12.5	V
	IP2				TBD	mA
Source Positive supply	VP3		14	16	18	V
	IP3				TBD	mA
Common voltage	Vcom_TFT		-20.0	Adjusted	20.0	V
	Icom_TFT			TBD	TBD	mA
	Vcom_FPL		-20.0	Adjusted	20.0	V
	Icom_FPL			TBD	TBD	mA
Maximum Power panel	Pmax				TBD	mW
Typical power panel	Ptyp			TBD		mW
Standby power panel	Pstby				TBD	mW

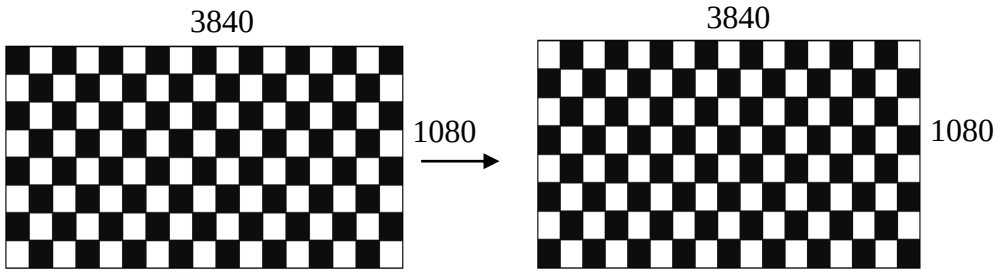
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	IPx	VPx = 15V	-		TBD	mA
	INx	VNx = -15V	-		TBD	mA
	IGH	V_{GH} = 27V	-		TBD	mA
	IGL	V_{GL} =-20V	-		TBD	mA
	ICOM	--	-		TBD	mA

Note :

1. The maximum average Currents for power consumption are measured using 65 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
2. The Typical average current for power consumption is measured using 65 Hz waveform with following pattern transition: from horizontal 8 generic color pattern to vertical 8 generic color pattern. (Note 6-2)
3. The standby power is the consumed power when the panel controller is in standby mode.
4. The Maximum Currents are measured using 65 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
5. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
6. Vcom is recommended to be set in the range of assigned value ± 0.1 V
7. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
8. The maximum current is for reference only.

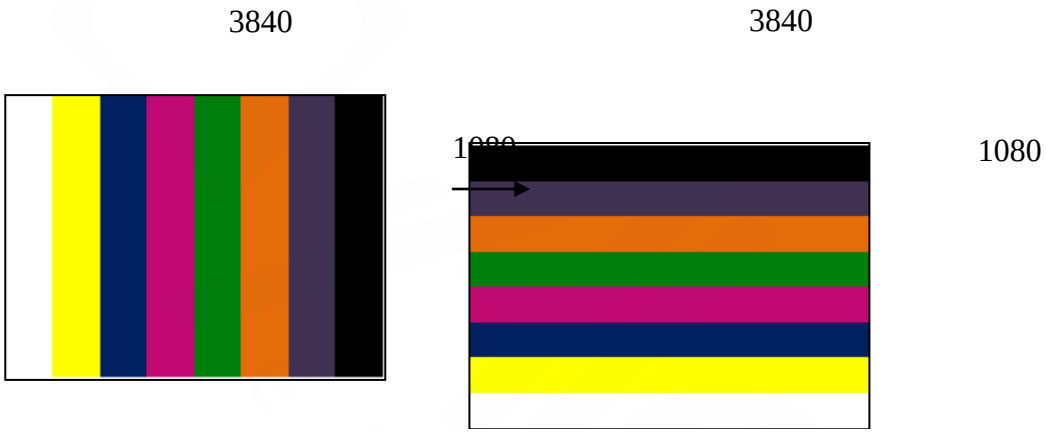
Note6-1

The maximum average current and Maximum Currents



Note6-2

The typical power consumption



Note6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
IPx	2.2uF x 1pcs / ±15% x 24 pcs
INx	2.2uF x 1pcs / ±15% x 24 pcs
IGH	2.2uF x 1pcs / ±15% x 2 pcs
IGL	2.2uF x 1pcs / ±15% x 3 pcs
ICOM	No Capacitor

6-3) Refresh Rate

The 28” color EPD is applied at a maximum screen refresh rate of 65Hz.

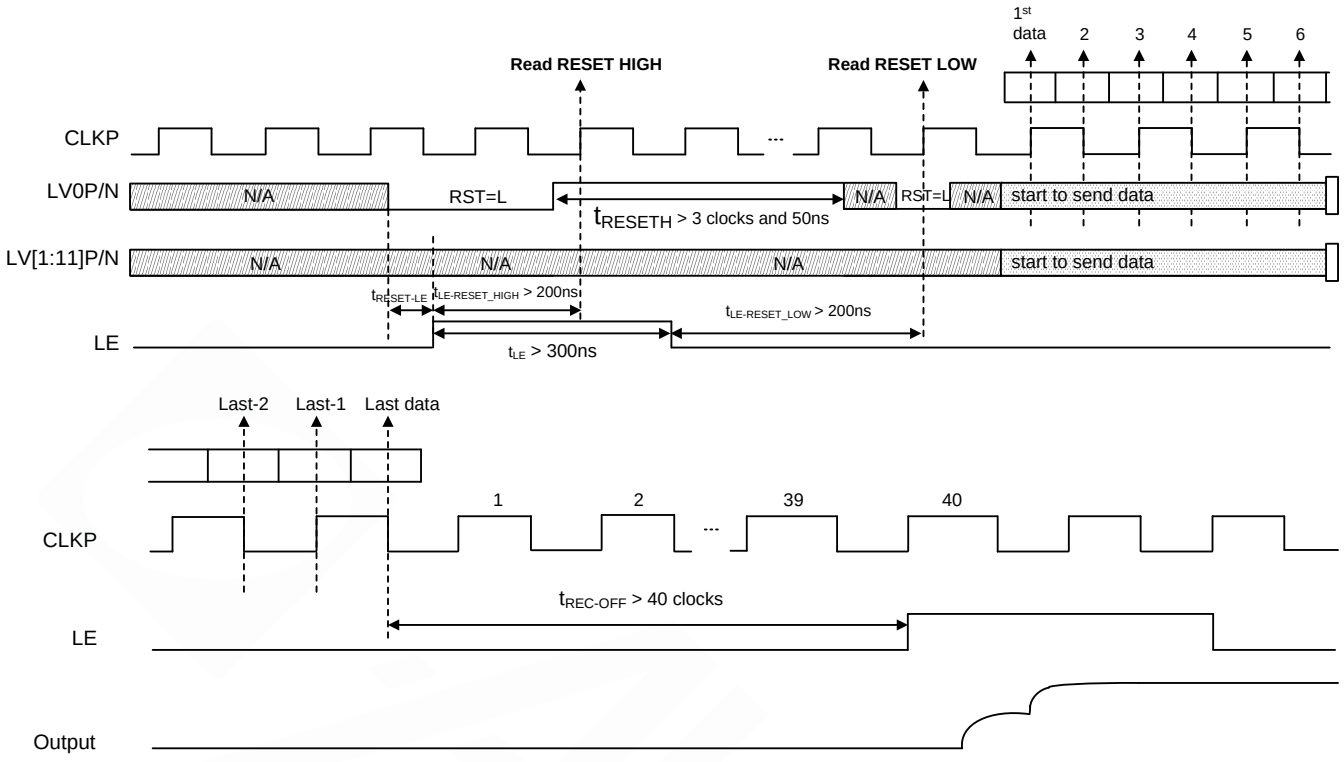
	Min.	Typ.	Max.
Refresh Rate	-	65 Hz	-

6-4) Panel AC characteristics

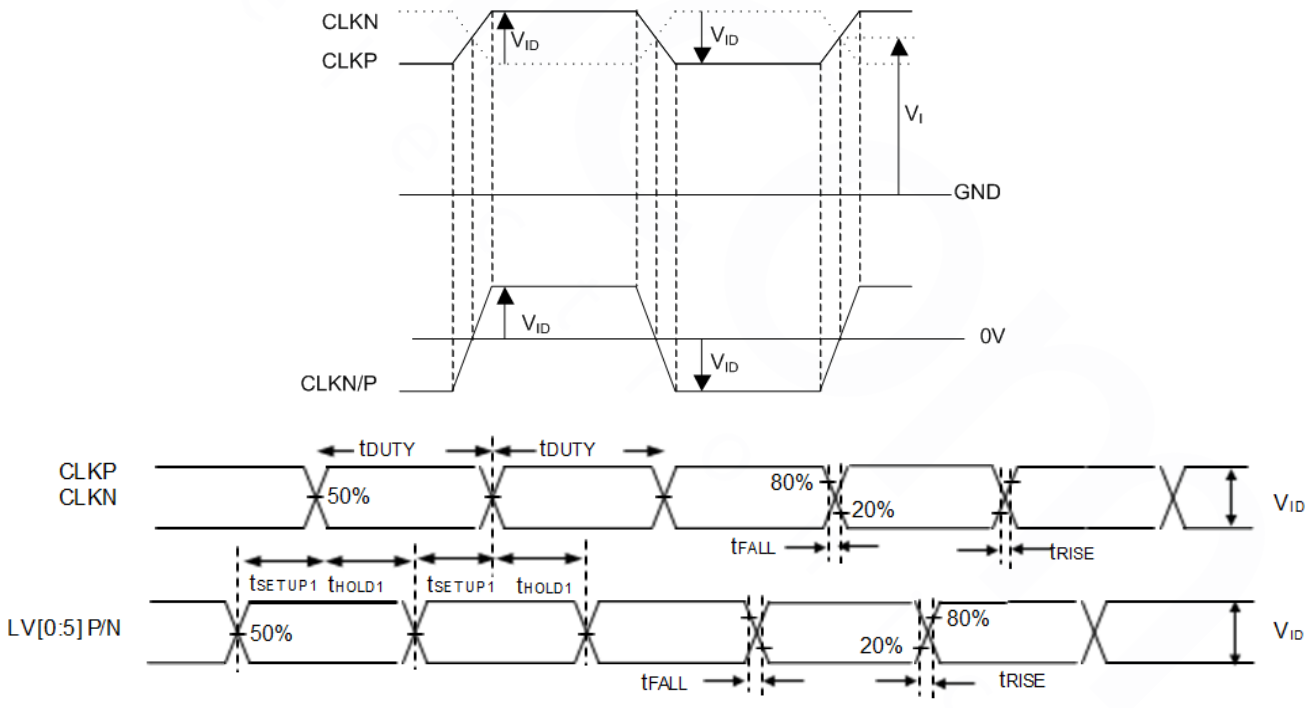
VDD=2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock duty	t_{DUTY}	45	-	55	%
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE\text{-}RESET\_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE\text{-}RESET\_LOW}$	200	-	-	ns
Start pulse delay time	t_{PLH1}	-	-	4	CLK
	t_{PHL1}	-	-	4	CLK
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC\text{-}OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Reset low to LE rising time	$t_{RESET\text{-}LE}$	0	-	-	ns
Gate clock frequency	f_{CLK}	-	-	200	kHz
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	t_{CLKH}-100	ns
Gate Start pulse hold time	t_{HD}	100	-	t_{CLKL}-100	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns
Gate STV output delay from CLK	t_{OD_STV}	-	-	500	ns
Output delay time from CLK	t_{D_OUT}	-	-	2	us
Output rise time, output pins	t_{R_OUT}	-	-	1	us
Output fall time, output pins	t_{F_OUT}	-	-	1	us
XONL/R pulse width	t_{WXON}	10	-	-	us
Output delay time from XON	t_{DXON_OUT}	-	-	20	us

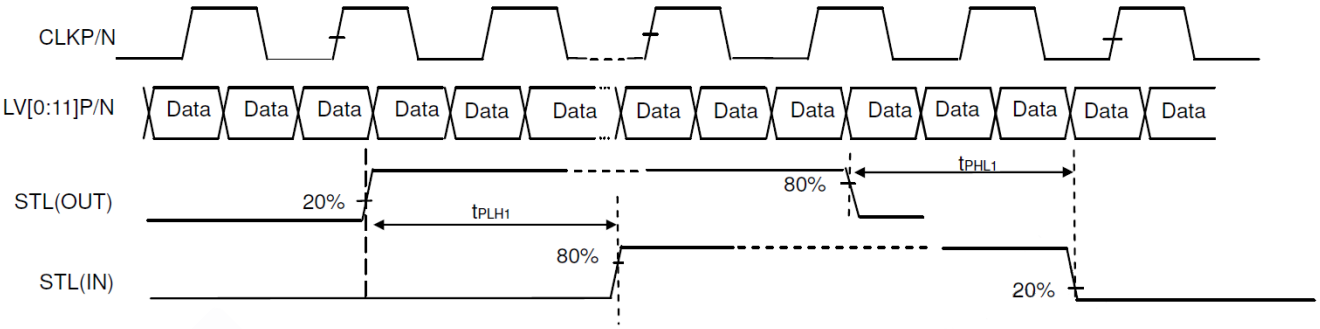
OUTPUT LATCH CONTROL SIGNALS



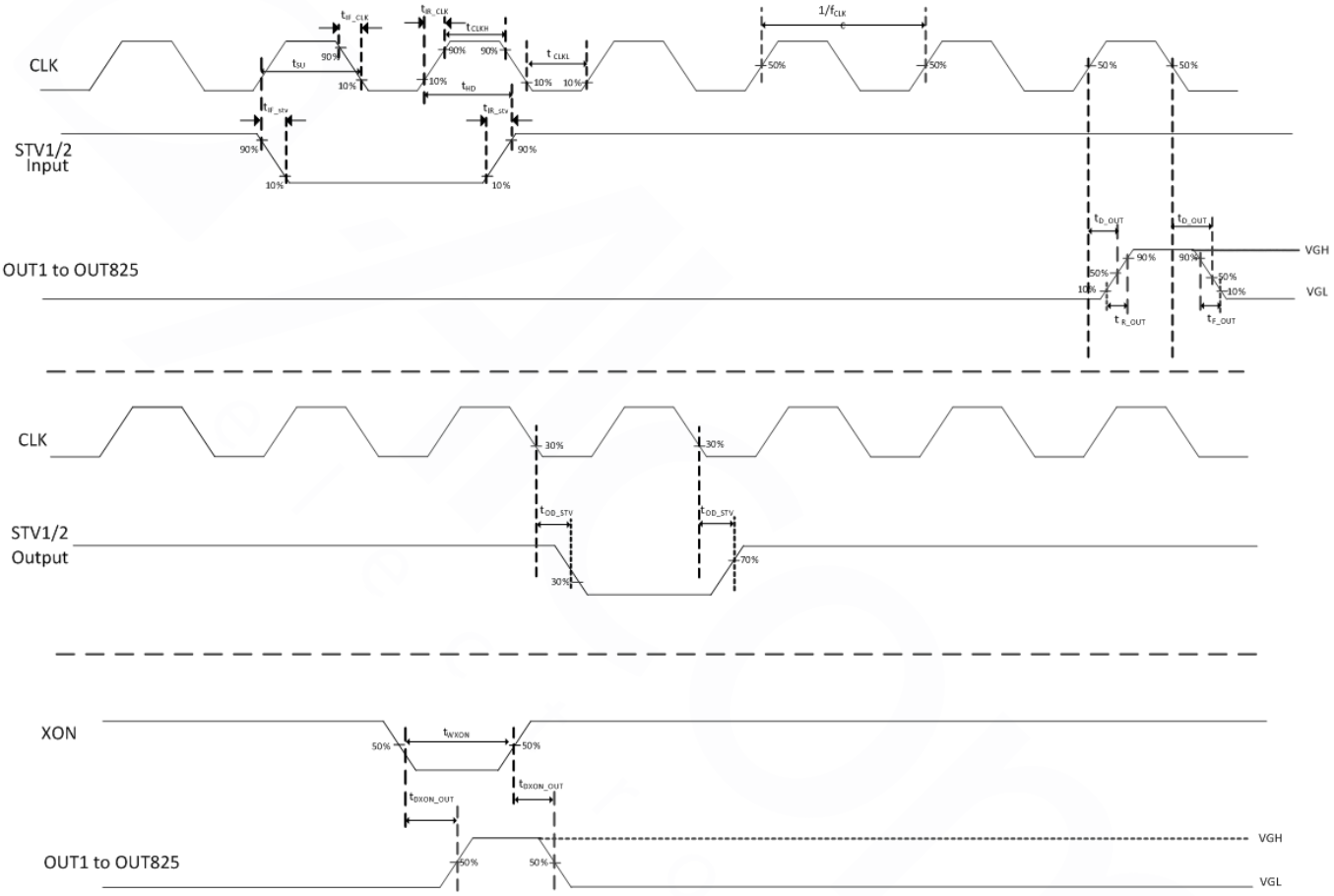
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：First gate line on timing
After 5CLK, Gate OUT1 is on.

6-5) Controllers Timing

The timing mode is depicted on Figure 6.1 and Figure 6.2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

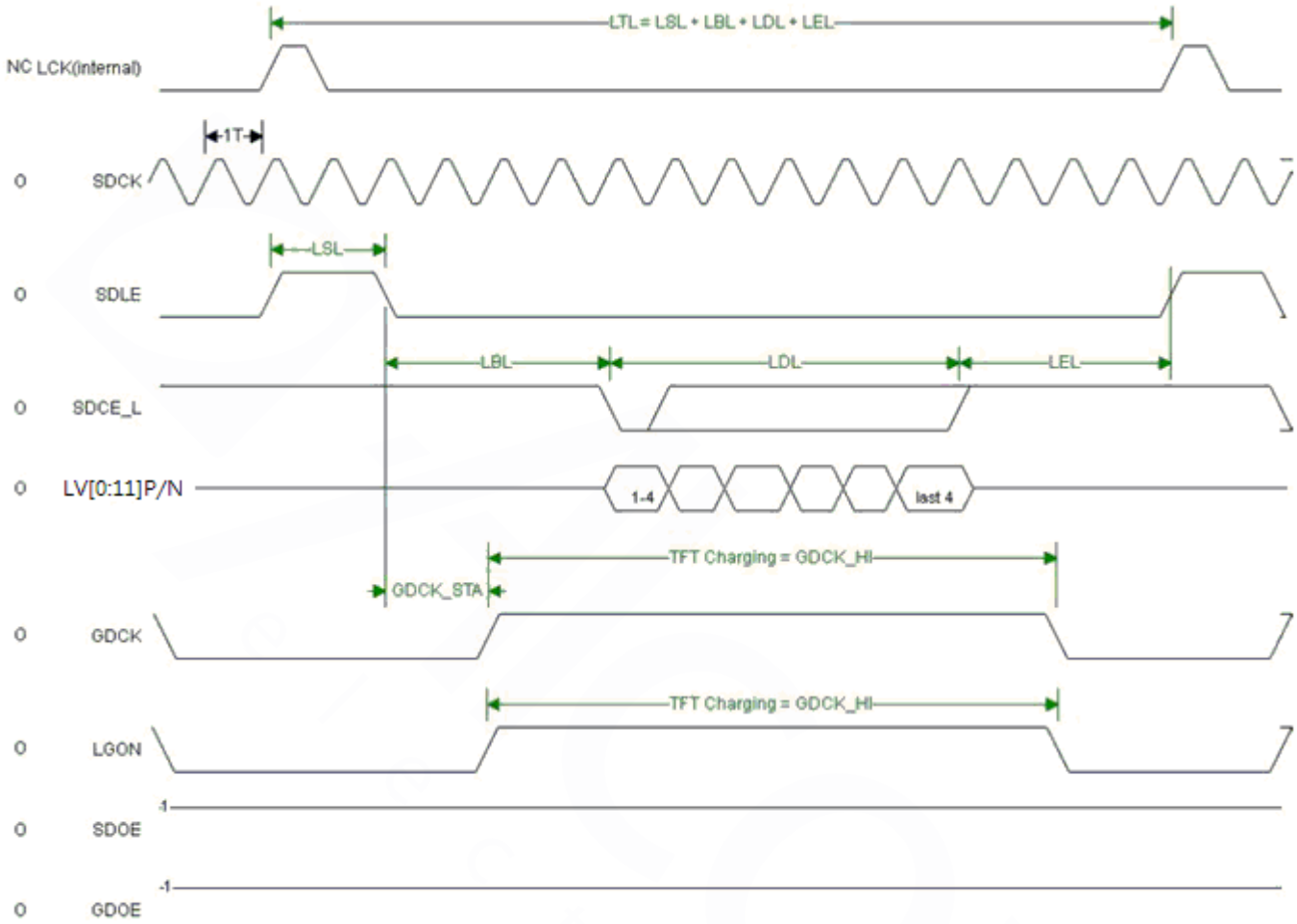


Figure 6.1 Line Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.

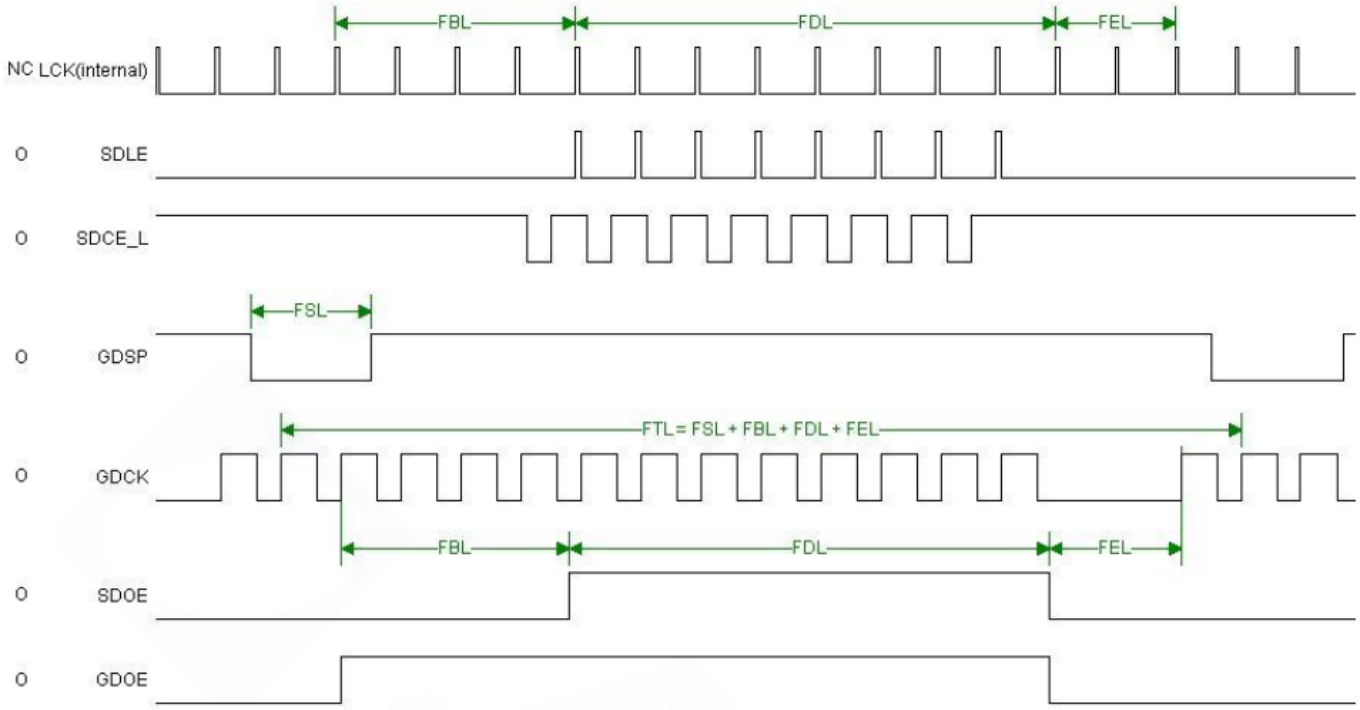


Figure 6.2 Frame Timing in Mode 3

Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL
Note 2:
SDCLK = XCL
LV[0:11]P/N = LV0P~LV11N
SDCE_L = XSTL
GDCK = CKV
GDSP = SPV
GDOE = Mode1
SDOE = XOE

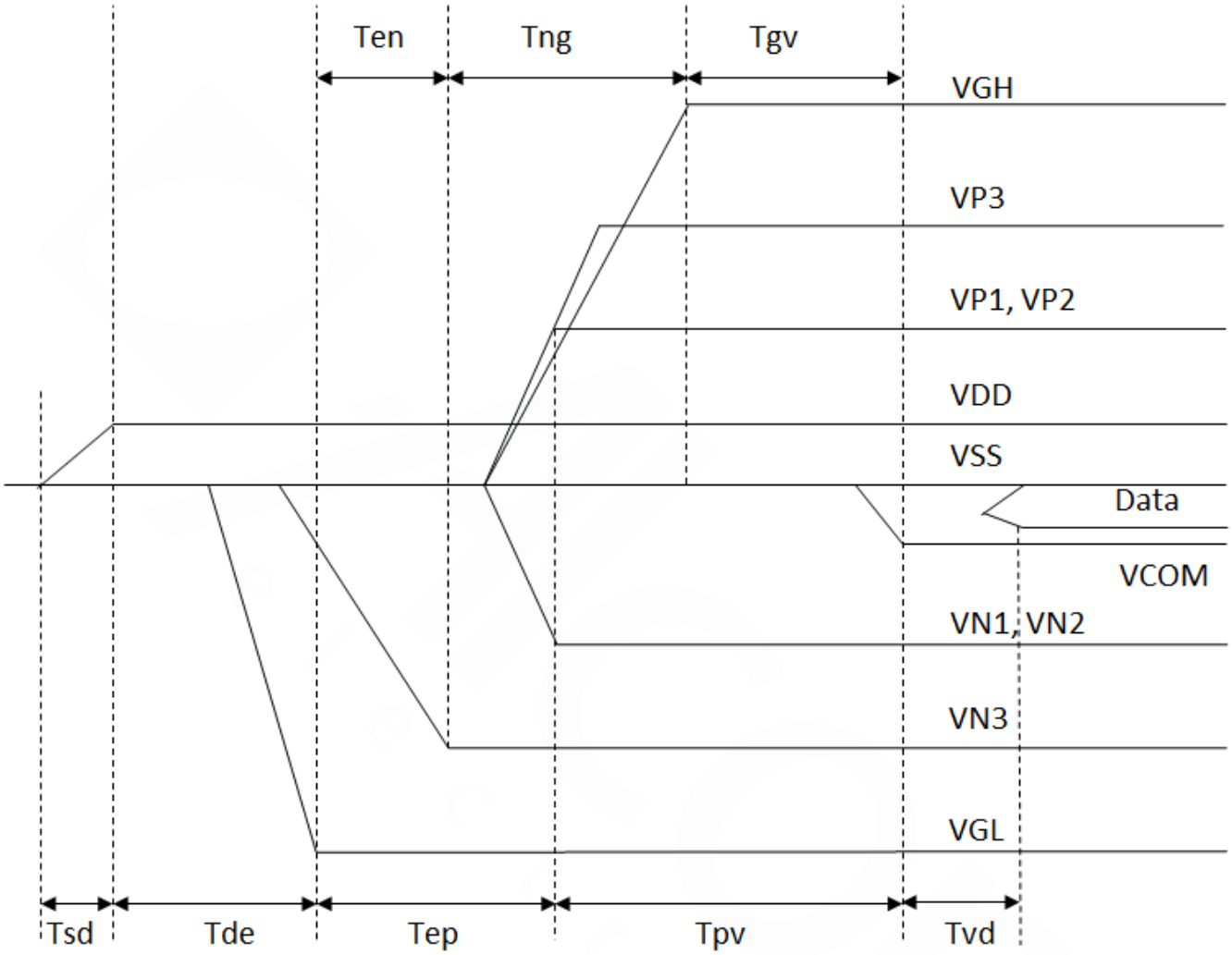
7. Power Sequence

Power Rails must be sequenced in the following order：

1. VSS → VDD → VNx → VPx (Source driver) → VCOM

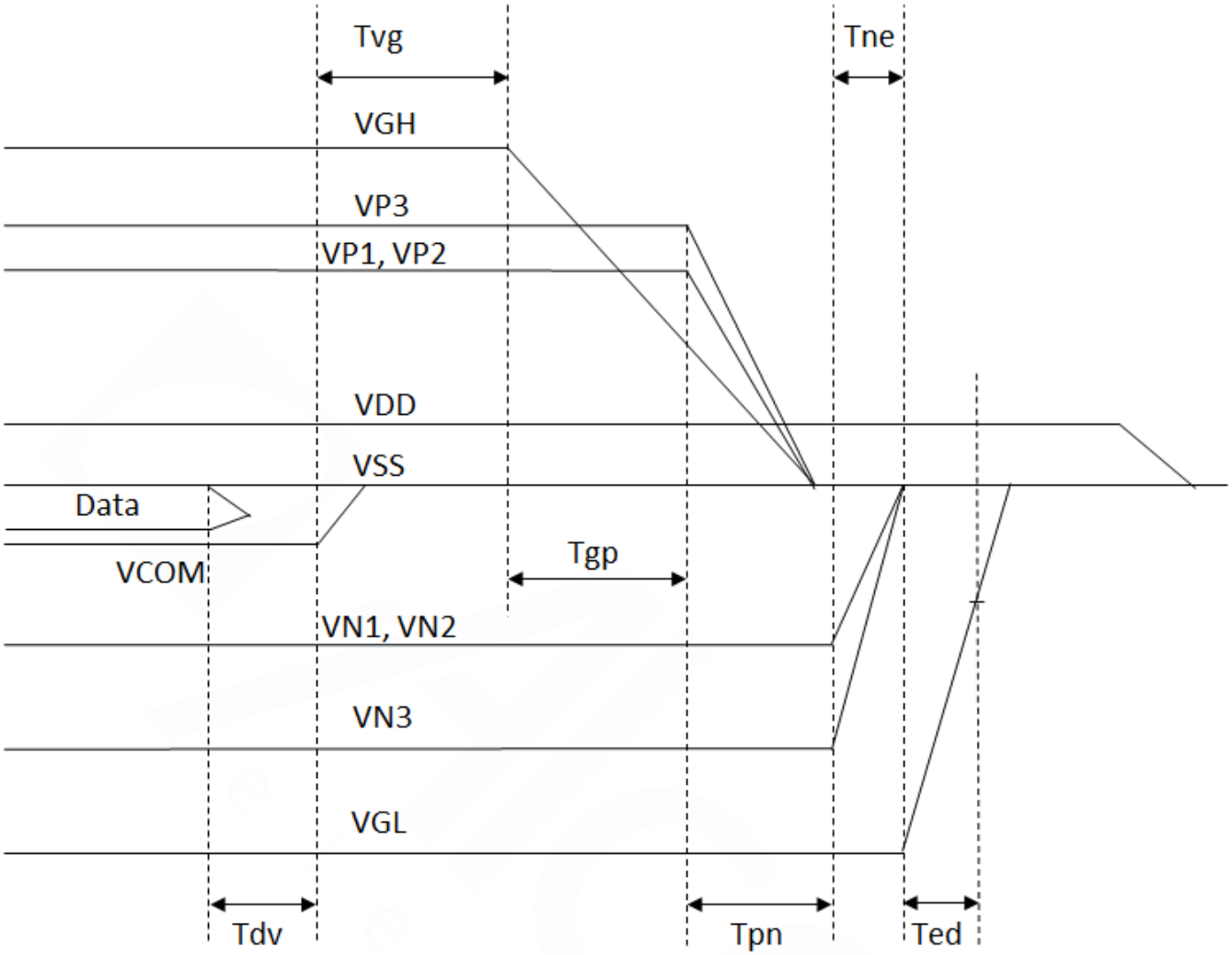
2. VSS → VDD → VGL → VGH (Gate driver)

POWER ON



	Min	Max	Remark
Tsd	30us	-	
Tde	100us	-	
Tep	1000us	-	
Tpv	100us	-	
Tvd	100us	-	
Ten	0us	-	
Tng	1000us	-	
Tgv	100us	-	

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

8. Optical characteristics

8-1) Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
CR	Contrast Ratio	KW		10	-		-
Gamut	Color Saturation	-		60K		dE^3	
Dither Color	Color Performance	Cyan (0,131,163)		TBD		L*,a*,b*	Note 8-1 8-2
		Magenta (196,0,137)		TBD			
		Yellow (216,203,0)		TBD			
		Red (190,26,0)		TBD			
		Green (0,137,39)		TBD			
		Blue (59,0,137)		TBD			
		Black (0,0,0)		TBD			
		White (255,255,255)		TBD			
T_{update_RS}	Update time	Image to Image (A→W→B)		25		sec	

Note 8-1：The rendered color inputs are chosen to have the highest saturation within a given color; They are not sRGB primaries

Note 8-2：Performance values at 25 ℃ ambient; 8 dither color

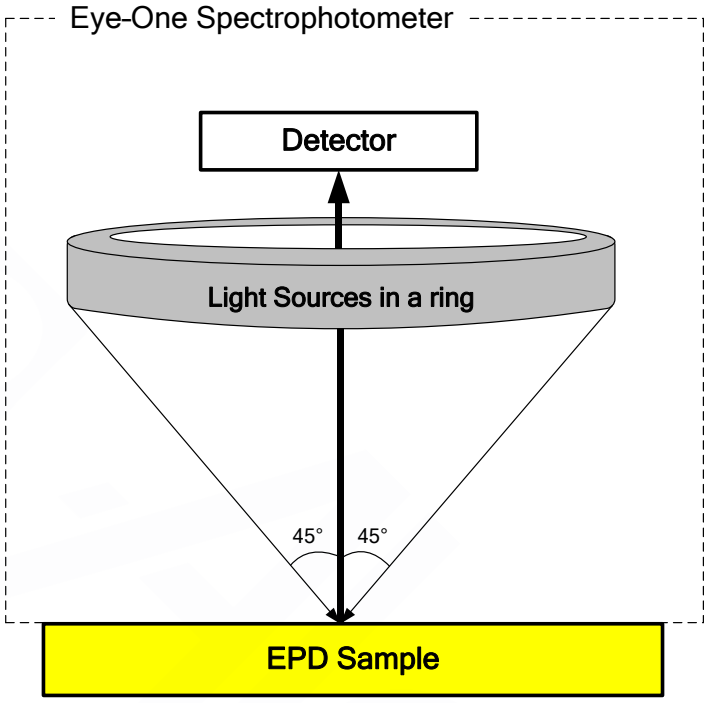
※This is the preliminary performance and is subjected to change.

※Performance values at 25°C ambient.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd)：

CR = Rl/Rd



8-3) Reflection Ratio

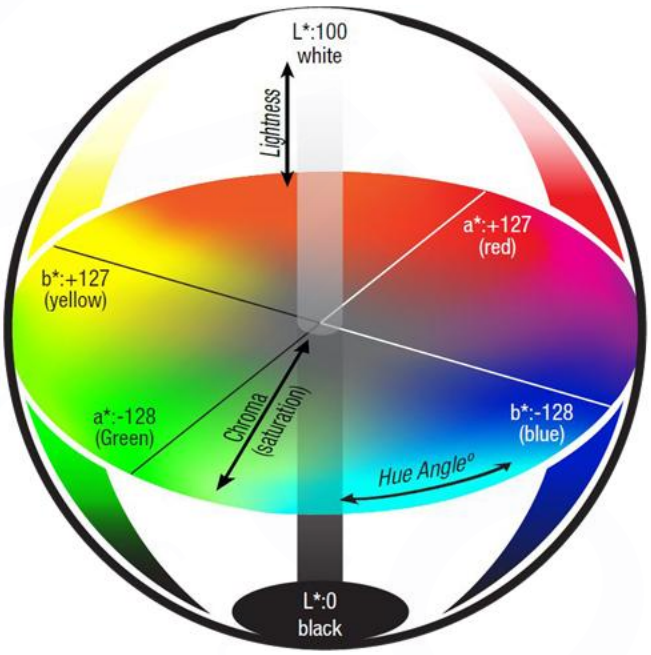
The reflection ratio is expressed as：

$R = \text{Reflectance Factor}_{\text{white board}} \quad x \quad (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

8-4) Definition of Color Performance & Saturation ratio

The Spectroradiometer PR655 with MS-75 lens was used to measure color image to obtain L*, a*, b*. Collect L*, a*, b* and then determine the color space.



9. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause’s circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.
Data sheet status
Product specification
This data sheet contains Preliminary product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition these are stress ratings only and operation of the device at these or at any other condition to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification

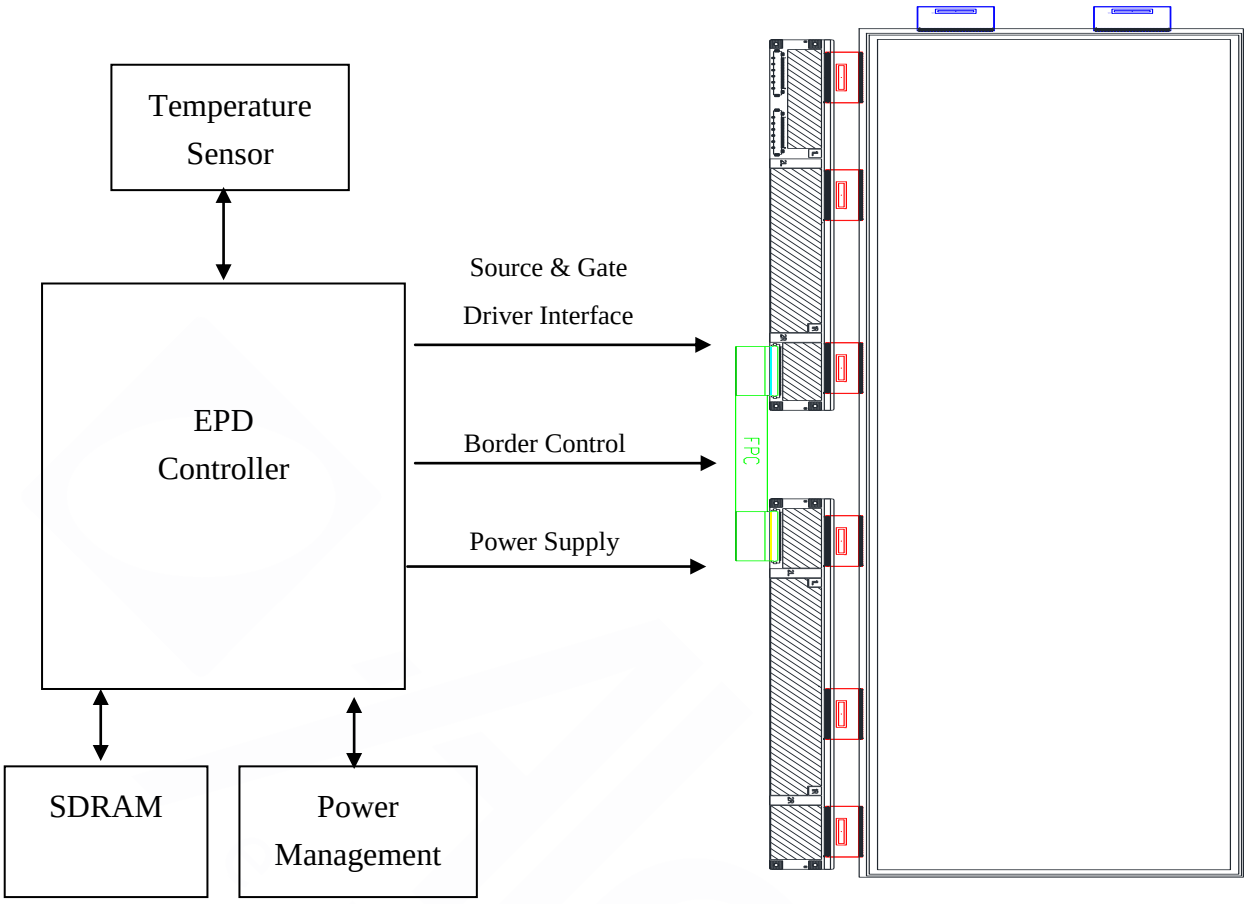
10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +35℃, RH = 50% for 240 hrs	IEC 60 068-2-2Bp	--
2	Low-Temperature Operation	T = 15℃, RH = 35% for 240 hrs	IEC 60 068-2-2Ab	--
3	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	--
4	High-Temperature Storage	T = +50℃, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
5	High-Temperature, High-Humidity Storage	T = +50℃, RH = 80% for 240 hrs	IEC 60 068-2-3CA	
6	Temperature Cycle	-25℃→+60℃, 50 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	--
7	Package Vibration	Random Wave (1.5Grms) Frequency: 10~200Hz Direction: X,Y,Z Duration: 30mins each direction	Full packed for shipment	PPBOX package
8	Package Drop Impact	Drop from height of 15.2 cm on concrete surface. Drop sequence: 6 flats	Full packed for shipment	PPBOX package
9	Electrostatic Effect (non-operating)	Air 15k, Contact 8k	IEC 62179, IEC 62180	--

Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

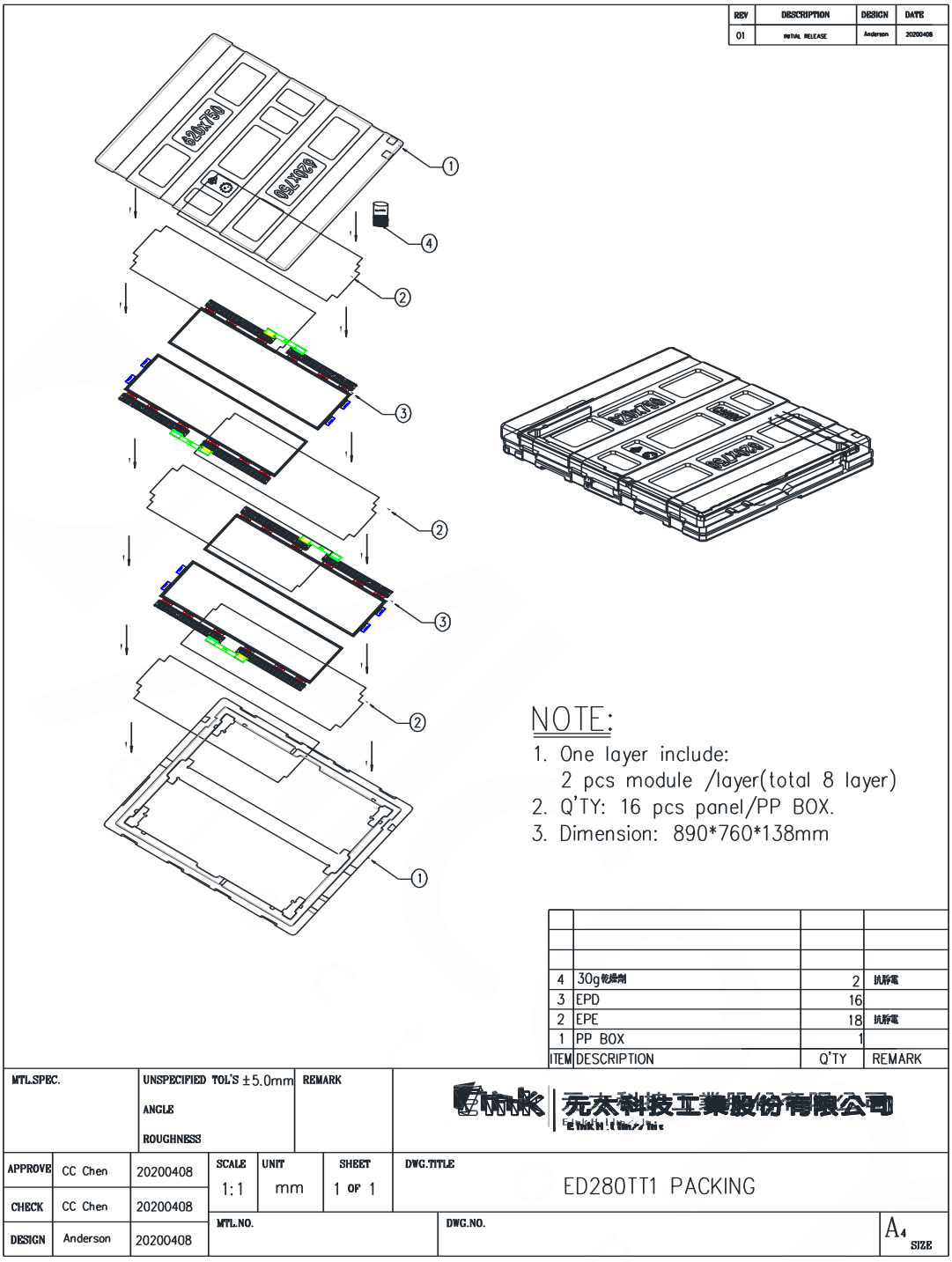
< Criteria >
In the standard conditions, there is not display function NG issue occurred. (Including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

11. Block Diagram

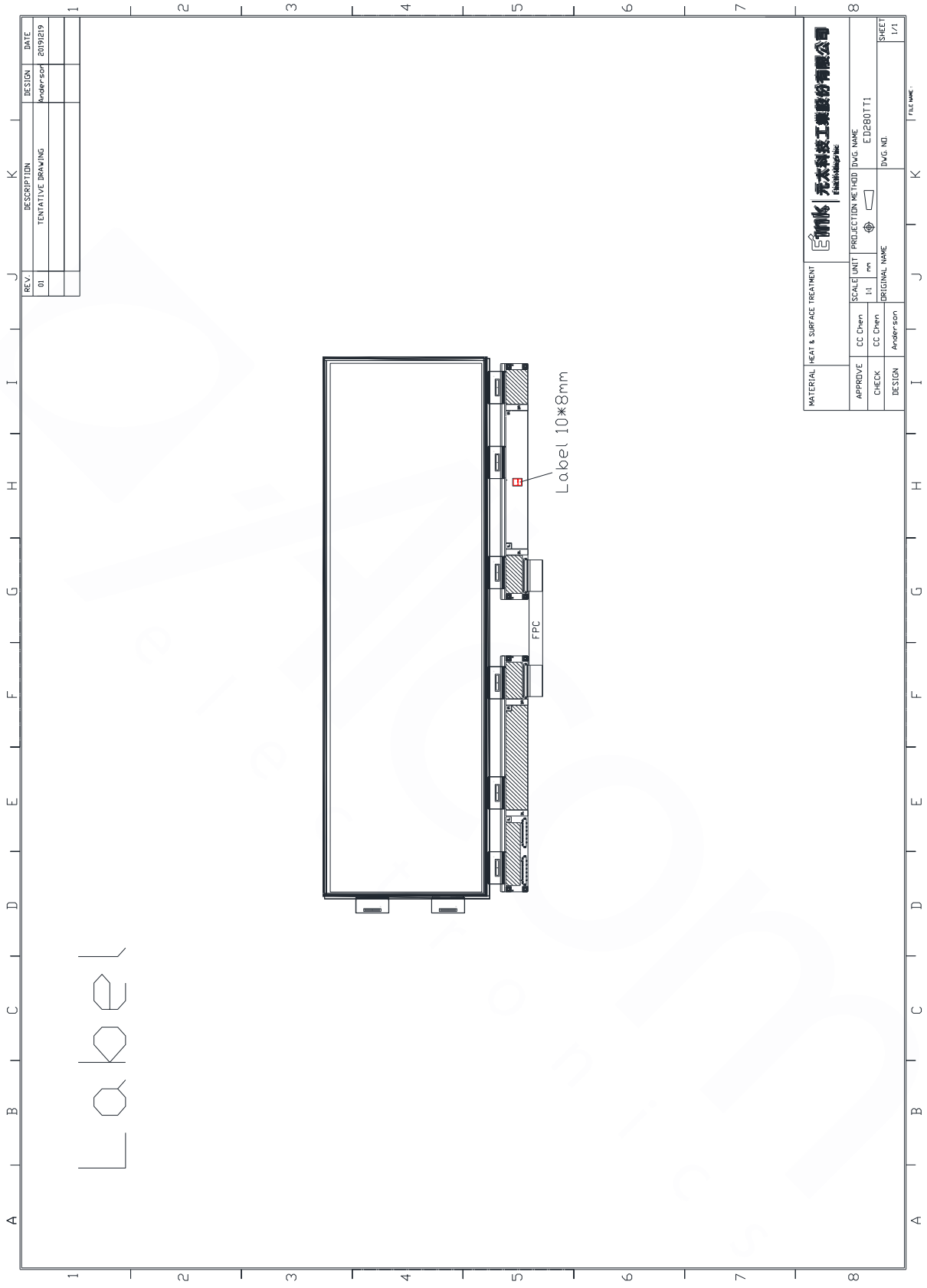


12. Packing

12-1) packing drawing



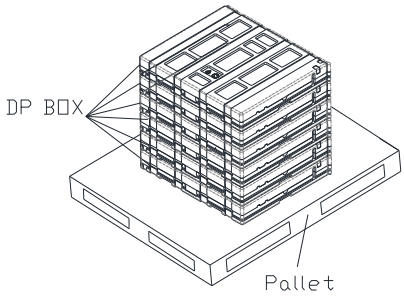
12-2) Label position

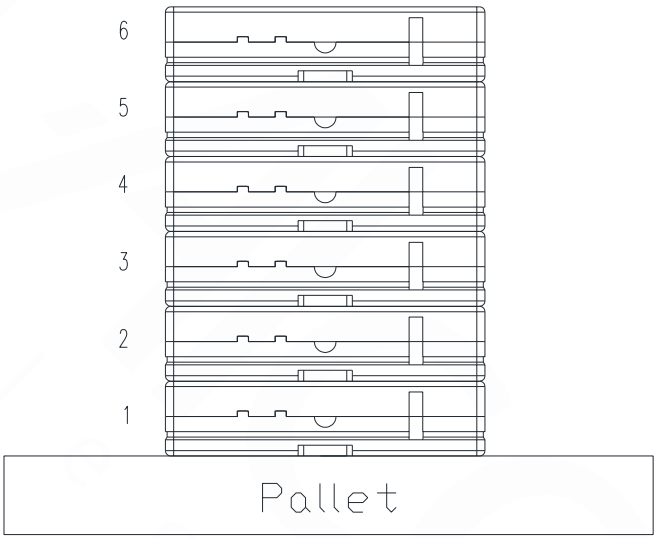


12-3) Pallet Stacking

Note: Stacking layer limitation: 6 layers.

REV	DESCRIPTION	DESIGN	DATE
1	INITIAL RELEASE	Anderson	20200602





NOTE:
1.Pallet Dimension:1150*950*114 mm
2.6Boxes/Pallet
3.PP Box Dimension :890*760*138mm

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
2		PP BOX	6	
1		Pallet	1	

MTL.SPEC.	UNSPECIFIED TOL'S	REMARK
	ANGLE	
	ROUGHNESS	

E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE	CC Chen	20200602	1:1	mm	1 OF 1	ED280TT1 Boxes&Pallet
CHECK	CC Chen	20200602				
DESIGN	Anderson	20200602	MTL.NO.			DWG.NO.

13. Bar Code definition

C01	R4	A	09	1	U	A	V	0007N	AT
1	2	3	4	2	5	6	2	7	2

1 : EPD model code

2 : Internal control codes

3 : FPL lot codes

4 : FPL lot codes

5 : Year:

U: 2019 / V: 2020 / W: 2021 /... / Z: 2024

6 : Month:

1:Jan. 2:Feb. ... 9:Sep. A:Oct. B:Nov. C:Dec.

7 : Serial codes