HT32F67742
Datasheet

**32-Bit Arm® Cortex®-M0+ BLE Microcontroller,
64 KB Flash and 8 KB SRAM with BLE, 1 Msps ADC,
DIV, USART, UART, SPI, I²C, GPTM, PWM, BFTM, SCI,
CRC, RTC, WDT, LCD and USB2.0 FS**

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1 General Description

The Holtek HT32F67742 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as BLE, USB2.0 FS, Hardware Divider DIV, SPI, USART, UART, SCI, I^2C, GPTM, PWM, BFTM, CRC-16/32, RTC, WDT, ADC, LCD and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as smart home appliances, smart sensor and data logging applications, smart toy applications, handheld equipment and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 64 KB on-chip Flash memory for instruction/data and option storage
- 8 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Bluetooth Low Energy Controller – BLEC

- 2.4 GHz RF transceiver compatible with Bluetooth Low Energy (BLE) 5.2 specification
- Programmable transmitter output power up to +3.5 dBm
- Excellent receiver sensitivity of -94 dBm @ 1 Mbps
- GFSK modulation, Frequency-Hopping Spread Spectrum (FHSS)
- Support LE 1 Mbps, 2 Mbps
- Three operating modes: Normal, Deep-Sleep and Power-Down

The Bluetooth Low Energy Controller, BLEC, is an ultra-low power 2.4 GHz RF transceiver compatible with the BLE 5.2 specification. With excellent receiver sensitivity and very low active RF current consumption, the device provides an excellent battery lifetime. The BLEC includes the RF transceiver, modem, protocol processing logic, link layer controller and link layer firmware library which support for Bluetooth 5.2 LE 1 Mbps and LE 2 Mbps connections. For power saving, the BLEC supports Deep-Sleep and Power-Down modes, which can be combined with the PWRCU (Power Management Control Unit) Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down operating modes to reduce power consumption for BLE applications.

Flash Memory Controller – FMC

- Flash accelerator to obtain maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated clock PLL and USB PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- V_{DD} power supply: 1.65 V to 3.6 V @ BLE OFF
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{DD} and V_{CORE} power domains
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of

power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 4 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include up to 4 external analog signal channels and 4 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D Conversion can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (V_{REF}) which can provide a stable reference voltage for the A/D Converter is internally connected to the ADC input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 49 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 49 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor

between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/ status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a quadrature decoder with two inputs.

Pulse-Width-Modulation Timer – PWM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse-Width-Modulation Timer, PWM, consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer

value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, i.e., when the device enters the power-saving mode, the RTC counter is used as a wakeup timer to let the system resume from the power saving mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization function to prevent the situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programming baud rate clock frequency up to (f_{PCLK}/16) MHz for Asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character Transfer mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (Elementary Time Unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and check functions
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface, SCI, is compatible with the ISO 7816-3 standard. This interface includes functions for Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by controlling the "START" bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Liquid Crystal Display Controller – LCD

- LCD Driver function with Static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty
- LCD Driver function with Static, 1/2, 1/3 or 1/4 bias
- Supports R type bias type
- Clock source can be selected from the LSI (32 kHz), LSE (32.768 kHz) or a clock ratio of either the HSI or HSE
- Contains three embedded LCD bias reference resistor ladders
- Double buffered memory
- Software selectable charge pump voltage
- Programmable dead time between frames – up to 7/2 phase periods for type A waveforms and 7 phase periods for type B waveforms
- Software selectable waveform type: type A or type B waveform
- LCD frame interrupt
- Blink capability: Up to 1, 2, 3, 4, 8 or all pixels which can be programmed to blink

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays. It includes up to 8 common terminals and 29 segment terminals to drive 116 (4 commons × 29 segments) or 200 (8 commons × 25 segments) LCD picture elements (pixels). The exact number of terminals depends on the device package pin out. An integrated charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 Full-Speed (12 Mbps) specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffers. Each endpoint buffer size is programmable using corresponding registers, thus providing maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 80-pin LQFP-EP package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F67742
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	GPTM	1
	PWM	2
	BFTM	2
	WDT	1
	RTC	1
Communication	USB	1
	SPI	2
	USART	1
	UART	2
	I²C	2
	SCI (ISO7816-3)	1
Hardware Divider		1
LCD (COM × SEG)		Up to 8 × 25, 6 × 27, 4 × 29
CRC-16/32		1
EXTI		16
12-bit ADC Number of channels 4 Channels		1
GPIO		Up to 49
BLE		1
CPU frequency		Up to 60 MHz
Operating voltage (@ BLE ON)		2.0 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		80-pin LQFP-EP

Block Diagram

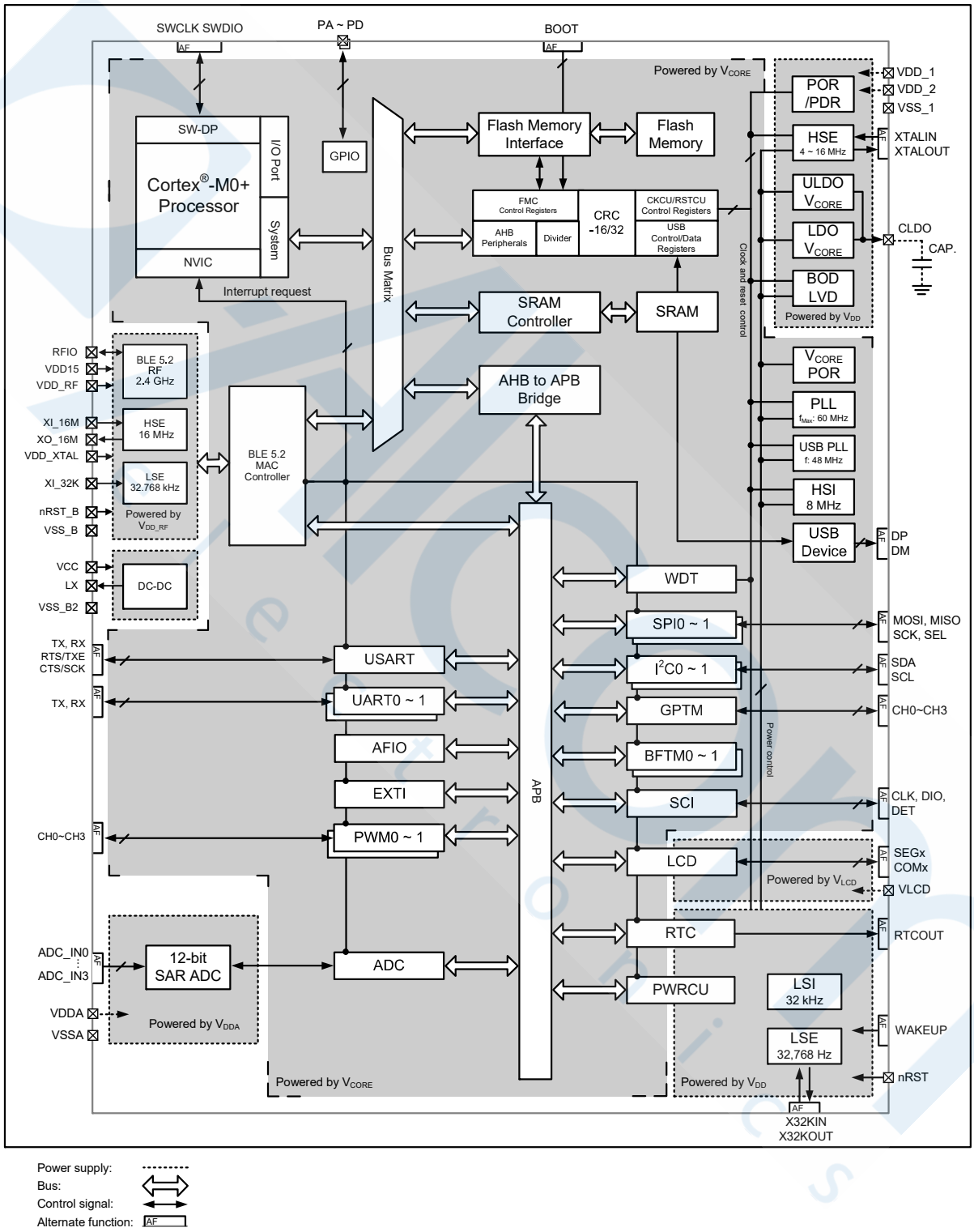


Figure 1. Block Diagram

Memory Map

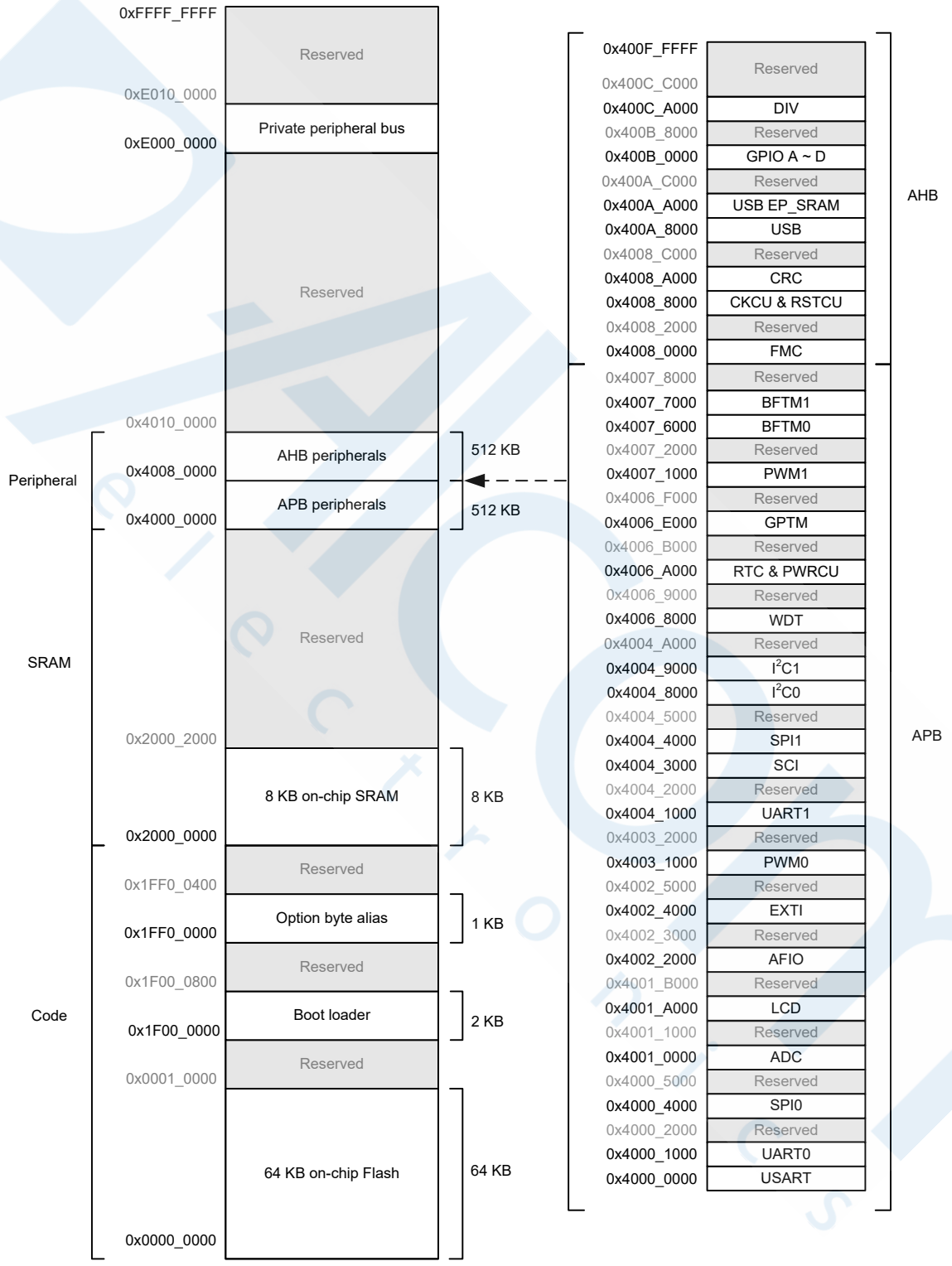


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_9FFF	Reserved	
0x4001_A000	0x4001_AFFF	LCD	
0x4001_B000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	
0x4007_2000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB	
0x400A_A000	0x400A_BFFF	USB EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

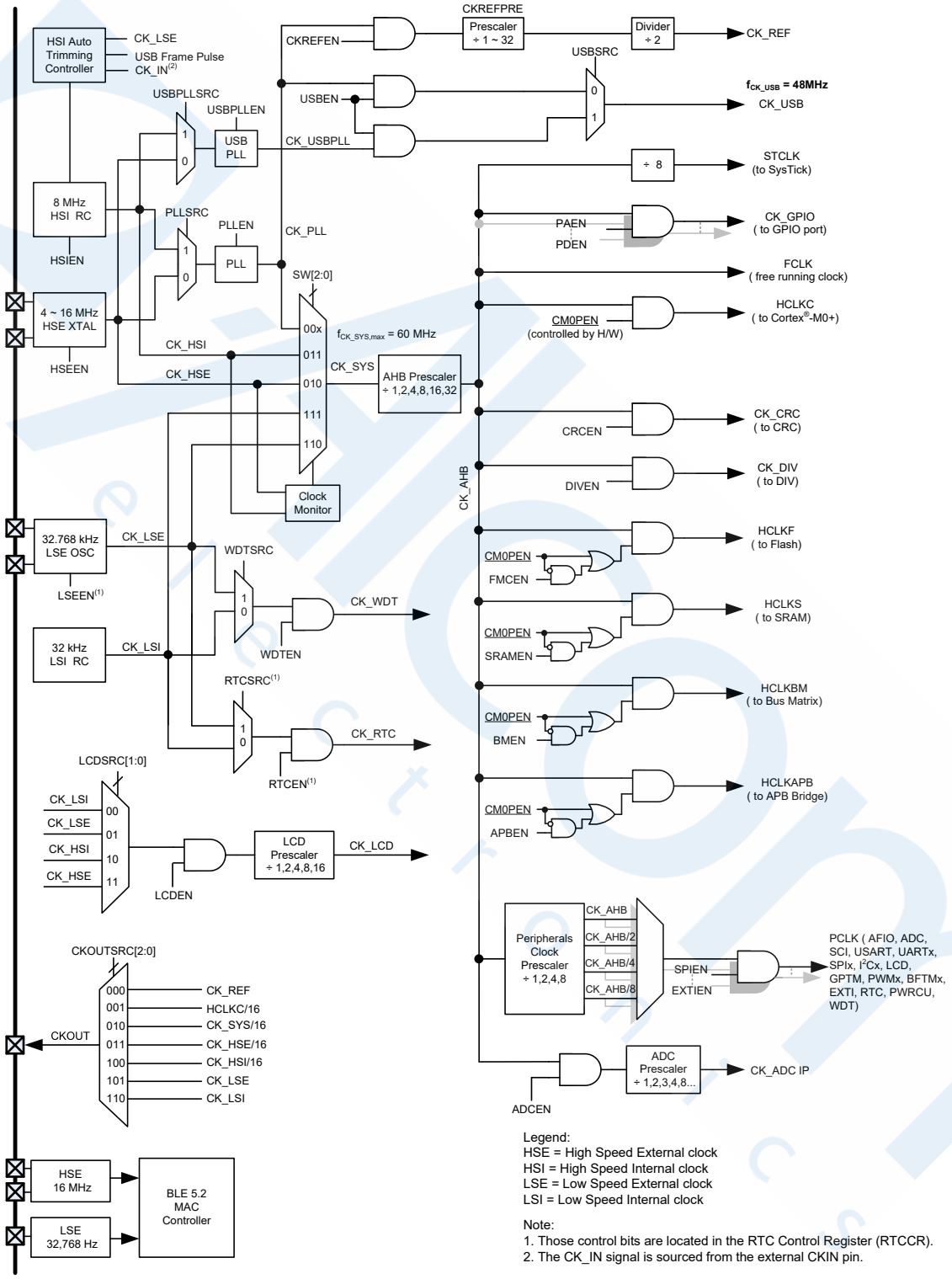


Figure 3. Clock Structure

4 Pin Assignment

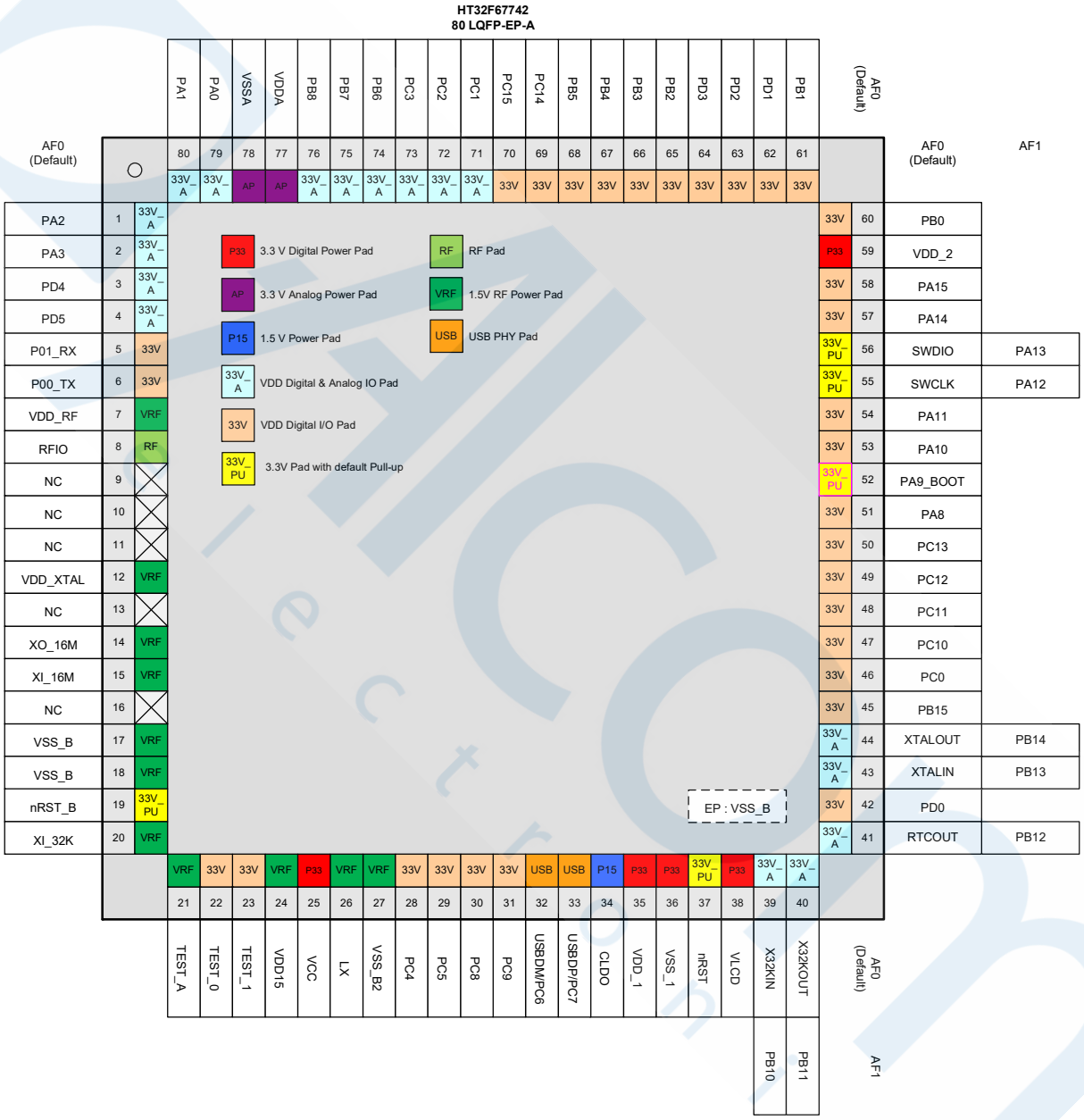


Figure 4. 80-pin LQFP-EP Pin Assignment

Table 3. Pin Assignment

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP-EP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	SCI	N/A	N/A	N/A	N/A	PWM	LCD	System Other
79	PA0	—	ADC_IN0	—	GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL	SCI_CLK	—	—	—	—	—	—	VREF
80	PA1	—	ADC_IN1	—	GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA	SCI_DIO	—	—	—	—	—	—	—
1	PA2	—	ADC_IN2	—	GT_CH2	SPI1_MISO	USR_TX	—	—	—	—	—	—	—	—	—
2	PA3	—	ADC_IN3	—	GT_CH3	SPI1_SEL	USR_RX	—	—	—	—	—	—	—	—	—
3	PD4	—		—	—	—	UR1_TX	—	—	—	—	—	—		—	—
4	PD5	—		—	—	—	UR1_RX	—	—	—	—	—	—		—	—
5	P01_RX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P00_TX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	VDD_RF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	RFIO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	VDD_XTAL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	XO_16M	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	XI_16M	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
17	VSS_B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
18	VSS_B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
19	nRST_B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
20	XI_32K	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
21	TEST_A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
22	TEST_0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
23	TEST_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
24	VDD15	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
25	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
26	LX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
27	VSS_B2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
28	PC4	—	—	—	GT_CH0	SPI1_SEL	USR_TX	I2C1_SCL	—	—	—	—	—	—	SEG11	—
29	PC5	—	—	—	GT_CH1	SPI1_SCK	USR_RX	I2C1_SDA	—	—	—	—	—	—	SEG12	—
30	PC8	—	—	—	GT_CH2	SPI1_MOSI	UR1_TX	—	—	—	—	—	—	—	SEG13	—
31	PC9	—	—	—	GT_CH3	SPI1_MISO	UR1_RX	—	—	—	—	—	—	—	SEG14	—
32	PC6	—	—	—	—	—	UR0_TX	I2C0_SCL	—	—	—	—	—	—	—	—
32	USBDM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
33	USBDP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
33	PC7	—	—	—	—	—	UR0_RX	I2C0_SDA	—	—	—	—	—	—	—	—
34	CLDO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
35	VDD_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
36	VSS_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
37	nRST	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
38	VLCD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
39	X32KIN	PB10	—	—	—	—	USR_TX	—	—	—	—	—	—	—	—	—
40	X32KOUT	PB11	—	—	—	—	USR_RX	—	—	—	—	—	—	—	—	—

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP-EP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	SCI	N/A	N/A	N/A	N/A	PWM	LCD	System Other
41	RTCOUT	PB12														WAKEUP
42	PD0	—	—	—	—	—	—	I2C0_ SDA	—	—	—	—	—	—	SEG15	—
43	XTALIN	PB13	—	—	—	—	—	—	—	—	—	—	—	—	—	—
44	XTALOUT	PB14	—	—	—	—	—	—	—	—	—	—	—	—	—	—
45	PB15	—	—	—	—	SPI0_ SEL	USR_ TX	I2C1_ SCL	—	—	—	—	—	PWM0_ CH2	COM0	—
46	PC0	—	—	—	—	SPI0_ SCK	USR_ RX	I2C1_ SDA	—	—	—	—	—	PWM0_ CH3	COM1	—
47	PC10	—	—	—	GT_ CH0	SPI1_ SEL	—	—	—	—	—	—	—	—	SEG25/ COM4	—
48	PC11	—	—	—	GT_ CH1	SPI1_ SCK	—	—	—	—	—	—	—	—	SEG26/ COM5	—
49	PC12	—	—	—	GT_ CH2	SPI1_ MOSI	UR1_ TX	I2C0_ SCL	—	—	—	—	—	—	SEG27/ COM6	—
50	PC13	—	—	—	GT_ CH3	SPI1_ MISO	UR1_ RX	I2C0_ SDA	—	—	—	—	—	—	SEG28/ COM7	—
51	PA8	—	—	—	—	—	USR_ TX	—	—	—	—	—	—	PWM1_ CH3	COM2	—
52	PA9_ BOOT	—	—	—	—	SPI0_ MOSI	—	—	—	—	—	—	—	PWM1_ CH2	—	CKOUT
53	PA10	—	—	—	—	—	USR_ RX	—	SCI_ DET	—	—	—	—	PWM0_ CH1	COM3	—
54	PA11	—	—	—	—	SPI0_ MISO	—	—	—	—	—	—	—	—	SEG0	—
55	SWCLK	PA12	—	—	—	—	—	—	—	—	—	—	—	—	—	—
56	SWDIO	PA13	—	—	—	—	—	—	—	—	—	—	—	—	—	—
57	PA14	—	—	—	—	SPI1_ SEL	USR_ RTS	I2C1_ SCL	SCI_ CLK	—	—	—	—	PWM0_ CH0	SEG1	—
58	PA15	—	—	—	—	SPI1_ SCK	USR_ CTS	I2C1_ SDA	SCI_ DIO	—	—	—	—	—	SEG2	—
59	VDD_2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
60	PB0	—	—	—	—	SPI1_ MOSI	USR_ TX	I2C0_ SCL	—	—	—	—	—	PWM0_ CH1	SEG3	—
61	PB1	—	—	—	—	SPI1_ MISO	USR_ RX	I2C0_ SDA	—	—	—	—	—	PWM1_ CH1	SEG4	—
62	PD1	—	—	—	—	—	USR_ RTS	—	SCI_ CLK	—	—	—	—	—	SEG16	—
63	PD2	—	—	—	—	—	USR_ CTS	—	SCI_ DIO	—	—	—	—	—	SEG17	—
64	PD3	—	—	—	—	—	—	—	SCI_ DET	—	—	—	—	—	SEG18	—
65	PB2	—	—	—	—	SPI0_ SEL	UR0_ TX	—	—	—	—	—	—	PWM0_ CH2	SEG5	CKIN
66	PB3	—	—	—	—	SPI0_ SCK	UR0_ RX	—	—	—	—	—	—	—	SEG6	—
67	PB4	—	—	—	—	SPI0_ MOSI	UR1_ TX	—	—	—	—	—	—	—	SEG7	—
68	PB5	—	—	—	—	SPI0_ MISO	UR1_ RX	—	—	—	—	—	—	—	SEG8	—
69	PC14	—	—	—	—	—	—	I2C0_ SCL	—	—	—	—	—	—	SEG9	—
70	PC15	—	—	—	—	—	—	I2C0_ SDA	—	—	—	—	—	—	SEG10	—
71	PC1	—	—	—	—	SPI1_ SEL	UR1_ TX	—	—	—	—	—	—	PWM0_ CH0	SEG19	—
72	PC2	—	—	—	—	SPI1_ SCK	—	—	—	—	—	—	—	PWM1_ CH0	SEG20	—
73	PC3	—	—	—	—	SPI1_ MOSI	UR1_ RX	—	—	—	—	—	—	PWM1_ CH2	SEG21	—

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
80 LQFP-EP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	SCI	N/A	N/A	N/A	N/A	PWM	LCD	System Other
74	PB6	—	—	—	—	SPI1_ MISO	UR0_ TX	—	SCI_ CLK	—	—	—	—	—	SEG22	—
75	PB7	—	—	—	—	—	—	I2C1_ SCL	SCI_ DET	—	—	—	—	PWM0_ CH3	SEG23	—
76	PB8	—	—	—	—	—	UR0_ RX	I2C1_ SDA	SCI_ DIO	—	—	—	—	PWM1_ CH3	SEG24	—
77	VDDA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
78	VSSA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9~11, 13,16	NC															

Table 4. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
80 LQFP-EP					Default Function (AF0)
79	PA0	AI/O	33V	4/8/12/16 mA	PA0
80	PA1	AI/O	33V	4/8/12/16 mA	PA1
1	PA2	AI/O	33V	4/8/12/16 mA	PA2
2	PA3	AI/O	33V	4/8/12/16 mA	PA3
3	PD4	AI/O	33V	4/8/12/16 mA	PD4
4	PD5	AI/O	33V	4/8/12/16 mA	PD5
5	P01_RX	I/O	33V	—	P01_RX
6	P00_TX	I/O	33V	—	P00_TX
7	VDD_RF	P	15V	—	RF power
8	RFIO	AI/O	15V	—	RF I/O
12	VDD_XTAL	P	15V	—	BLE 16 MHz Crystal oscillator power
14	XO_16M	AO	15V	—	BLE 16 MHz Crystal oscillator output
15	XI_16M	AI	15V	—	BLE 16 MHz Crystal oscillator input
17	VSS_B	P	—	—	RF power ground
18	VSS_B	P	—	—	RF power ground
19	nRST_B	I	33V_PU	—	BLE hardware reset
20	XI_32K	AI	—	—	BLE 32.768 kHz Crystal oscillator
21	TEST_A	O	—	—	Test pin
22	TEST_0	I	—	—	Test pin
23	TEST_1	I	—	—	Test pin
24	VDD15	P	—	—	BLE internal power
25	VCC	P	—	—	BLE digital power
26	LX	AO	15V	—	RF DC-DC switching output
27	VSS_B2	P	—	—	BLE ground reference for digital I/O
28	PC4	I/O	33V	4/8/12/16 mA	PC4
29	PC5	I/O	33V	4/8/12/16 mA	PC5
30	PC8	I/O	33V	4/8/12/16 mA	PC8
31	PC9	I/O	33V	4/8/12/16 mA	PC9

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
80 LQFP-EP					Default Function (AF0)
32	PC6	I/O	33V	4/8/12/16 mA	PC6
32	USBDM(4)	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
33	USBDP(4)	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
33	PC7	I/O	33V	4/8/12/16 mA	PC7
34	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1
35	VDD_1	P	—	—	Voltage for digital I/O
36	VSS_1	P	—	—	Ground reference for digital I/O
37	nRST	I	33V_PU	—	External reset pin and external wake-up pin in the Power-Down mode
38	VLCD	P	—	—	Voltage for LCD power supply It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1 for LCD supply power with internal charge pump mode, or connected a general bypass capacitor for external LCD supply power
39	PB10	AI/O	33V	4/8/12/16 mA	X32KIN
40	PB11	AI/O	33V	4/8/12/16 mA	X32KOUT
41	PB12	AI/O	33V	4/8/12/16 mA	RTCOUT
42	PD0	I/O	33V	4/8/12/16 mA	PD0
43	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
44	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
45	PB15	I/O	33V	4/8/12/16 mA	PB15
46	PC0	I/O	33V	4/8/12/16 mA	PC0
47	PC10	I/O	33V	4/8/12/16 mA	PC10
48	PC11	I/O	33V	4/8/12/16 mA	PC11
49	PC12	I/O	33V	4/8/12/16 mA	PC12
50	PC13	I/O	33V	4/8/12/16 mA	PC13
51	PA8	I/O	33V	4/8/12/16 mA	PA8
52	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
53	PA10	I/O	33V	4/8/12/16 mA	PA10
54	PA11	I/O	33V	4/8/12/16 mA	PA11
55	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
56	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
57	PA14	I/O	33V	4/8/12/16 mA	PA14
58	PA15	I/O	33V	4/8/12/16 mA	PA15
59	VDD_2	P	—	—	Voltage for digital I/O
60	PB0	I/O	33V	4/8/12/16 mA	PB0
61	PB1	I/O	33V	4/8/12/16 mA	PB1
62	PD1	I/O	33V	4/8/12/16 mA	PD1

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
80 LQFP-EP					Default Function (AF0)
63	PD2	I/O	33V	4/8/12/16 mA	PD2
64	PD3	I/O	33V	4/8/12/16 mA	PD3
65	PB2	I/O	33V	4/8/12/16 mA	PB2
66	PB3	I/O	33V	4/8/12/16 mA	PB3
67	PB4	I/O	33V	4/8/12/16 mA	PB4
68	PB5	I/O	33V	4/8/12/16 mA	PB5
69	PC14	I/O	33V	4/8/12/16 mA	PC14
70	PC15	I/O	33V	4/8/12/16 mA	PC15
71	PC1	AI/O	33V	4/8/12/16 mA	PC1
72	PC2	AI/O	33V	4/8/12/16 mA	PC2
73	PC3	AI/O	33V	4/8/12/16 mA	PC3
74	PB6	AI/O	33V	4/8/12/16 mA	PB6
75	PB7	AI/O	33V	4/8/12/16 mA	PB7
76	PB8	AI/O	33V	4/8/12/16 mA	PB8
77	VDDA	P	—	—	Analog voltage for ADC
78	VSSA	P	—	—	Ground reference for ADC
9~11, 13, 16	NC	—	—	—	No connected

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply.
2. 33V = 3.3 V tolerant, PU = Pull-up, 15V = 1.5 V.
3. The EP means the exposed pad on the packages. It must be connected to ground.
4. In the Boot loader mode, only the USB interface can be used for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{LCD}	LCD Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	BLE OFF	1.65	3.3	3.6	V
		BLE ON	2.0			
V_{DDA}	Analog Operating Voltage	—	Note	3.3	3.6	V
V_{LCD}	LCD Operating Voltage	—	2.2	3.3	3.6	V

Note: The minimum electrical characteristics are shown in other tables below.

BLE Characteristics

Table 7. BLE Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Crystal Oscillator 16 MHz					
	Frequency	—	16	—	MHz
	Frequency Accuracy Requirement	-30	—	30	ppm
ESR	Equivalent Series Resistance	—	—	80	Ω
C0	Crystal Shunt Capacitance	—	—	3	pF
CL	Crystal Load Capacitance	—	7	—	pF
Crystal Oscillator 32.768 kHz					
	Frequency	—	32.768	—	kHz
	Frequency Accuracy Requirement	-20	—	20	ppm

Symbol	Parameter		Min.	Typ.	Max.	Unit
ESR	Equivalent Series Resistance		—	—	70k	Ω
C0	Crystal Shunt Capacitance		—	—	2	pF
CL	Crystal Load Capacitance		—	12.5	—	pF
RX Characteristics						
PSENS	Sensitivity @ 1 Mbps		—	-94	—	dBm
	Sensitivity @ 2 Mbps		—	-91	—	dBm
CI0	In-band Blocking	Co-channel Interference	—	7	—	dB
CI1		Interference at f_{OFFS} = ±1 MHz	-9	—	-6	dB
CI2		Interference at f_{OFFS} = ±2 MHz	—	-44	—	dB
CI3		Interference at f_{OFFS} = ±3 MHz	—	-50	—	dB
CI4		Interference at f_{IMAGE}	—	-25	—	dB
CI5		Interference at fIMAGE +/- 1 MHz	—	-35	—	dB
Intermodulation	P_{in} = -64 dBm; P_{unwant} = -50 dBm; f0 = 2 × f1 - f2, f2 - f1 = 3 MHz or 4 MHz or 5 MHz		-25	—	-22	dBm
TX Characteristics						
PTX	Output Power		—	3.5	—	dBm
PBW	Modulation 20 dB Bandwidth		—	—	1	MHz
PRF1	Out of Band Emission 2 MHz		—	-20	—	dB
PRF2	Out of Band Emission 3 MHz		—	-58	—	dB
Dev	Transmit FM Deviation		115	250	300	kHz
Drift	Transmit Drift in Any Position		—	—	400	Hz/μs

On-Chip LDO Voltage Regulator Characteristics

Table 8. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 10 mA and voltage variant = ± 5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
		V_{DD} = 1.65 V ~ 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	20	25	
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 9. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{ULDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 10. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Run Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz	All peripherals enabled	14.9	17.0	—	mA
				All peripherals disabled	6.9	7.9	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz	All peripherals enabled	11.9	13.6	—	
				All peripherals disabled	6.5	7.4	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz	All peripherals enabled	6.2	7.1	—	
				All peripherals disabled	3.2	3.6	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	3.2	3.6	—	
				All peripherals disabled	1.4	1.6	—	
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	13.2	17.5	—	μA
				All peripherals disabled	9.2	12.2	—	
	Sleep Mode	60 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, MCU core sleep	All peripherals enabled	10.3	11.8	—	mA
				All peripherals disabled	1.5	1.7	—	
		40 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, MCU core sleep	All peripherals enabled	7.1	8.1	—	
				All peripherals disabled	1.2	1.3	—	
		20 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, MCU core sleep	All peripherals enabled	4.2	4.8	—	
				All peripherals disabled	0.9	1.0	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, MCU core sleep	All peripherals enabled	2.4	2.7	—	
				All peripherals disabled	0.4	0.5	—	
	Deep-Sleep1 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		5.0	7.6	—	μA
	Deep-Sleep2 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		5.0	7.6	—	μA
			V_{DD} = V_{LCD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on, LCD ON(5), external V_{LCD} = V_{DD}		7.5	—	—	
			V_{DD} = 2.7 V, V_{LCD} = 3.25 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC off, LCD on(6), internal V_{LCD} pump		55.3	—	—	

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A		Unit
					25 °C	85 °C	
I_{DD}	Power-Down Mode	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on	1.40	2.15	—	μA
			V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off	1.30	1.95	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.
6. LCD enabled with internal V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

Reset and Supply Monitor Characteristics

Table 11. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.4	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 12. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	ms

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{DDLVD}	Operation Current (2)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 13. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0 V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1	—	—	160	Ω
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 14. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 1.65 V ~ 2.7 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L <$ 7 pF, V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.
1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.

2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	1.65	—	3.6	V
f_{CK_HSI}	HSI Frequency	V_{DD} = 3.3 V	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -20 °C ~ 60 °C	-2.5	—	2.5	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{CK_HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{CK_HSI} = 8 MHz	—	300	500	μA
	HSI Oscillator Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{CK_HSI} = 8 MHz	—	—	10	μs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V	—	—	100	μs

System PLL Characteristics

Table 17. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

USB PLL Characteristics

Table 18. USB PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	USB PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	USB PLL Output Clock	—	64	—	96	MHz
t_{LOCK}	USB PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 19. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 20. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	3.3 V I/O		-0.4	—	V_{DD} × 0.35	V
		Reset pin		-0.4	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.4	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.4	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V		16	—	—	
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ
C_{IO}	I/O Pin Capacitance	—	—	4.2	—	pF

ADC Characteristics

Table 21. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	A/D Converter Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

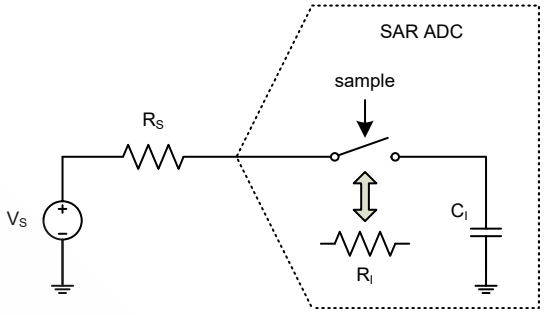


Figure 5. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 22. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		1.65	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 °C Temperature	V_{DDA} ≥ 1.65 V	VREFSEL[1:0] = 00	1.190	1.215	1.240	V
		V_{DDA} ≥ 2.30 V	VREFSEL[1:0] = 01	1.96	2.00	2.04	
		V_{DDA} ≥ 2.80 V	VREFSEL[1:0] = 10	2.45	2.50	2.55	
		V_{DDA} ≥ 3.00 V	VREFSEL[1:0] = 11	2.65	2.70	2.75	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 1.65 V ~ 3.6 V, V_{REF} = 1.215 V, T_A = -40 °C ~ 85 °C		-3.0	—	+3.0	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	45	55	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

V_{DDA} Monitor Characteristics

Table 23. V_{DDA} Monitor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R	Resistor Bridge for V_{DDA}	—	—	50	—	kΩ
Q	Ratio on V_{DDA} Measurement	—	—	2	—	—
E_R	Error on Ratio	—	-1	—	+1	%
t_{SVDDA}	ADC Sampling Time when Reading the V_{DDA}	—	5	—	—	μs

Note: Data based on characterization results only, not tested in production.

GPTM / PWM Characteristics

Table 24. GPTM / PWM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM and PWM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I^2C Characteristics

Table 25. I^2C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I^2C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 01.

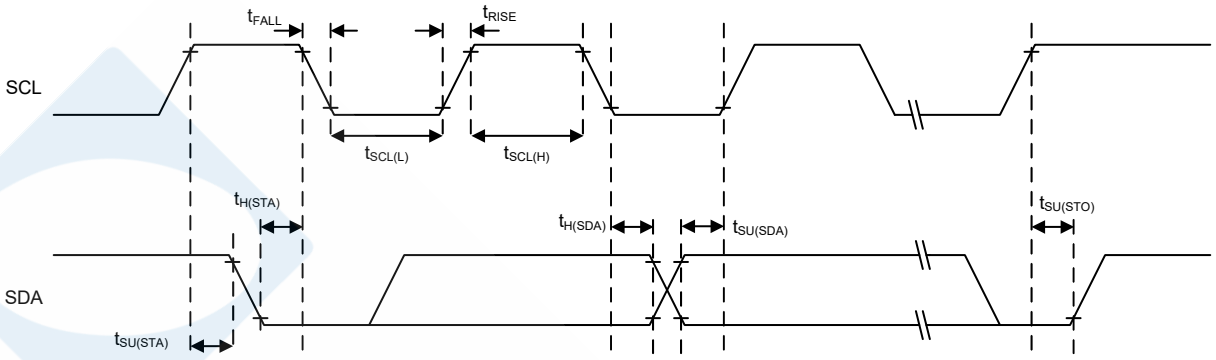


Figure 6. I²C Timing Diagram

SPI Characteristics

Table 26. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

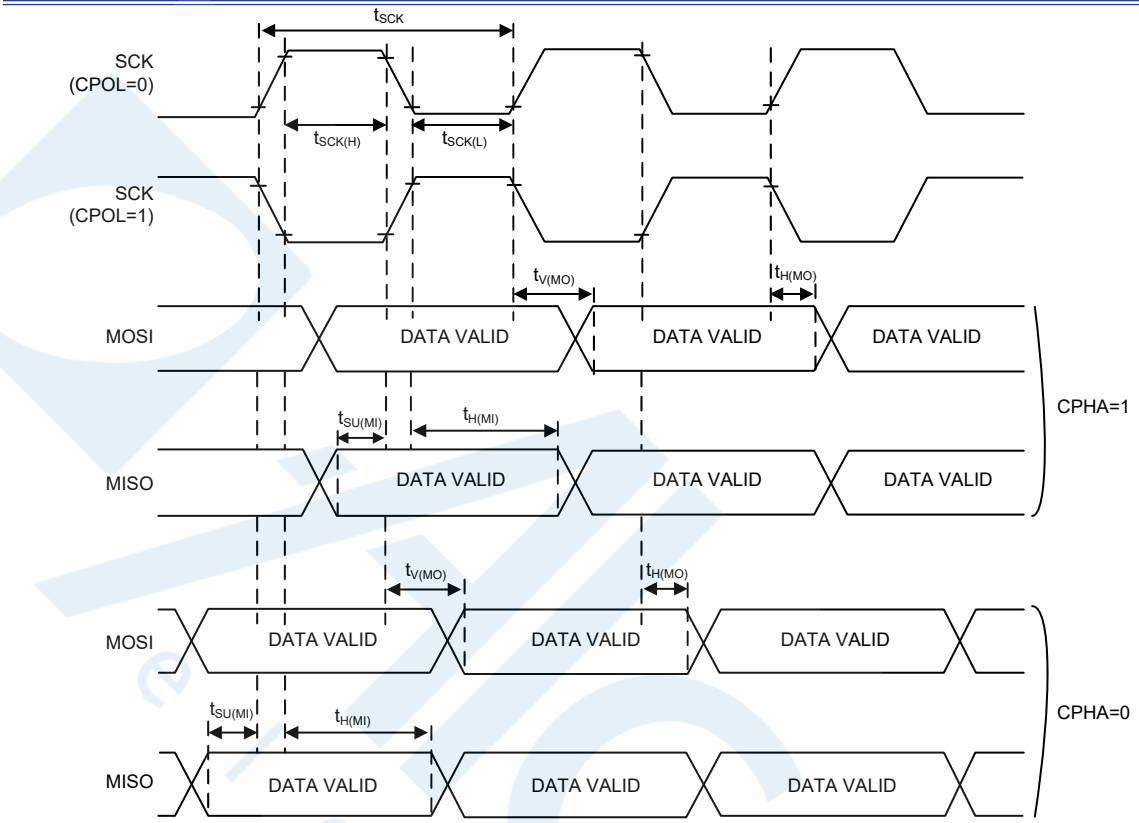


Figure 7. SPI Timing Diagram – SPI Master Mode

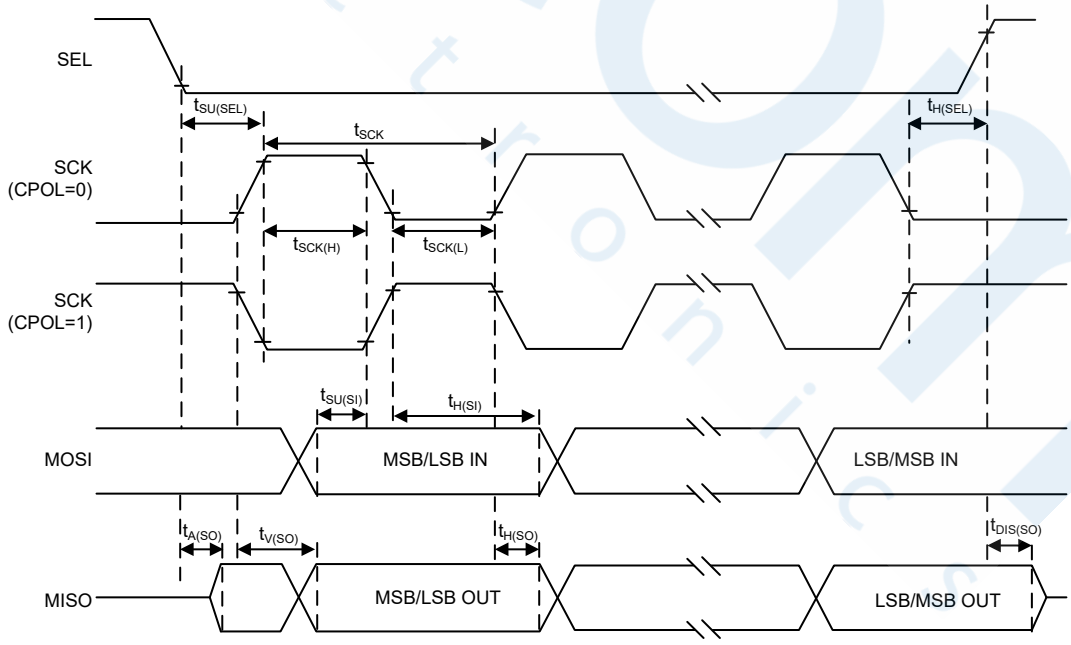


Figure 8. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

LCD Characteristics

Table 27. LCD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LCD}	LCD External Voltage	—	—	—	3.6	V
	LCD Internal Charge Pump Voltage	CPVS = 000	—	2.65	—	V
		CPVS = 001	—	2.75	—	V
		CPVS = 010	—	2.85	—	V
		CPVS = 011	—	2.95	—	V
		CPVS = 100	—	3.1	—	V
		CPVS = 101	—	3.25	—	V
		CPVS = 110	—	3.4	—	V
		CPVS = 111	—	3.55	3.6	V
C_{LCD}	V_{LCD} External Capacitor	—	0.22	—	2.2	μF
I_{LCD}	Supply Current @ V_{DD} = 3.3 V	External V_{LCD}(1)	—	2.4	—	μA
	Supply Current @ V_{DD} = 2.7 V	Internal charge pump(2)	—	50	—	
R_H	Internal Low Drive Resister Network Overall Value	—	—	3	—	MΩ
R_L	Internal High Drive Resister Network Overall Value	—	—	120	—	kΩ
V_{44}	Segment/Common Highest Level Voltage	—	—	—	V_{LCD}	V
V_{34}	Segment/Common 3/4 Level Voltage	—	—	3/4 V_{LCD}	—	V
V_{23}	Segment/Common 2/3 Level Voltage	—	—	2/3 V_{LCD}	—	V
V_{12}	Segment/Common 1/2 Level Voltage	—	—	1/2 V_{LCD}	—	V
V_{13}	Segment/Common 1/3 Level Voltage	—	—	1/3 V_{LCD}	—	V
V_{14}	Segment/Common 1/4 Level Voltage	—	—	1/4 V_{LCD}	—	V
V_0	Segment/Common Lowest Level Voltage	—	0	—	—	V

Note: 1. LCD enabled with external V_{LCD} = V_{DD} = 3.3 V, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

2. LCD enabled with internal charge pump V_{LCD} = 3.25 V, V_{DD} = 2.7 V, 1/4 duty, 1/3 bias, division ratio = 64, high drive disabled, all pixels active, no LCD connected.

3. Data based on characterization results only, not tested in production.

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 28. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	1.5 kΩ R_L to V_{DD33}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.

2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the V_{DD} voltage range of 2.7 to 3.0 V.

3. R_L is the resistor load connected to the USB driver USBDP.

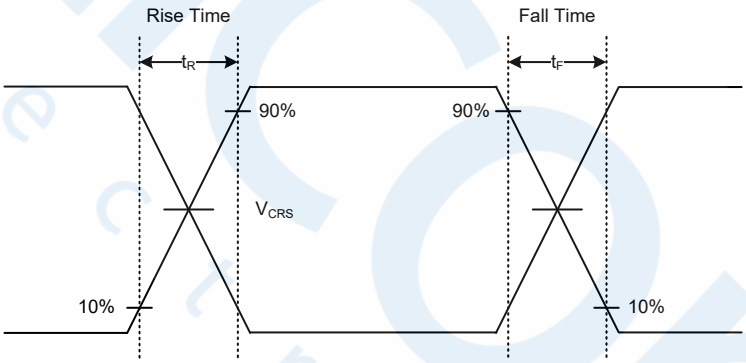


Figure 9. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 29. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Time	C_L = 50 pF	4	—	20	ns
t_F	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{R/F}$	Rise Time / Fall Time Matching	$t_{R/F} = t_R / t_F$	90	—	110	%

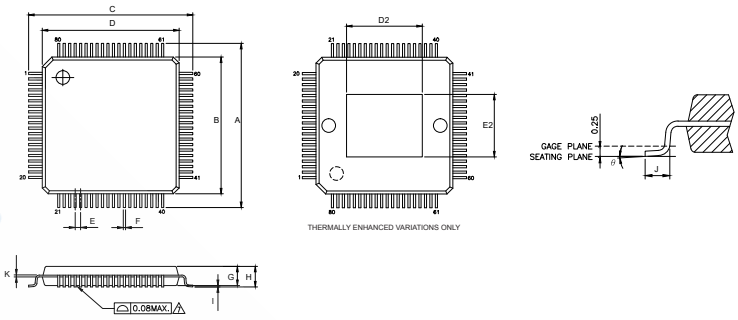
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

80-pin LQFP-EP (10 mm × 10 mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.472 BSC	
B		0.394 BSC	
C		0.472 BSC	
D		0.394 BSC	
E		0.016 BSC	
D2	0.185	—	0.224
E2	0.153	—	0.186
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		12.00 BSC	
B		10.00 BSC	
C		12.00 BSC	
D		10.00 BSC	
E		0.40 BSC	
D2	4.71	—	5.69
E2	3.88	—	4.72
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°