HT32F67041/HT32F67051
Datasheet

32-Bit Arm® Cortex®-M0+ 2.4GHz RF Transceiver Microcontroller, up to 128 KB Flash and 8 KB SRAM with 1 Msps ADC, DIV, UART, SPI, I²C, GPTM, SCTM, BFTM, CRC, RTC, WDT, PDMA and AES-128

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1 General Description

The Holtek HT32F67041/67051 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as PDMA, AES-128, Hardware Divider DIV, SPI, UART, I^2C, GPTM, SCTM, BFTM, CRC-16/32, RTC, WDT, ADC, 2.4GHz RF Transceiver and SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The fully integrated 2.4GHz RF transceiver is a high performance RF GFSK transceiver and is operated in the worldwide frequency band at 2.4 GHz for Industrial, Scientific, and Medical applications. The frequency band is programmable at 2.402~2.480 GHz and incorporates a baseband modem with programmable data rates of 125 Kbps and 250 Kbps. The output transmitting power can be up to +6 dBm (Max.).

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as wireless keyboards/mice, wireless microphones, smart toys, baby monitors, smart-home peripherals and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option byte storage
- 8 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the series devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Control Unit – PWRCU

- V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{DD} and V_{CORE} power domains
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 10 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in these devices. There are multiplexed channels, which include up to 10 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D Conversion can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (V_{REF}) which can provide a stable reference voltage for the A/D Converter is internally connected to the ADC input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 29 GPIOs
- Port A, B are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 29 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer, SCTM, consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control features
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counter when compare match occurs

The Basic Function Timer, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

2.4GHz RF Transceiver

- Frequency band: 2402 ~ 2480 MHz
- GFSK modulation
- Programmable TX output power up to 5 dBm (Max. +6 dBm)
- Programmable data rate: 125 / 250 Kbps
- TX current consumption: < 20 mA @ 5 dBm
- RX current consumption: < 17 mA @ 250 Kbps
- RX sensitivity: -96 dBm @ 250 Kbps on-air data rate
- Dual sleep modes
  - Deep Sleep mode
  - Light Sleep mode
- Packet Handing
  - Data Whitening
  - Auto-ACK/Resend
  - CRC optional protocol
  - Support burst packets
  - Suport automatic ACK transaction
  - Six data-pipes for 1:6 star network
- Interrupt generation capability with wakeup from Sleep, Deep-Sleep1 mode through the EXTI controller
- FCC/ETSI Compliant

The 2.4GHz RF Transceiver is a high performance RF GFSK transceiver for wireless applications in 2.4GHz frequency bands. It incorporates a highly integrated 2.4 GHz transceiver and a baseband modem with programmable data rates of 125 Kbps and 250 Kbps. Data handing features include 3 levels of 32-byte TX / RX FIFO and packet handing such as whitening and CRC checking.

The 2.4GHz RF transceiver supports a middle sleep mode for a fast XO start-up with 30 μA bleeding current. At 2.4 GHz, the transceiver can achieve -96 dBm sensitivity at 250 Kbps and can deliver +5 dBm TX output power at 20 mA current consumption. A fully integrated Fractional-N synthesizer can support a wide frequency range with a fine resolution.

Additional link layer features like RSSI for channel assessment, auto-acknowledgement, auto-resend and 6 pipes star network topology, facilitate microcontroller based ISM bands wireless link applications.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provide reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes an APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, i.e., when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the MCU power saving modes.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module

provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size

- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:
  ADC, SPI, UART, I^2C, GPTM, AES-128 and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by using the control register “START” bit. After 8 clock cycles, the divider calculate complete flag will be set to 1, and if the divisor register data is zero, the division by zero error flag will be set to 1.

Advanced Encryption Standard – AES-128

- Supports AES Encrypt / Decrypt functions
- Supports AES ECB/CBC/CTR modes
- Supports Key Size of 128 bits
- Supports 4 words Initial Vector for CBC and CTR modes
- 4 × 32 bits AES data buffer
- Supports PDMA interface
- Supports Word Data Swap function

The AES core supports both encryption and decryption functions and supports 128-bit input data. It should be noted that hardware does not pad out any input data bits, therefore users need to do pad action by software at first.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 32-pin QFN package for HT32F67041
- 46-pin QFN package for HT32F67051
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F67041	HT32F67051
Main Flash (KB)		64	127
Option Bytes Flash (KB)		1	1
SRAM (KB)		8	8
Timers	GPTM	1	
	SCTM	4	
	BFTM	2	
	WDT	1	
	RTC	1	
Communication	SPI	2	
	UART	2	
	I²C	2	
PDMA		6 channels	
Hardware Divider		1	
CRC-16/32		1	
AES-128		1	
12-bit ADC Number of channels		1 10 external channels	
GPIO		16	Up to 29
CPU frequency		Up to 60 MHz	
RF frequency band		2402 MHz ~ 2480 MHz	
RF data rate		125Kbps / 250Kbps	
TX output power		Max. 6dBm	
Operating voltage		2.2 V ~ 3.6 V	
Package		32-pin QFN	46-pin QFN

Block Diagram

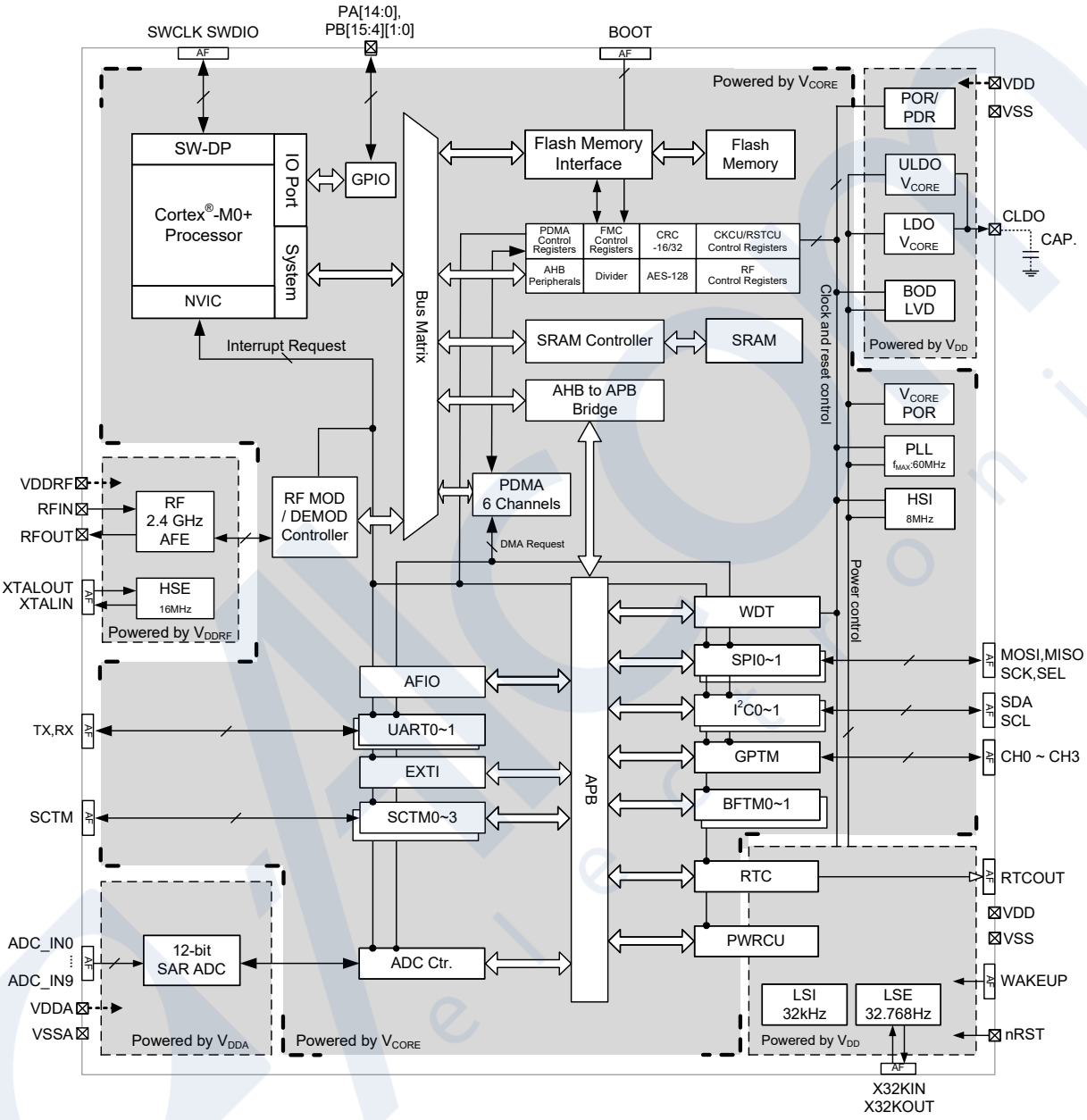


Figure 1. Block Diagram

Memory Map

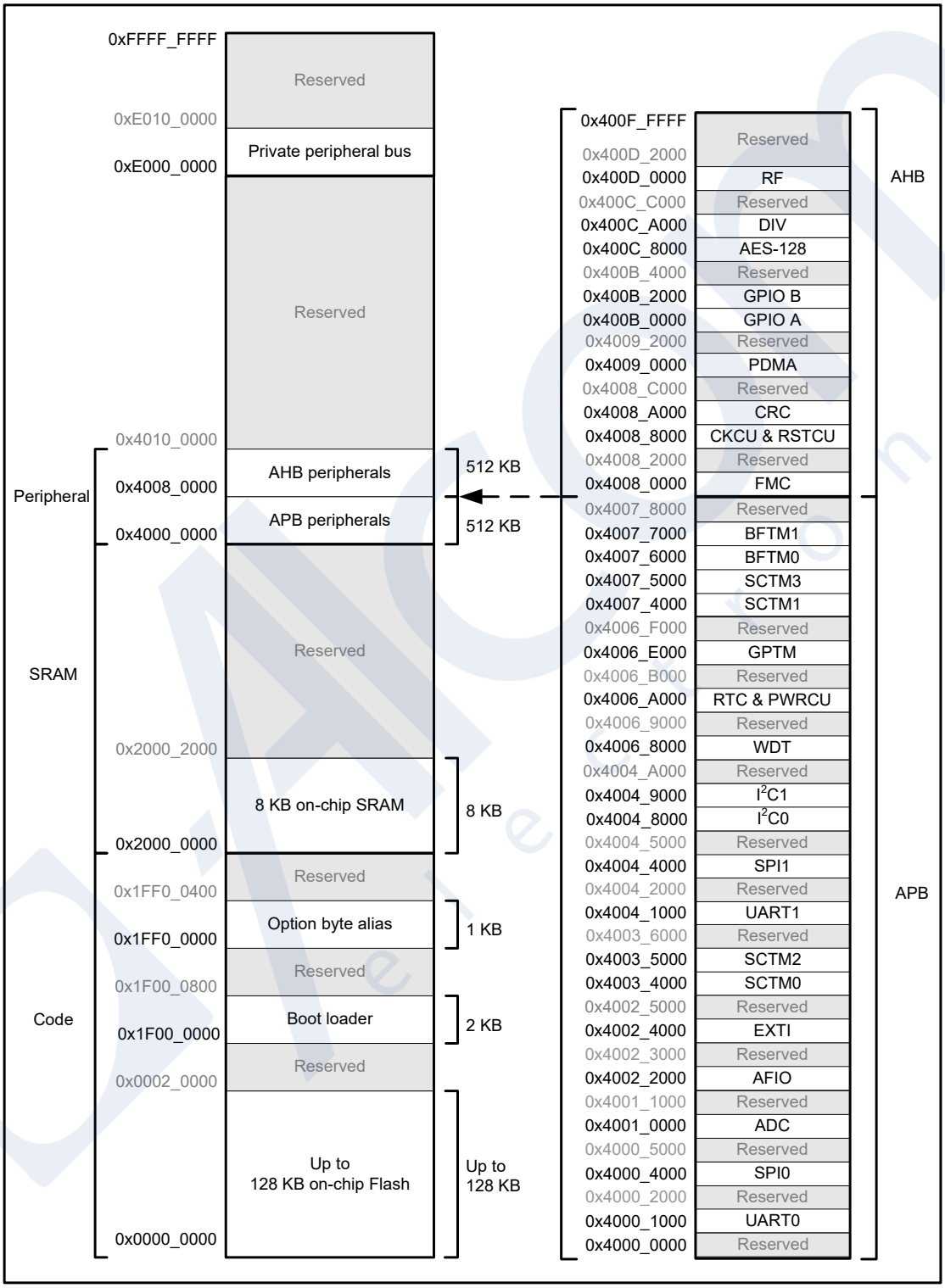


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400C_7FFF	Reserved	
0x400C_8000	0x400C_9FFF	AES-128	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400C_FFFF	Reserved	
0x400D_0000	0x400D_1FFF	RF	
0x400D_2000	0x400F_FFFF	Reserved	

Clock Structure

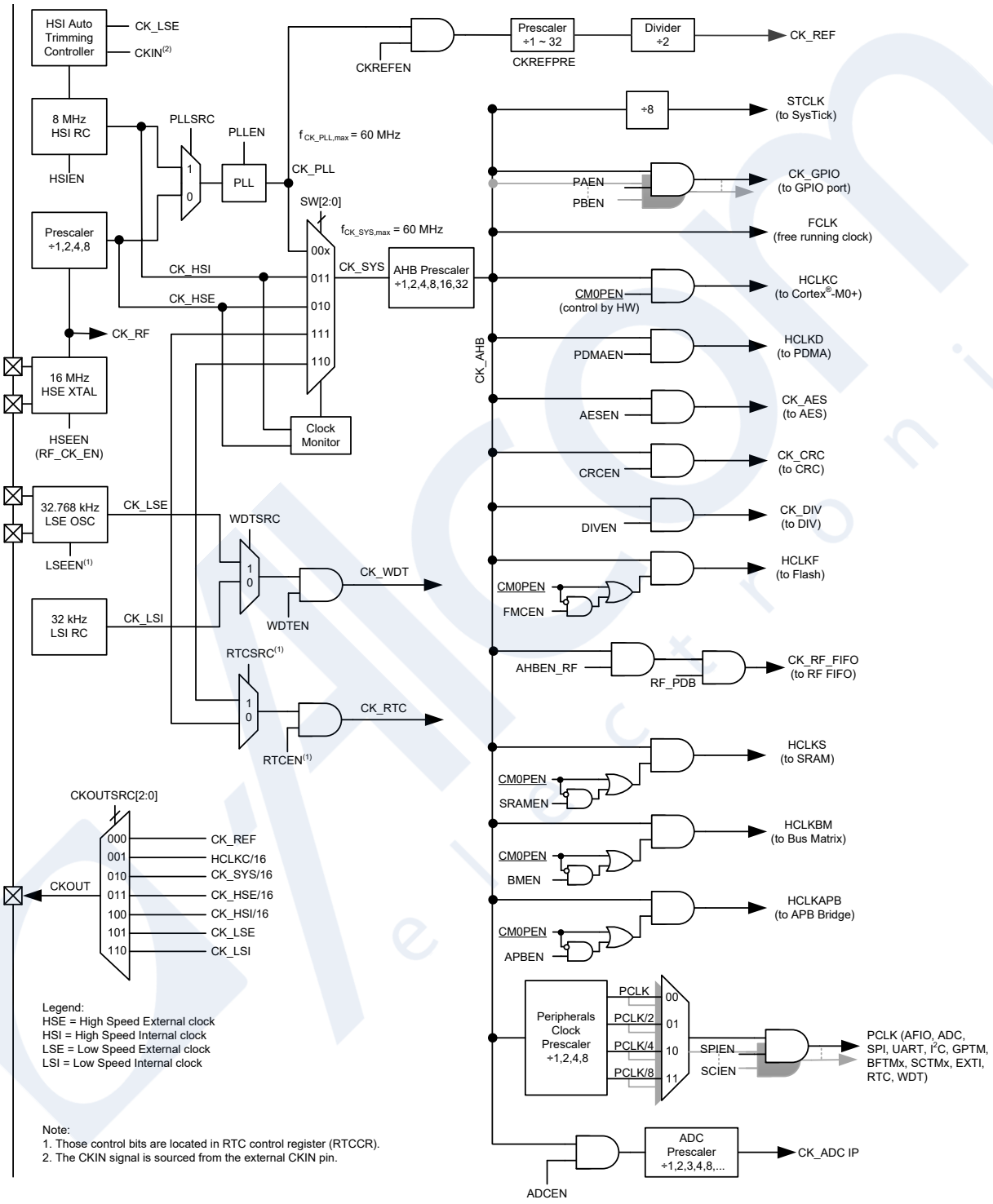


Figure 3. Clock Structure

4 Pin Assignment

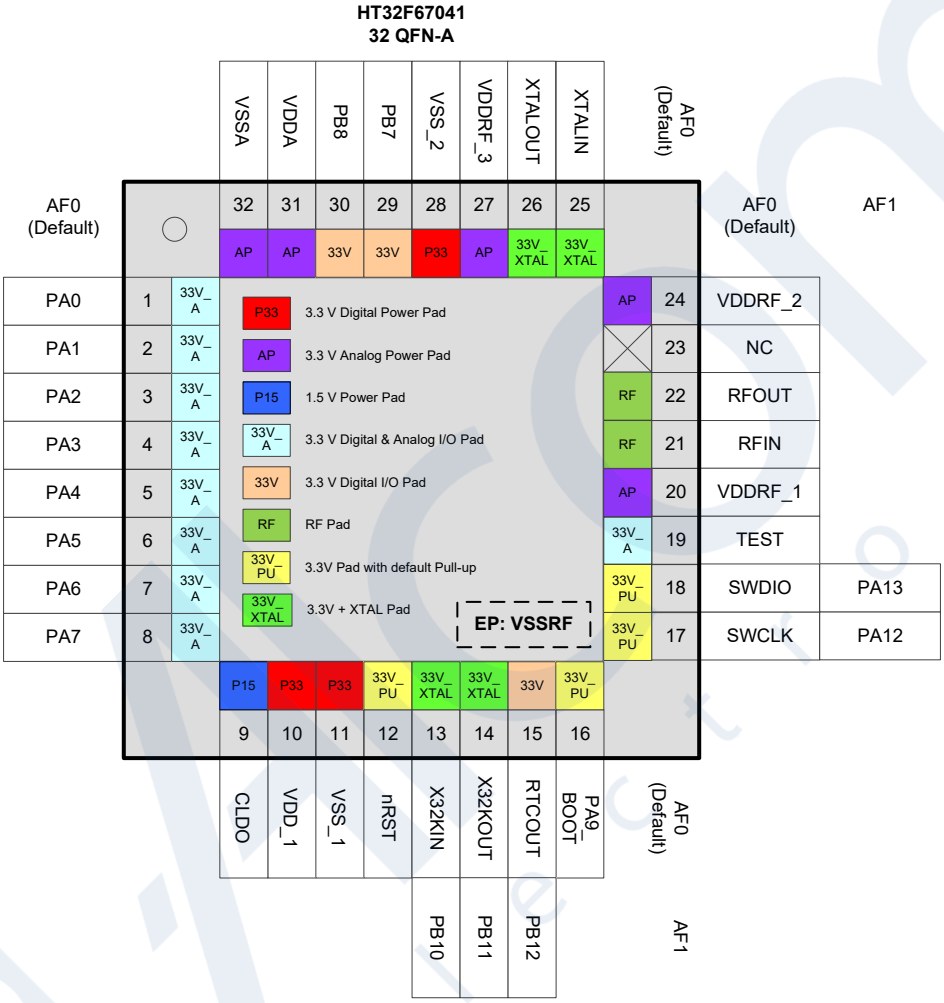


Figure 4. HT32F67041 32-pin QFN Pin Assignment

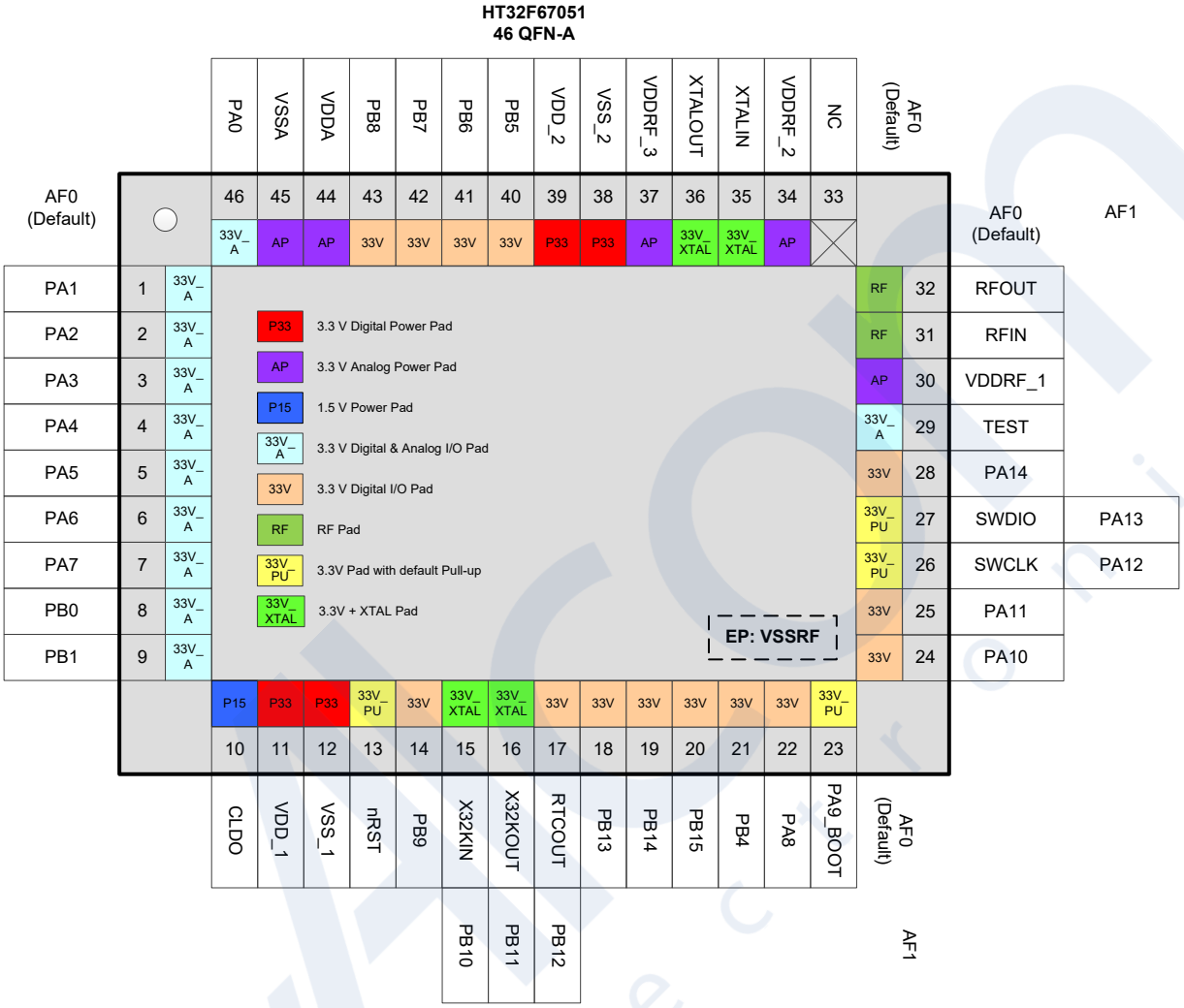


Figure 5. HT32F67051 46-pin QFN Pin Assignment

Table 3. Pin Assignment

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
46 QFN	32 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I²C	N/A	N/A	N/A	N/A	RF	SCTM	N/A	System Other
46	1	PA0		ADC_IN0			SPI0_SEL							GIO0			VREF
1	2	PA1		ADC_IN1			SPI0_SCK							GIO1			
2	3	PA2		ADC_IN2		GT_CH0	SPI0_MOSI							GIO2	SCTM0		
3	4	PA3		ADC_IN3		GT_CH1	SPI0_MISO							GIO3	SCTM1		
4	5	PA4		ADC_IN4		GT_CH2	SPI1_SEL	UR0_TX	I2C0_SCL					GIO4	SCTM2		
5	6	PA5		ADC_IN5		GT_CH3	SPI1_SCK	UR0_RX	I2C0_SDA					GIO5	SCTM3		
6	7	PA6		ADC_IN6		GT_CH0	SPI1_MOSI	UR1_TX	I2C1_SCL						SCTM0		
7	8	PA7		ADC_IN7		GT_CH1	SPI1_MISO	UR1_RX	I2C1_SDA						SCTM1		
8		PB0		ADC_IN8		GT_CH2	SPI1_SEL	UR0_TX	I2C0_SCL						SCTM2		
9		PB1		ADC_IN9		GT_CH3	SPI1_SCK	UR0_RX	I2C0_SDA						SCTM3		
10	9	CLDO															
11	10	VDD_1															
12	11	VSS_1															
13	12	nRST															
14		PB9				GT_CH2	SPI1_SCK	UR0_TX	I2C0_SCL						SCTM2		
15	13	X32KIN	PB10				SPI0_SEL	UR1_TX	I2C1_SCL						SCTM3		
16	14	X32KOUT	PB11				SPI0_SCK	UR1_RX	I2C1_SDA						SCTM0		
17	15	RTCOUT	PB12			GT_CH1	SPI0_MISO	UR0_RX	I2C0_SDA						SCTM1		WAKEUP
18		PB13				GT_CH2	SPI0_MOSI	UR0_TX	I2C0_SCL						SCTM2		CKIN
19		PB14				GT_CH3	SPI0_SEL	UR1_TX	I2C1_SCL						SCTM3		
20		PB15				GT_CH0	SPI0_SCK								SCTM0		
21		PB4				GT_CH1	SPI0_MOSI	UR1_TX	I2C1_SCL						SCTM1		
22		PA8				GT_CH2	SPI0_MISO	UR1_RX	I2C1_SDA						SCTM2		
23	16	PA9_BOOT				GT_CH3	SPI0_MISO	UR0_RX	I2C0_SDA						SCTM3		CKOUT
24		PA10				GT_CH0		UR0_TX	I2C0_SCL						SCTM0		
25		PA11				GT_CH1		UR0_RX	I2C0_SDA						SCTM1		
26	17	SWCLK	PA12														
27	18	SWDIO	PA13														
28		PA14				GT_CH2	SPI1_SEL	UR1_RX	I2C1_SDA						SCTM2		
29	19	TEST															

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
46 QFN	32 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I²C	N/A	N/A	N/A	N/A	RF	SCTM	N/A	System Other
30	20	VDDRF_1															
31	21	RFIN															
32	22	RFOUT															
33	23	NC															
34	24	VDDRF_2															
35	25	XTALIN															
36	26	XTALOUT															
37	27	VDDRF_3															
38	28	VSS_2															
39		VDD_2															
40		PB5				GT_CH0	SPI1_MOSI	UR0_TX	I2C0_SCL						SCTM3		
41		PB6				GT_CH1	SPI1_MISO	UR0_RX	I2C0_SDA						SCTM0		
42	29	PB7				GT_CH2	SPI0_MOSI	UR1_TX	I2C1_SCL						SCTM1		
43	30	PB8				GT_CH3	SPI0_MISO	UR1_RX	I2C1_SDA						SCTM2		
44	31	VDDA															
45	32	VSSA															

Table 4. Pin Description

Pin Number		Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
46 QFN	32 QFN					Default Function (AF0)
46	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
1	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
2	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
3	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
4	5	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
5	6	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
6	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
7	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
8		PB0	AI/O	33V	4/8/12/16 mA	PB0
9		PB1	AI/O	33V	4/8/12/16 mA	PB1
10	9	CLDO	P	—	—	Core power LDO V_{CORE} output. A 1 μF capacitor must be connected as close as possible between this pin and VSS_1.
11	10	VDD_1	P	—	—	Voltage for digital I/O
12	11	VSS_1	P	—	—	Ground reference for digital I/O
13	12	nRST	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
14		PB9	I/O	33V	4/8/12/16 mA	PB9

Pin Number		Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
46 QFN	32 QFN					Default Function (AF0)
15	13	PB10	AI/O	33V	< 2 mA	X32KIN
16	14	PB11	AI/O	33V	< 2 mA	X32KOUT
17	15	PB12	I/O	33V	< 2 mA	RTCOUT
18		PB13	I/O	33V	4/8/12/16 mA	PB13
19		PB14	I/O	33V	4/8/12/16 mA	PB14
20		PB15	I/O	33V	4/8/12/16 mA	PB15
21		PB4	I/O	33V	4/8/12/16 mA	PB4
22		PA8	I/O	33V	4/8/12/16 mA	PA8
23	16	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
24		PA10	I/O	33V	4/8/12/16 mA	PA10
25		PA11	I/O	33V	4/8/12/16 mA	PA11
26	17	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
27	18	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
28		PA14	I/O	33V	4/8/12/16 mA	PA14
29	19	TEST	AI/O	33V	< 2 mA	TEST
30	20	VDDRF_1	P	—	—	Voltage for RF I/O
31	21	RFIN	AI/O	33V	< 2 mA	RFIN
32	22	RFOUT	AI/O	33V	< 2 mA	RFOUT
33	23	NC	—	—	—	—
34	24	VDDRF_2	P	—	—	Voltage for RF I/O
35	25	XTALIN	AI/O	33V	4/8/12/16 mA	XTALIN
36	26	XTALOUT	AI/O	33V	4/8/12/16 mA	XTALOUT
37	27	VDDRF_3	P	—	—	Voltage for RF I/O
38	28	VSS_2	P	—	—	Ground reference for digital I/O
39		VDD_2	P	—	—	Voltage for digital I/O
40		PB5	I/O	33V	4/8/12/16 mA	PB5
41		PB6	I/O	33V	4/8/12/16 mA	PB6
42	29	PB7	I/O	33V	4/8/12/16 mA	PB7
43	30	PB8	I/O	33V	4/8/12/16 mA	PB8
44	31	VDDA	P	—	—	Analog voltage for ADC
45	32	VSSA	P	—	—	Ground reference for ADC

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, PU = Pull-up.
2. 33V = 3.3 V tolerant.
3. The GPIOs are in an AF0 state after a V_{CORE} power on reset (POR) except for the RTCOUT pin.
4. In the Boot loader mode, the UART interface is available for communication.
5. The EP means the exposed pad on the packages. It must be connected to ground.
6. The VSSRF is ground reference for RF circuit.

5 Application Circuit

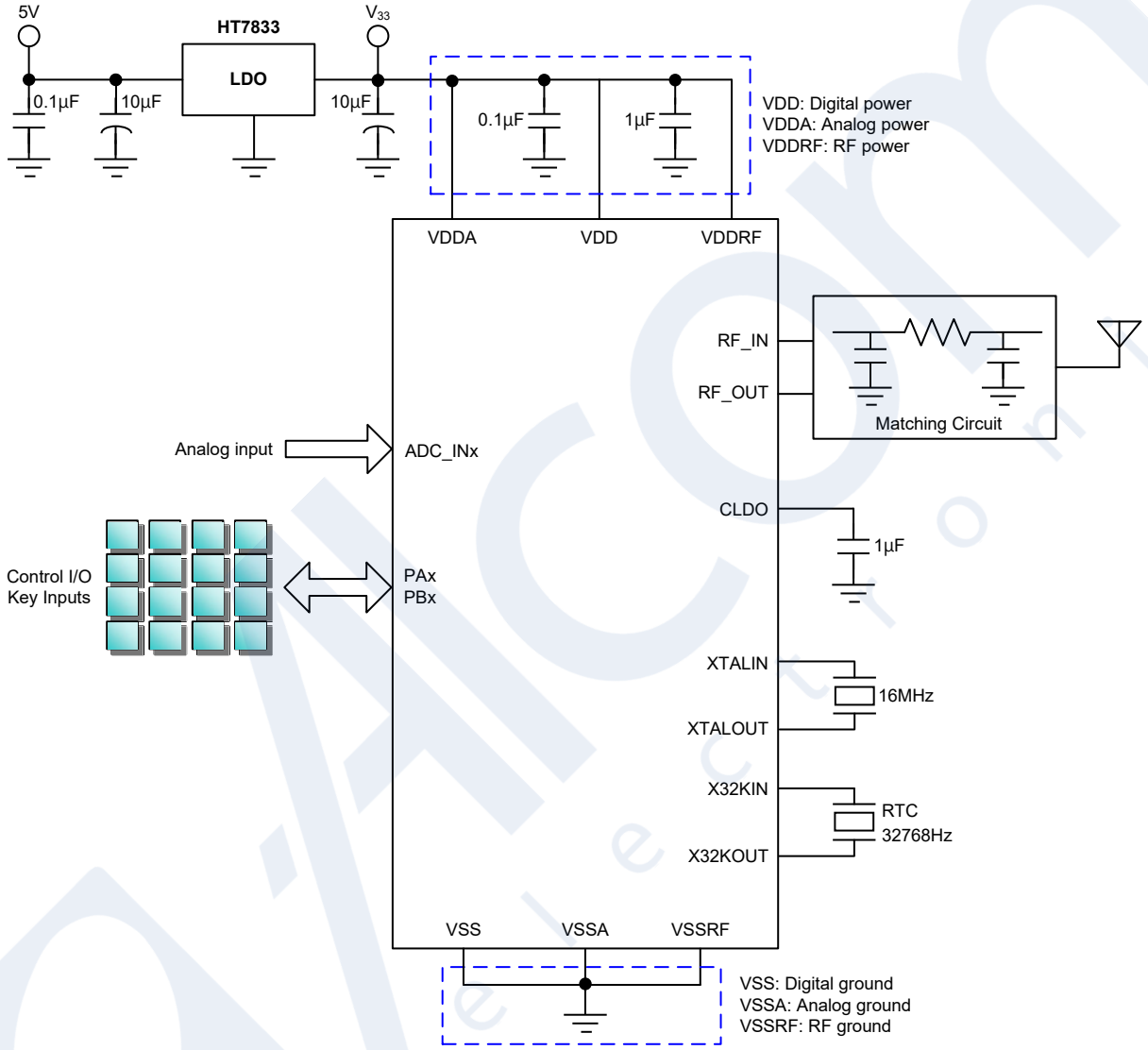


Figure 6. Application Circuit

6 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	I/O Operating Voltage	—	1.65	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V
V_{DDRF}	RF Operating Voltage	—	2.2	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 10 mA and voltage variant = ± 5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
		V_{DD} = 1.65 V ~ 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	20	25	
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 8. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{ULDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{ULDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 9. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	60 MHz	V_{DD} = 3.3 V, HSE = 16 MHz, PLL = 60 MHz	All peripherals enabled	—	17.8	—	mA
				All peripherals disabled	—	7.8	—	
		20 MHz	V_{DD} = 3.3 V, HSE = 16 MHz, PLL = 20 MHz	All peripherals enabled	—	7	—	
				All peripherals disabled	—	3.6	—	
		8 MHz	V_{DD} = 3.3 V, HSE off, PLL off, HSI = 8 MHz	All peripherals enabled	—	3.2	—	
				All peripherals disabled	—	1.5	—	
		32 kHz	V_{DD} = 3.3 V, HSE off, PLL off, LSI on, f_{PCLK} = 32 kHz	All peripherals enabled	—	19.8	—	μA
				All peripherals disabled	—	14.5	—	
	Supply Current (Sleep Mode)	60 MHz	V_{DD} = 3.3 V, HSE = 16 MHz, PLL = 60 MHz, MCU core sleep	All peripherals enabled	—	12	—	mA
				All peripherals disabled	—	1.3	—	
		20 MHz	V_{DD} = 3.3 V, HSE = 16 MHz, PLL = 20 MHz, MCU core sleep	All peripherals enabled	—	4.5	—	
				All peripherals disabled	—	0.8	—	
		8 MHz	V_{DD} = 3.3 V, HSE off, PLL off, HSI = 8 MHz, MCU core sleep	All peripherals enabled	—	2.3	—	
				All peripherals disabled	—	0.5	—	
I_{DD}	Supply Current (Deep-Sleep1 Mode)	—	V_{DD} = 3.3 V, HSE/HSI/LSE/PLL clock off, LDO off, ULDO on, LSI on, RTC off		—	—	9.5	μA
	Supply Current (Deep-Sleep2 Mode)	—	V_{DD} = 3.3 V, HSE/HSI/LSE/PLL clock off, LDO off, ULDO on, LSI on, RTC off		—	—	9.5	μA
	Supply Current (Power-Down Mode)	—	V_{DD} = 3.3 V, LDO off, ULDO off, LSE off, LSI on, RTC on		—	—	2.05	μA
			V_{DD} = 3.3 V, LDO off, ULDO off, LSE off, LSI on, RTC off		—	—	2.0	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.

3. RTC means real time clock.
4. Code = while (1) {208 NOP} executed in Flash.

Reset and Supply Monitor Characteristics

Table 10. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.4	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	T_A = -40 °C ~ 85 °C	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 11. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation Current (3)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 12. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.2	—	3.6	V
f_{HSE}	HSE Frequency	49US/SMD3225/SMD2520	—	16	—	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	12	16	20	pF
Δf_{XTAL}	XTAL Tolerance	—	-20	—	20	ppm
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	100	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	49US with a 12pF, C_{LOAD} @ V_{DD} = 3.3V	—	—	1	ms
		SMD3225 with a 12pF C_{LOAD} @ V_{DD} = 3.3V	—	—	1.5	ms

Table 13. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz R_{ESR} = 50 kΩ, C_L ≥ 7 pF V_{DD} = 1.65 V ~ 2.7 V T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz R_{ESR} = 50 kΩ, C_L < 7 pF V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 14. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	1.65	—	3.6	V
f_{CK_HSI}	HSI Frequency	V_{DD} = 3.3 V	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 2.5 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-2.5	—	2.5	%
		V_{DD} = 2.2 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{CK_HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{CK_HSI} = 8 MHz	—	300	500	μA
	HSI Oscillator Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{CK_HSI} = 8 MHz	—	—	10	μs

Table 15. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V	—	—	100	μs

System PLL Characteristics

Table 16. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 17. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 18. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	$V_I = V_{SS}$, On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	3.3 V I/O	$V_I = V_{DD}$, On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	3.3 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		16	—	—	
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ

ADC Characteristics

Table 19. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	A/D Converter Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

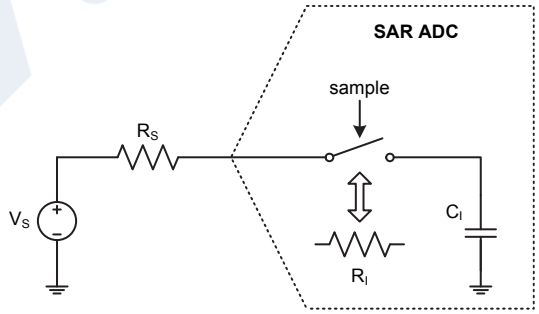


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 20. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		1.65	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 ˚C Temperature	V_{DDA} ≥ 1.65 V	VREFSEL[1:0] = 00	1.190	1.215	1.240	V
		V_{DDA} ≥ 2.30 V	VREFSEL[1:0] = 01	1.96	2.00	2.04	
		V_{DDA} ≥ 2.80 V	VREFSEL[1:0] = 10	2.45	2.50	2.55	
		V_{DDA} ≥ 3.00 V	VREFSEL[1:0] = 11	2.65	2.70	2.75	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 1.65 V ~ 3.6 V, V_{REF} = 1.215 V, T_A = -40 °C ~ 85 °C		-3.0	—	+3.0	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	45	55	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

GPTM/SCTM Characteristics

Table 21. GPTM / SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM / SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 22. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: SEQFILTER = 01 and COMBFILTEREN = 0 that COMB_filter is disabled.

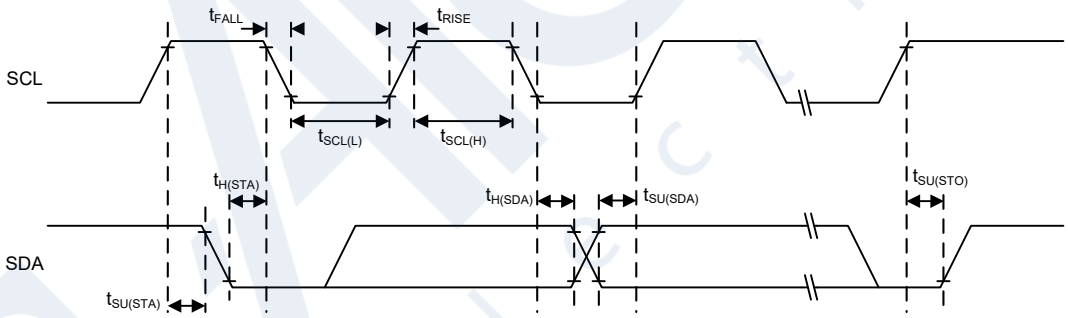


Figure 8. I²C Timing Diagram

SPI Characteristics

Table 23. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

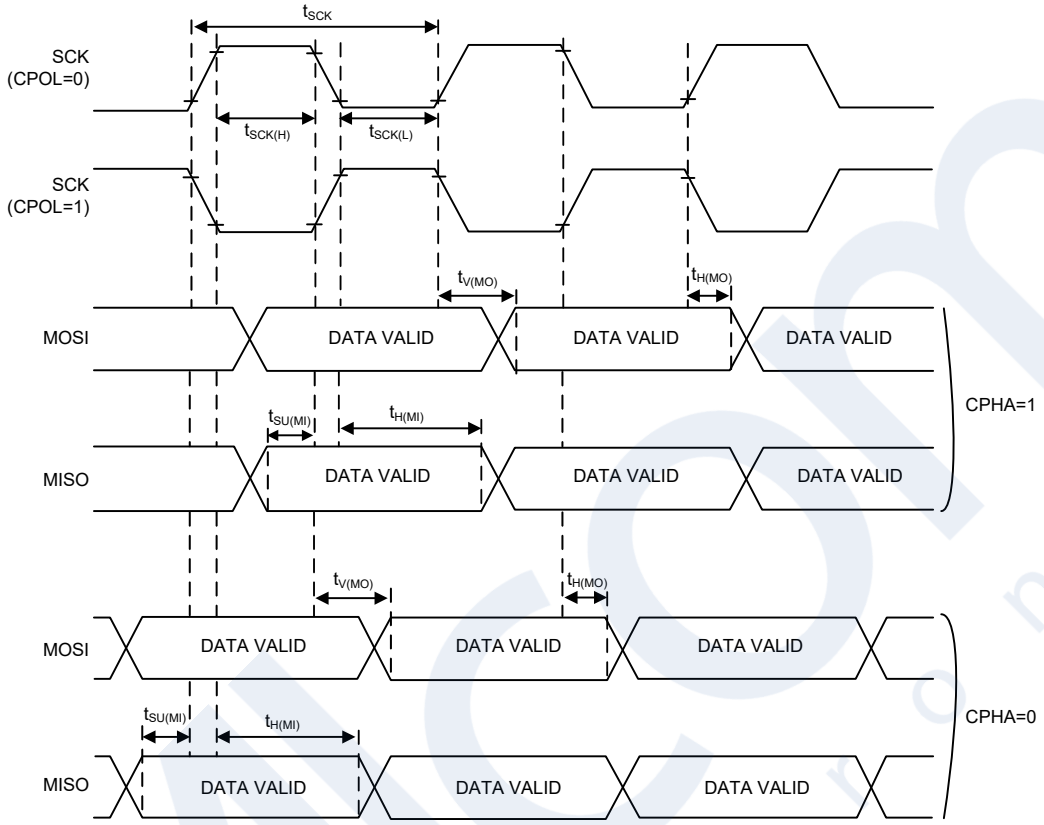


Figure 9. SPI Timing Diagram – SPI Master Mode

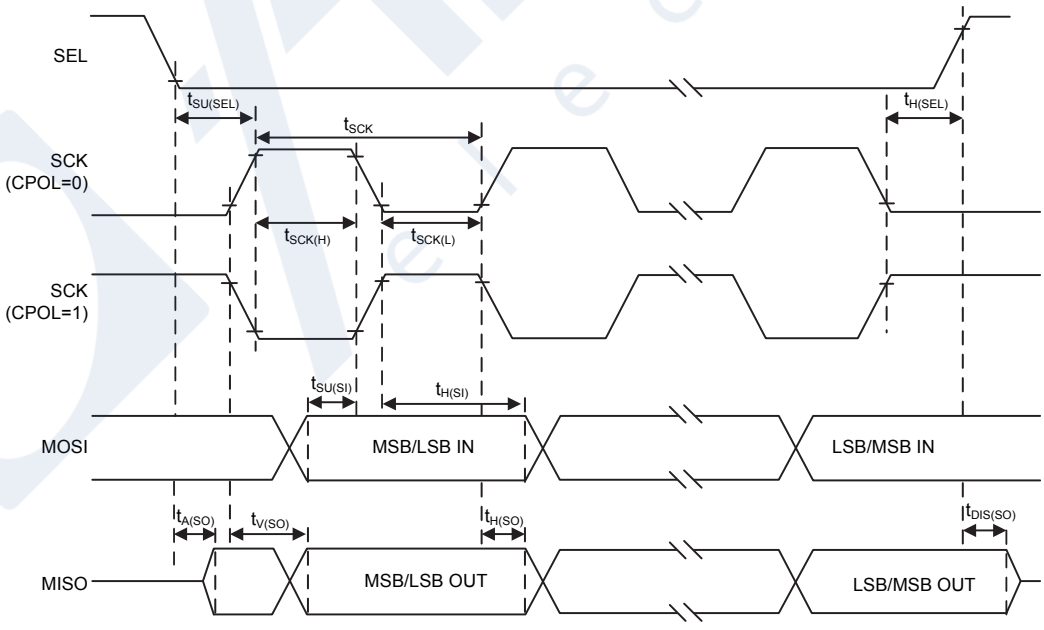


Figure 10. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

RF Transceiver Characteristics

Table 24. RF Transceiver Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDRF}	Operating Voltage	—	2.2	—	3.6	V
I_{DDRF}	Operating Current	RF Deep Sleep Mode	—	0.5	—	μA
		RF Light Sleep Mode (X'tal on)	—	600	—	μA
I_{TX}	TX Current Consumption	TX Output Power @ 0 dBm	—	17	—	mA
		TX Output Power @ 5 dBm	—	20	—	mA
I_{RX}	RX Current Consumption	RX Mode	—	17	—	mA
f_{RF}	RF Frequency Band	—	2400	—	2480	MHz
DR	Data Rate	—	125	—	250	Kbps
f_{DEV}	Frequency Deviation	Data Rate:125 / 250 Kbps	—	160	—	kHz
PN_{PLL}	PLL Phase Noise	@ ±100 kHz offset	—	-85	—	dBc/Hz
		@ ±1 MHz offset	—	-95	—	dBc/Hz
ACP	Adjacent Channel Transmit Power(250Kbps)	1st ACP ± 1 MHz offset	—	-30	—	dBc
		2nd ACP ± 2 MHz offset	—	-45	—	dBc
SE_{TX}	TX Spurious Emission	f < 1 GHz	—	—	-36	dBm
		47 MHz < f < 74 MHz 87.5 MHz < f < 118 MHz 174 MHz < f < 230 MHz 470 MHz < f < 862 MHz	—	—	-54	
		2nd, 3rd Harmonic	—	—	-30	
		1.8 GHz ~ 1.9 GHz	—	—	-47	
		5.15 GHz ~ 5.3 GHz	—	—	-47	
P_{RF}	RF Output Power	2400 ~ 2480 MHz, 50Ω Load	-10	5	6	dBm
SEN_{RX}	Receiver Sensitivity @ BER < 0.1%	DR = 125 kbps (f_{DEV}=160 kHz)	—	-97	—	dBm
		DR = 250 kbps (f_{DEV}=160 kHz)	—	-96	—	
SE_{RX}	RX Spurious Emission	25 MHz ~ 1 GHz	—	—	-57	dBm
		Above 1 GHz	—	—	-47	
$P_{IN.max}$	Maximum Input Power	—	—	—	10	dBm
	RSSI Range	AGC on	-110	—	-20	dBm

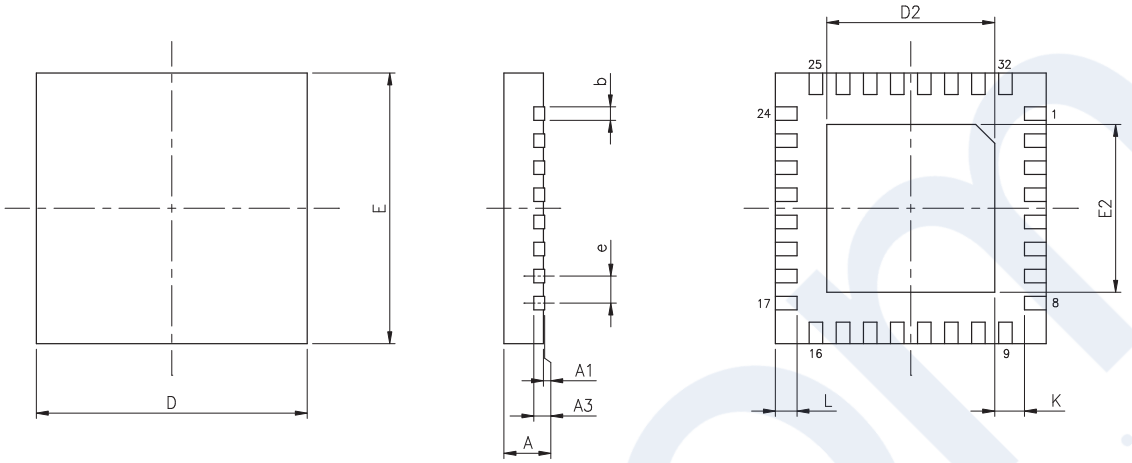
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

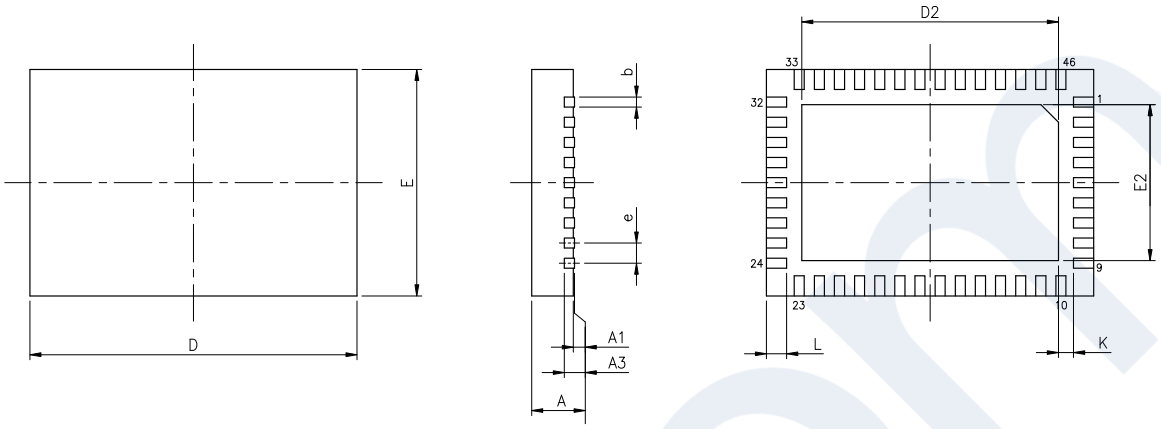
SAW Type 32-pin QFN (5mm × 5mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.007	0.010	0.012
D		0.197 BSC	
E		0.197 BSC	
e		0.020 BSC	
D2	0.122	—	0.142
E2	0.122	—	0.142
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.10	—	3.60
E2	3.10	—	3.60
L	0.35	0.40	0.45
K	0.20	—	—

SAW Type 46-pin QFN (6.5mm × 4.5mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.256 BSC	
E		0.177 BSC	
e		0.016 BSC	
D2	0.197	—	0.205
E2	0.118	—	0.126
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		6.50 BSC	
E		4.50 BSC	
e		0.40 BSC	
D2	5.00	—	5.20
E2	3.00	—	3.20
L	0.35	0.40	0.45
K	0.20	—	—