HyperBus ™ / PSRAM Memory Interface Solution

HyperBus is a high-performance memory interface which offers:

• Low signal count (Address, Command, and Data using only eight DQ pins)

• High Bandwidth performance

• Low Power consumption

• User-friendly protocol

HyperBus currently interfaces to the HyperRAM TM and HyperFlash TM memories with maximum performance (up to 333 MBytes/s). Designed for reliable while being compactness, these memories are great for mobile and automotive applications.

Features:

• Low FPGA Fabric resource utilization

• Supports Burst Mode for Read/Write transfers

• Operating Frequency up to 166 MHz (max 333 MBytes/s) with only 12 x IO pins (CS, Clk/Clk_n, DQS, DQ[7:0])

• 16 bit Slave Data Interface with Burst (and wrap) support

• 16 bit Slave Register Interface to access HyperRAM memory registers

• Burst Wrap mode support

• Configurable IP options

• SCF Timing Constraints.

• Dual-die memories supported

GOWIN
PROGRAMMING FOR FUTURE

- Support proprietary memory interfaces without ASIC spin
  - Time and cost to market – Develop now, no ASIC costs
  - Optimized resources & architectures – IO, interfaces and logic only for the specific use case
- Additional Gowin Advantage
  - R-Series devices with built in PSRAM with a Hyperbus Interface!
    - No additional logic required to interface between internal PSRAM and External HyperRAM!
    - External SPI Flash can also be multiplexed with HyperBUS IO!
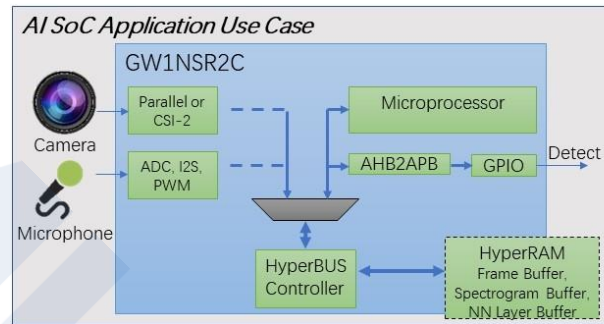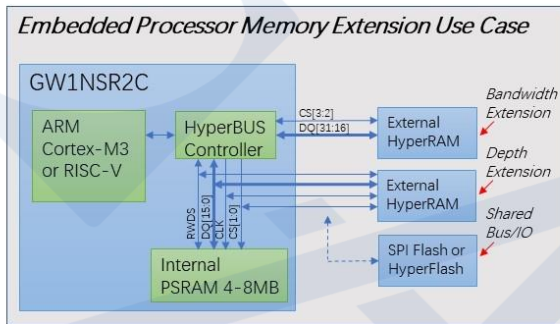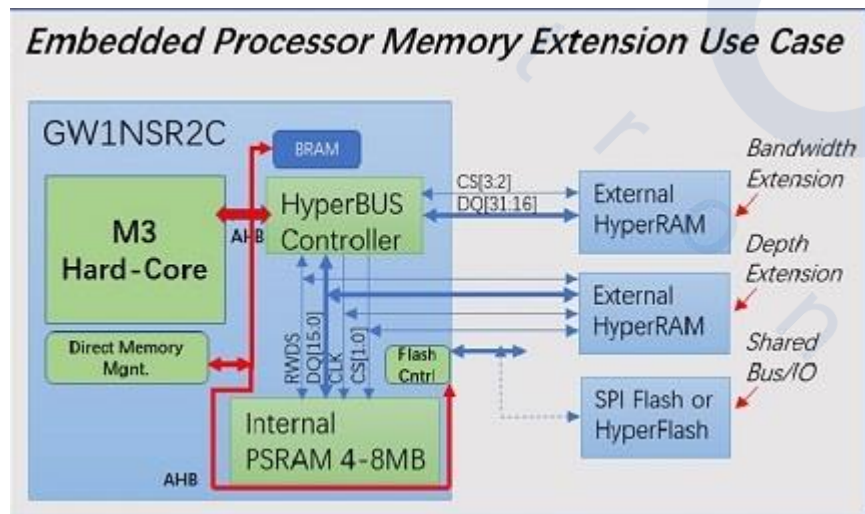

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Memories Supported:

Winbond PSRAM

ISSI IS66/67WVH8M8ALL/BLL - 64Mb

Cypress S27KL/S0641 - 64Mb

Cypress S70KL/S1281 - 128Mb

Embedded Processor Memory Extension Use Case

2AR-18-P

- BRAM
- M1 Soft-Core
- Direct Memory Mgnt.
- HyperBUS Controller
  - CS[3:2]
  - DQ[31:16]
- AHB
- RWDS
- DQ[15:0]
- CLK
- CS[1:0]
- Flash Cntrl
- Internal PSRAM 4-8MB
- AHB

- External HyperRAM — *Bandwidth Extension*
- External HyperRAM — *Depth Extension*
- SPI Flash or HyperFlash — *Shared Bus/IO*