GW1NZ series

The GW1NZ series of FPGA products offer Always On, ultra-low power consumption at extremely low costs. The non-volatile devices are offered with various packages for flexible usage. They can be widely used in communication, industry control, consumer (especially mobile and wearable), etc.

Features

- **Ultra low power consumption**

—55nm embedded flash technology

—LV: Supports 1.2V core voltage

—ZV: Supports 0.9V core voltage (below 28uW standby power consumption Always On)

—Power Management Module

—Clock dynamically turns on and off

- **Power Management Module**

—SPMI: System power management interface hard core

- **User Flash**

—64K bits

—Data Width: 32

— 10,000 write cycles

—Greater than ten years' data retention at +85 ℃

—Supports page erasure: 2048 bytes per page

—Duration: Max. 25ns

—Electric current

a) Read Operation: 2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX);

b) Write operation/erase operation: 12/12 mA(MAX)

—Quick page erasure/Write operation

—Clock frequency: 40MHz

—Write operation time: ≤16μs

—Page erasure time: ≤120 ms

- **Multiple I/O Standards**

—LVCMOS33/25/18/15/12；LVTTL33， PCI，

—LVDS25E， BLVDSE， MLVDSE， LVPECLE， RSDSE

—Input hysteresis option

—Supports 4mA,8mA,16mA,24mA,etc. drive options

—Slew Rate option

—Output drive strength option

—Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option

—Hot Socket

—I3C hard core, supports SDR mode

- **Abundant Slices**

—Four input LUT (LUT4)

—Double-edge flip-flops

—Supports shifter register

—Supports shadow SRAM

- **Block SRAM with multiple modes**

—Supports Dual Port, Single Port, and Semi Dual Port

—Supports bytes write enable

- **Flexible PLLs**

—Frequency adjustment (multiply and division) and phase adjustment

—Supports global clock

- **Built-in Flash programming**

—Instant-on

—Supports security bit operation

—Supports AUTO BOOT and DUAL BOOT

- **Configuration**

—JTAG configuration

—Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

GW1NZ Family Table

Device	GW1NZ-1
LUT4	1,152
Flip-Flop (FF)	864
Shadow SRAM S-SRAM (bits)	4K
Block SRAM B-SRAM (bits)	72K
PLLs + DLLs	1 + 0
User Flash (bits)	64K
Max. User I/O on die	48
VCC	1.2V(LV) / 0.9V(ZV)

Package Information and Max. User I/O

Package	Pitch (mm)	Size (mm)	GW1NZ-1
FN32	0.4	4 x 4	25
CS16	0.4	1.8 x 1.8	11
QN48	0.4	6 x 6	40