GOWIN
PROGRAMMING FOR THE FUTURE

GW1NRF series of Bluetooth FPGA Products

Data Sheet

DS891-1.0E, 11/12/2019

Disclaimer

Revision History

Date	Version	Description
11/12/2019	1.0E	Initial version published.

Contents

Contents i
List of Figures iii
List of Tables v
1 About This Guide 1
1.1 Purpose 1
1.2 Supported Products 1
1.3 Related Documents 1
1.4 Abbreviations and Terminology 2
1.5 Support and Feedback 3
2 General Description 4
2.1 Features 4
2.2 Product Resources 7
2.3 Package Information 8
3 Architecture 9
3.1 Architecture Overview 9
3.2 SoC System 11
3.3 Configurable Function Unit 18
3.4 IOB 20
3.5 Block SRAM (B-SRAM) 30
3.6 User Flash 40
3.7 DSP 41
3.8 Clock 45
3.9 Long Wire (LW) 50
3.10 Global Set/Reset (GSR) 51
3.11 Programming Configuration 51
3.12 On Chip Oscillator 52
4 AC/DC Characteristics 53
4.1 Operating Conditions 53
4.2 ESD 54
4.3 DC Characteristics 56

4.4 Switching Characteristics 64
4.5 User Flash Characteristics 66
4.6 Configuration Interface Timing Specification 69
5 Ordering Information 74
5.1 Part Name 74
5.2 Package Mark 75

List of Figures

Figure 3-1 GW1NRF Architecture Overview 9
Figure 3-2 RF Transceiver Block Diagram 16
Figure 3-3 CFU View 18
Figure 3-4 Register in CLS 19
Figure 3-5 IOB Structure View 20
Figure 3-6 GW1NRF I/O Bank Distribution 21
Figure 3-7 True LVDS Design 24
Figure 3-8 I/O Logic Output 24
Figure 3-9 I/O Logic Input 25
Figure 3-10 IODELAY 25
Figure 3-11 Register Structure in I/O Logic 26
Figure 3-12 IEM Structure 26
Figure 3-13 I/O Logic in Basic Mode 27
Figure 3-14 I/O Logic in SDR Mode 27
Figure 3-15 I/O Logic in DDR Input Mode 28
Figure 3-16 I/O Logic in DDR Output Mode 28
Figure 3-17 I/O Logic in IDES10 Mode 28
Figure 3-18 I/O Logic in OSER4 Mode 28
Figure 3-19 I/O Logic in IVideo Mode 29
Figure 3-20 I/O Logic in OVideo Mode 29
Figure 3-21 I/O Logic in IDES8 Mode 29
Figure 3-22 I/O Logic in OSER8 Mode 30
Figure 3-23 I/O Logic in IDES10 Mode 30
Figure 3-24 I/O Logic in OSER10 Mode 30
Figure 3-25 Single Port Block Memory 34
Figure 3-26 Dual Port Block Memory 35
Figure 3-27 Semi Dual Port Block Memory 35
Figure 3-28 ROM Block Memory 36
Figure 3-29 Pipeline Mode in Single Port, Dual Port and Semi Dual Port 37
Figure 3-30 Independent Clock Mode 39
Figure 3-31 Read/Write Clock Mode 39
Figure 3-32 Single Port Clock Mode 39

Figure 3-33 GW1NRF User Flash Ports 40
Figure 3-34 DSP Macro 42
Figure 3-35 GW1NRF-4B Clock Resources 45
Figure 3-36 GCLK Quadrant Distribution 46
Figure 3-37 DQCE Concept 47
Figure 3-38 DCS Concept 47
Figure 3-39 DCS Rising Edge 47
Figure 3-40 DCS Falling Edge 48
Figure 3-41 PLL Structure 48
Figure 3-42 GW1NRF HCLK Distribution 50
Figure 3-43 GW1NRF DLL Function 50
Figure 4-1 GW1NRF User Flash Read Operation 68
Figure 4-2 GW1NRF User Flash Program Operation 68
Figure 4-3 GW1NRF User Flash Erase Operation 68
Figure 4-4 JTAG Timing 69
Figure 4-5 Power Recycle Timing 70
Figure 4-6 RECONFIG_N Trigger Timing 70
Figure 4-7 SSPI Timing Diagram 71
Figure 4-8 MSPI Timing Diagram 72
Figure 5-1 Part Naming–ES 74
Figure 5-2 Part Naming–Production 74
Figure 5-3 Package Mark 75

List of Tables

Table 1-1 Abbreviations and Terminologies 2
Table 2-1 Product Resources 7
Table 2-2 Package Information, Max. I/O and LVDS Pairs 8
Table 3-1 Register Description in CLS 19
Table 3-2 Output I/O Standards and Configuration Options 21
Table 3-3 Output I/O Standards and Configuration Options 22
Table 3-4 B-SRAM Signals 31
Table 3-5 Memory Size Configuration 32
Table 3-6 Dual Port Mixed Read/Write Data Width Configuration 32
Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration 32
Table 3-8 Single Port Block Memory Configuration 34
Table 3-9 Dual Port Memory Configuration 35
Table 3-10Semi Dual Port Memory Configuration 36
Table 3-11 Block ROM Configuration 36
Table 3-12 Clock Operations in Different B-SRAM Modes 38
Table 3-13 Flash Module Signal Description 40
Table 3-14 Truth Table in User Mode 41
Table 3-15 DSP Ports Description 42
Table 3-16 Internal Registers Description 43
Table 3-17 PLL Ports Definition 49
Table 3-18 GW1NRF-4B Oscillator Output Frequency Options 52
Table 4-1 Absolute Max. Ratings 53
Table 4-2 Recommended Operating Conditions 53
Table 4-3 Power Supply Ramp Rates 54
Table 4-4 Hot Socket Specifications 54
Table 4-5 GW1NRF ESD – HBM 54
Table 4-6 GW1NRF ESD - CDM 54
Table 4-7 DC Electrical Characteristics under Recommended Operating Conditions 54
Table 4-8 Static Supply Current[1] 56
Table 4-9 DC Characteristics, DCDC Step-Down Configuration, VBAT2=3.0V 56
Table 4-10 DC Characteristics, DCDC Step-Up Configuration, VBAT2=1.5V 57
Table 4-11 Low Frequency Crystal Oscillator Specifications 58

Table 4-12 High Frequency Crystal Oscillator Specifications 58
Table 4-13 General RF Characteristics 58
Table 4-14 Transmitter Characteristics 58
Table 4-15 Receiver Characteristics 60
Table 4-16 I/O Operating Conditions Recommended 60
Table 4-17 IOB Single‐Ended DC Electrical Characteristic 61
Table 4-18 IOB Differential Electrical Characteristics 62
Table 4-19 CFU Block Internal Timing Parameters 64
Table 4-20 B-SRAM Internal Timing Parameters 64
Table 4-21 DSP Internal Timing Parameters 64
Table 4-22 External Switching Characteristics 65
Table 4-23 On chip Oscillator Output Frequency 65
Table 4-24 User Flash DC Characteristics 66
Table 4-25 User Flash Timing Parameters 66
Table 4-26 JTAG Timing Parameters 69
Table 4-27 Parameters for Power Recycle and RECONFIG_N Trigger Timing 70
Table 4-28 SSPI Timing parameters 71
Table 4-29 MSPI Timing Parameters 72

1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NRF series of Bluetooth FPGA products. It is designed to help you understand the GW1NRF series of Bluetooth FPGA products quickly and select and use devices appropriately.

1.2 Supported Products

The information in this guide applies to the following products:

GW1NRF series of Bluetooth FPGA products: GW1NRF- 4B.

1.3 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1NRF series of Bluetooth FPGA products Data Sheet
2. Gowin FPGA Products Programming and Configuration User Guide
3. GW1NRF series of Bluetooth FPGA products Package and Pinout
4. GW1NRF-4B Pinout

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
SIP	System in Package
SOC	System on Chip
RF	Radio Freqency
OTP	One Time Programmable
HCI	Host Controller Interface
ACI	Application Controller Interface
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
PSRAM	Pseudo Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
QN88	QFN88
TDM	Time Division Multiplexing

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2General Description

The GW1NRF series of FPGA products are the first generation products in the LittleBee® family and represent one form of SoC FPGA. The GW1NRF series of FPGA products integrate 32 bits hardcore processor and support Bluetooth 5.0 Low Energy radio. They have abundant logic units, IOs, built-in B-SRAM and DSP resources, power management module, and security module. The GW1NRF series provides low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NRF series of Bluetooth FPGA products including FPGA synthesis, layout, place and routing, data bitstream generation and download, as well as microprocessor configuration and firmware compilation..

2.1 Features

- User Flash
  - Up to 1,792 Kbits
  - 10,000 write cycles
- Lower power consumption
  - 55 nm embedded flash technology
  - LV: supports 1.2 V core voltage
  - UV: Built-in linear voltage regulator unit, unified power supply of V_{CC}/ V_{CCX}/ V_{CCO}
  - Clock dynamically turns on and off
- 32bits MCU: ARC EM4
  - Runs at 24MHz
  - Floating-point unit for sensor processing
  - 136KB ROM
  - 128KB OTP
  - 48KB instruction RAM
  - 28KB data RAM
  - Universal, sleep, and Bluetooth protocol timers

  - I2C and SPI master interfaces
  - Supports 8 GPIO
- Bluetooth 5.0 Low Energy Technology
  - BT 5.0 Controller Subsystem(QD ID 93999)
  - Bluetooth stack(QD ID 84268) in ROM
  - SPI and UART HCI/ACI Transport Layers
  - Up to engiht simultaneous connections supported
  - Extended PDU length and enhanced security
- Security Features
  - TRNG (True Random Number Generator)
  - AES-128 Hardware Encryption Engine
  - Key Generation
- Firmware Over-the-Air Updating
  - Per application, function, and configuration
- Sophisticated Power Management System
  - Digital step-up/down DCDC operation
  - Supports 1.5V and 3.0V batteries
  - Scheduler and memory manager
  - Low frequency RC or crystal oscillator time base
- Low Current Consumption at 3V
  - 3.0mA typical peak receiver current
  - 5.2mA typical peak transmitter current at0.4dBm
  - 1.0uA connected sleep mode
  - 5nA chip disable mode
- High Performance RF
  - -94dBm Bluetooth low energy receiver sensitivity for 1Mpbs operation and 37 byte payload
  - -34dBm ~ +6.1dBm transmitter output power range
- Multiple I/O standards
  LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4 mA,8 mA,16 mA,24 mA,etc. drive options
  - Slew rate option
  - Output drive strength option
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
  - Hot socket
- High performance DSP
  - High performance digital signal processing ability
  - Supports 9 x 9,18 x 18,36 x 36 bits multiplier and 54 bits accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter
- Abundant slices
  - Four-input LUT (LUT4)

  - Double-edge flip-flops
  - Supports shift register and distributed register
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports bytes write enable
- Flexible PLLs+DLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports JTAG transparent transmission
  - Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1NRF-4B
LUT4	4,608
Flip-Flop (FF)	3,456
Block SRAM B-SRAM (bits)	180K
B-SRAM quantity B-SRAM	10
User Flash (bits)	256K
18 x 18 Multiplier	16
PLLs+DLLs	2+2
Total number of I/O banks	4
Max. I/O[1]	25
Hard Core Processor	ARC EM4
Memory Module	136KB ROM 48KB IRAM 28KB DRAM 128KB OTP
RF module	Bluetooth 5.0 LE RF
Security Core	AES hard core encryption TRNG Key generator
Low power module	Power Management Unit DCDC Step Up/Down Regulator
Core Voltage (LV)	1.2V
Core Voltage (UV)	1.8V/2.5V/3.3V

2.3 Package Information

Table 2-2 Package Information, Max. I/O and LVDS Pairs

Package	Pitch(mm)	Size(mm)	GW1NRF-4B
QN48	0.4	6 x 6	25(4)

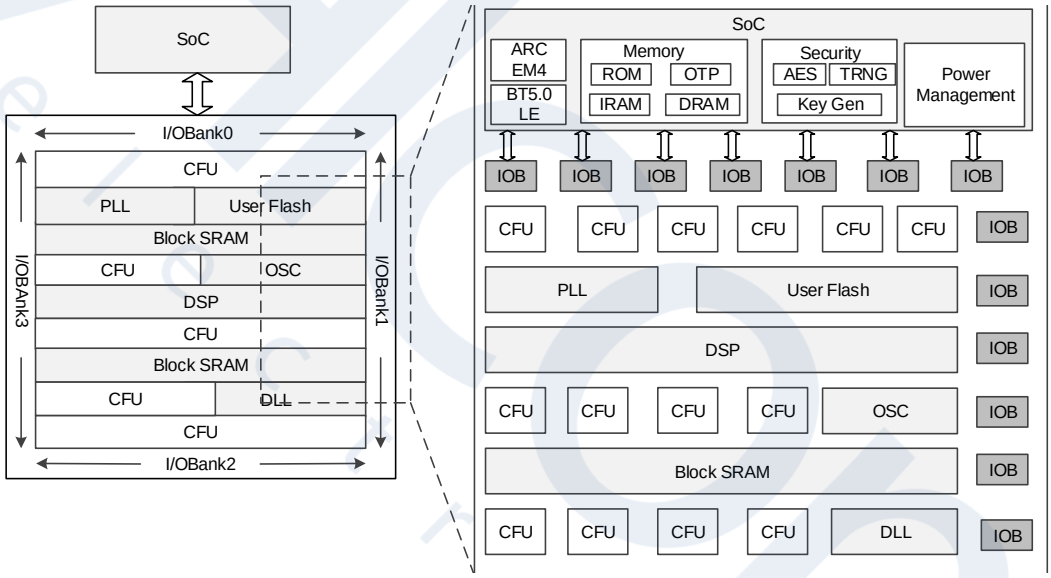
Note!

- [1] The package types in this data sheet are written with abbreviations. See 5.1 Part Name.
- For more detailed information, please refer to *GW1NRF-4B Pinout*.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. See *GW1NRF series of Bluetooth FPGA Products Package and Pinout Manual* for more details.

3 Architecture

3.1 Architecture Overview

Figure 3-1 GW1NRF Architecture Overview



GW1NRF series is one form of SoC with abundant resources, flexiable usage, small package size, and low comsuption. It supports Bluetooth 5.0 Low Energy radio. 32 bits MCU can be used to control data communication between RF modem, memories, and external peripherals, such as sensors, memory, display, or touch drivers. The built-in floating point unit can be exploited to implement advanced algorithms such as sensor fusion. The built-in BSRAM and PLL resources provide data storage with high speed and high bandwidth.

Included in ROM is a Bluetooth 5.0 link layer with a Host Controller Interface (HCI), a Bluetooth stack with proprietary Application Controller Interface (ACI), several profiles and over-the-air firmware updating routines. The Bluetooth low energy controller and host can be configured to support up to eight simultaneous connections. Secure connections and extended packet length are also supported.

AES-128 hardcore, TRNG, and the key generator guarantee the security of data communication.

SoC includes a socphisticated on-chip power management system with built-in DCDC regulator. It can be configured to 1.5V and 3V automaticly. Current consumption is minimized for all modes of the application utilizing an efficient scheduler and memory manager. Several memory configuration options allow for optimum performace for any given application. A stable, low-power sleep oscillator (RC or crystal based) minimizes power consumption while in a connected state.

SoC features a state-of-the-art 2.4GHz transceiver: an extremely low-power receiver with excellent sensitivity/selectivity, and a programmable transmitter for optimized output power and current comsumption. See 3.2 SoC System for more detailed information.

The core of the GW1NRF devices is the array of configurable logic unit (CFU) surrounded by IO blocks. GW1NRF also provides B-SRAM, DSP, PLL, DLL, user Flash, and on chip oscillator and supports Instant-on. See Table 2-1 for more detailed information on internal resources.

Configurable Function Unit (CFU) is the base cell for the array of the GW1NRF series of Bluetooth FPGA products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode and ALU mode. See 3.2.5 Operating Modes for more detailed information.

The I/O resources in the GW1NRF series of Bluetooth FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. See 3.4 IOB for more detailed information.

The B-SRAM is embedded as a row in the GW1NRF series of Bluetooth FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. Each B-SRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. See 3.5 Block SRAM (B-SRAM) for more detailed information.

The User Flash is embedded in the GW1NRF series of Bluetooth FPGA products, without loss of data even if power off. See 3.6 User Flash for more detailed information.

The GW1NRF series of Bluetooth FPGA products also provide DSP. DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. See 3.7 DSP for more detailed information.

GW1NRF provides one PLL and one DLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the GW1NRF series of the FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock

resource for user designs with the clock precision reaching ±5%. See 3.8Clock, 3.12On Chip Oscillator for more detailed information.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NRF series of Bluetooth FPGA products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. See 3.8Clock, 3.9Long Wire (LW), 3.10Global Set/Reset (GSR) for more detailed information.

3.2 SoC System

The CPU is a 32-bit ARC EM4 V3.2 by Synopsys, with an integrated floating point unit (FPU), which is optimized for area, power, and performance efficiency. The ARC's RISC pipe-lined architecture with mostly single-cycle operations is approximately 30% more efficient than other popular 32-bit CPUs. Effective use of the sleep instruction minimizes power consumption. During sleep mode the entire MCU subsystem can be shut off and only the power management system and required state retention memories (if any) need to be powered. The power management system will properly wakeup the MCU subsystem when it is needed. The CPU is awakened on an interrupt, quickly executes the required functions with a 24MHz clock, and returns to sleep. A hardware interrupt handler is implemented with several interrupt levels in order to define high and low priority functions.

There are four additional CPU coprocessors: 1) an AES-128 crypto engine, 2) LOG2, 3) JLI_Rebase, and 4) a CRC calculator. Dedicated CPU instructions are defined to run AES encryption/decryption, calculate a log2() function, a function to help with rebasing the JLI table, and a function to calculate CRC values respectively.

FPU

The ARC also includes a Floating Point Unit (FPU) compliant with the IEEE 754-2008. FPU supports for all IEEE specified rounding modes

The FPU has single precision hardware support for multiply, add, subtract, integer/float conversions, compare, divide, and square root. All FPU operations are supported by the Metaware compiler for ARC EM4

Memories

Code memory is split to ROM, RAM and OTP and use is optimized for power consumption.

In sleep mode ROM can be shut off without losing its contents while RAM will lose its contents and needs to be reloaded. Therefore all critical functions for Bluetooth low energy controller and hostare implemented in the ROM.

48kB RAM is available for application and patch development. These can then be moved into OTP for production. The patching system is based on using instruction index tables and dedicated CPU instructions. All functions that are to be patched must use index table call. The index table is loaded from ROM into RAM and rebuilt during the boot process.

It is also rebuilt when waking from sleep mode if IRAM0 is not specified for retention.

28kB of RAM is provided for data. Either 4kB, 8kB, or 20kB of that data RAM can be specified as retention memory which is kept active during sleep mode at the expense of additional leakage current. Data in non-retention memory is lost during sleep mode.

128kB OTP is available for instructions or data. Trimming, configuration data, Bluetooth profiles and services, an application, and code patches can be installed into OTP during manufacturing or at a later time in the field using the over-the-air firmware (FOTA) updating mechanism. Code can be executed from OTP or copied to RAM for execution, whichever is more power efficient.

Table 3-1 Memories

Name	Type	Size	Usage	RAM Retention	Address Range
IROM	ROM	128KB	CPU program, boot, LL, Host	-	0x000000~0x01FFF F
IRAM1	SRAM	48KB	CPU program, to be l oaded from OTP or serial interface	N0	0x020000~0x02BFF F
IRAM0	SRAM	4KB	CPU instruction index table	Optional	0x030000~0x030FFF
OTP	OTP	128KB	CPU program, profiles, applications	N/A	0x100000~0x11FFFF
DRAM0	SRAM	4KB	CPU data, unique ID, co nfiguration	YES	0x800000~0x800FFF
DRAM1	SRAM	4KB	CPU data	Optional	0x801000~0x801FFF
DRAM2	SRAM	12KB	CPU data	Optional	0x802000~0x804FFF
DRAM3	SRAM	8KB	CPU data	N0	0x805000~0x806FFF
DROM	ROM	8KB	SW constants	-	0x808000~0x809FFF

Security

The security features are implemented in a combination of digital hard ware and software functions which are described in the table below. A hardware based true random number generator is implemented which complies with the NIST 800-90A standard. Packet encryption and decryption is implemented in hardware with an AES-128 core embedded in-line with the RF packet processor block which allows the operation to be performed on the fly. (A second AES-128 block is included for non-real-time operation.) Finally, the EEC P-256 function is implemented in software for key generation.

Table 3-2 Memories

Features	Bluetooth Specification	Implementation
Random data gene ration	Vol2, Part H, Section 2	True RNG based on logic Pseudo RNG: NIST, Recommendation f or Random Number Generation Using Deterministic Random Bit Genera

Features	Bluetooth Specification	Implementation
		tors, Special Publication 800-90A, January 2012 Variant with block cipher (AES)
Packet encryption and authentication	Vol6, Part E	HW block in RF IP packet processor with AES core embedded to compute MIC and encrypt/decrypt a packet on the fly
Key generation	Vol3, Part H, Section 2.4	Implemented in SW included ECC P-256 function

Peripherals

Peripherals supported by CPU include an I2C master, SPI master, UART, SPI slave, GPIO, and timers. The SPI slave includes flow control for maximum transfer efficiency. The I2C master and SPI master have 16 byte buffers. The reception (RX) and transmission of the UART slave and SPI slave have 64 byte FIFOs.

The device offers abundant resources, and different peripheral controllers can be realized. I/O resources support different level standards, offering multiple peripheral interfaces. For further detailed information, please refer to 3.4 IOB.

3.2.1 Bluetooth Module

Bluetooth Controller Mode

- Host connect to controller via Host Controller Interface (HCI)
- HCI interface implemented via SPI or UART transport layer
- Link layer implemented in ROM
- Up to 8 simultaneous connections supported
- Long packet lengths (payload up to 255 bytes) supported

Bluetooth Companion Mode

- Interface to host with proprietary Application Controller Interface (ACI)
- ACI interface implemented via SPI or UART transport layer
- Bluetooth 4.2 certified stack and standard profiles and services implemented in ROM
- Additional profiles and services can be loaded and stored in OTP
- Secure connections including key-exchange supported
- All other Controller Mode features supported except HCI

Bluetooth Application Mode

- Application hosting
  - Low energy applications such as proximity or sensor beacons using Bluetooth are easily implemented
  - Connections to digital peripherals through SPI, I2C, UART, and GPIOs allow for data collection, storage, or display for example.
  - All Controller Mode and Companion Mode features supported

3.2.2 Timers

Three types of timers are included in the system. The first timer is a 32-bit timer driven by the 32kHz crystal oscillator or low-frequency RC

oscillator (divided by 12) and is dedicated to the sleep function which controls when the CPU is woken up.The second timer is a 32-bit timer driven by the 48MHz crystal oscillator or 24/48MHz RC oscillator and used by the link layer for higher-speed protocol related timing. The third timer is a universal timer, which can be used by the application.

There are two universal timers with the following features:

- 32-bit up counter, selectable auto-reload
- clock source: system clock, GPIO
- 7-bit pre-scaler
- SW start/stop
- HW start/stop
- input capture on HW events (GPIO)
- input capture on SW event
- limit value
- compare value
- output to GPIO; maximal frequency 12MHz, minimal duty cycle 45/65
- interrupt on limit value, compare and input capture

3.2.3 Power Management

There is a sophisticated power management system in the chip. Power consumption and battery life are optimized under all working conditions. The memory architecture is divided into several different power domains for power consumption optimizations. When a memory is not being used, it can be switched off to reduce current consumption.

During Bluetooth connected sleep mode the entire MCU subsystem can be shut off and only the power management system and required state retention memories (if any) need to be powered. The power management system will properly wakeup the MCU subsystem when it is needed. The RF modem is also on a separate supply domain and is turned on and off as needed in order to minimize energy consumption.

Key low-power circuits include a configurable and highly-efficient DCDC converter, low noise bandgap references, low drop-out regulators (LDOs), a high frequency RC oscillator for efficient MCU operation, and a high accuracy, low frequency, RC oscillator for sleep mode control.

DC DC Switching Power Supply

The DCDC converter is a single-output, step-up/down converter with a simple bang-bang regulation. The output voltage is monitored with a supply voltage level detector (SVLD) circuit and the regulation is adjusted accordingly. In sleep mode, the DCDC converter is off but the output capacitor can optionally be kept charged.

Most common 1.5V and 3.0V primary battery cell technologies are directly supported including Lithium, Alkaline, Zinc-Air and Silver Oxide. For 1.5V batteries, the on-chip DCDC converter steps up the voltage to the required internal levels. For 3.0V batteries, the on-chip DCDC converter steps the voltage down internally for efficient power consumption. Very few external components are necessary for the DCDC converter operation; however, it is also possible to operate without the converter or using an external converter to minimize component count even further.

The power management can be configured in several different modes:

- In DCDC Step-Down Configuration, the battery is connected to VBAT1 and VBAT2. The DCDC switching output is connected to VCC.
- In DCDC Step-Up Configuration, the battery is connected to VCC, and VBAT2.The DCDC switching output is connected to VBAT1.
- In DCDC Off Configuration, the battery is connected VBAT1, and VBAT2. The DCDC switching output is connected to ground, and VCC is connected to a 2.2µF decoupling capacitor. There is a dedicated linear regulator (LDO VCC) between VBAT1 and VCC which creates 1.25V on VCC.
- In External-DCDC Configuration, the battery is connected to pads VBAT2, and VCC. The DCDC switching output is connected to ground, and VBAT1 is connected to an externally supplied voltage with a minimal level of 2.6V.

Supply Monitoring

The power management configuration is automatically detected by the power management logic and setup appropriately. This is accomplished with use of an internal supply voltage level detector (SVLD) that can be applied to the following supply domains: VBAT1, VCC, AVDD_RF (internal RF supply), and SW_DCDC. The SVLD supply domains are described in the table below. VBAT1 is used to monitor the battery voltage in DCDC Step-Down Configuration or the DCDC control loop in DCDC Step-Up Configuration. VCC is used to monitor the battery voltage in DCDC Step-Up Configuration or the DCDC control loop in DCDC Step-Down Configuration. AVDD_RF is used to monitor the voltage on the RF IP. In case of low-voltage an event is issued.

Table 3-3 SVLD Supply Domains

Supply	Range	Step	Comment/Configuration
VBAT1	1.9V~3.4V	100mV 4bits	Used for battery voltage monitoring Step-Down, DCDC Off: battery monitoring Step-Up: DCDC control loop External DCDC: DCDC voltage monitor
VCC	0.95~1.7V	100mV 4bits	“0010” → 1.05V Step-Up, External-DCDC: battery monitoring Step-Down: DCDC control loop DCDC Off: LDO voltage monitor
AVDD_RF	0.94V, 0.99V	1bit	Used for RF supply monitoring CPU will use the information to inform Host about battery level

3.2.4 RF Description

The RF modem is also on a separate supply domain and is turned on and off as needed in order to minimize energy consumption. The RF transceiver exceeds the specifications and requirements of the Bluetooth 5.0 PHY specification.

The main features of the RF transceiver are the following:

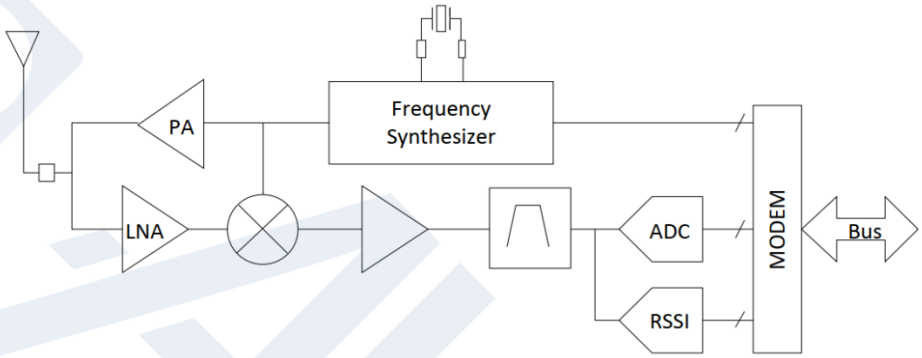
- Ultra-low-power: The peak current in receive mode is 3.0 mA and in transmit mode is 5.2mA at 0.4dBm and 3.0V in DCDC Step-Down

Configuration at room temperature.

- Excellent RF performance: including -94dBm sensitivity for 1Mbps operation with 37 byte payload and a programmable output power range from -34dBm to +6.1dBm
- Low-voltage: Operation from 3.6V down to 1.05V
- Very high degree of integration: small footprint with few external components

The RF transceiver block diagram is shown in the figure below.

Figure 3-2 RF Transceiver Block Diagram



The RF transceiver is based on a low-IF architecture and comprises the following building blocks:

- Single-ended 50 Ohm RF port with on-chip harmonic filter
- High gain, low power, LNA and mixer
- Power Amplifier with programmable output power range
- Low-IF receiver with 5th order channel filter and ADC converter
- Fully integrated frequency synthesis with fast settling time and digital modulation
- 48MHz XTAL reference with finely trimmable internal loading capacitor

3.2.5 Operating Modes

Operating modes are designed to optimize the power consumption during operation, as shown in the table below.

Table 3-4 Operating Modes

Mode	VDD supply	Clock	Description
Active RC (active mode)	Full, high load DC/DC on	RC 48MHz	CPU enabled, logic power domains co ntrolled by CPU
Active XTAL (active mode)	Full, high load DC/DC on	XTAL 48MHz	CPU enabled, logic power domains co ntrolled by CPU, RF controlled by CPU
Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered-down; VCC optionally c harged (on by default) DCCM0 and optionally DCCM1, DCC M2, and ICCM0 in retention mode LF RC oscillator with normal precision, PML clock reduced to 250kHz
Deep Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered down, VCC not charged DCCM0 and optionally DCCM1, DCC M2, and ICCM0 in retention mode LF RC oscillator in low precision opera tion, PML clock reduced to 250kHz
Chip Disable	None	None	Chip disabled

When the CPU is active, two modes are possible. Active RC mode is used with a high-frequency (HF) RC oscillator for fast turn-on and turn-off performance. This can be used to service the peripherals, for example. When the RF is required, active XTAL mode is used with a high- accuracy crystal oscillator for channel frequency precision required by the RF standards. The crystal oscillator takes longer to turn on than the RC oscillator and more energy is consumed when in use.

In the sleep and deep sleep modes, the sleep timer clock (device timing reference) can be connected either to the digitally calibrated RF low-frequency (LF) RC oscillator or to the low-frequency crystal (LF XTAL) oscillator. If the LF crystal oscillator is used, the LF RC oscillator is switched to a relaxed mode with less supply current and less accuracy. LF RC runs all the time since it is used for the power management logic. The LF crystal option brings higher clock accuracy (about 10 times), which requires a shorter RF window in time for TDMA functions, hence lower average current. However, it requires an external crystal component. SoC current is 650nA during deep sleep mode.

Chip disable mode is provided as the lowest power mode possible with the battery voltage still applied to the IC but all functions are disabled. SoC current is only 5nA at this time.

3.2.6 Software Development

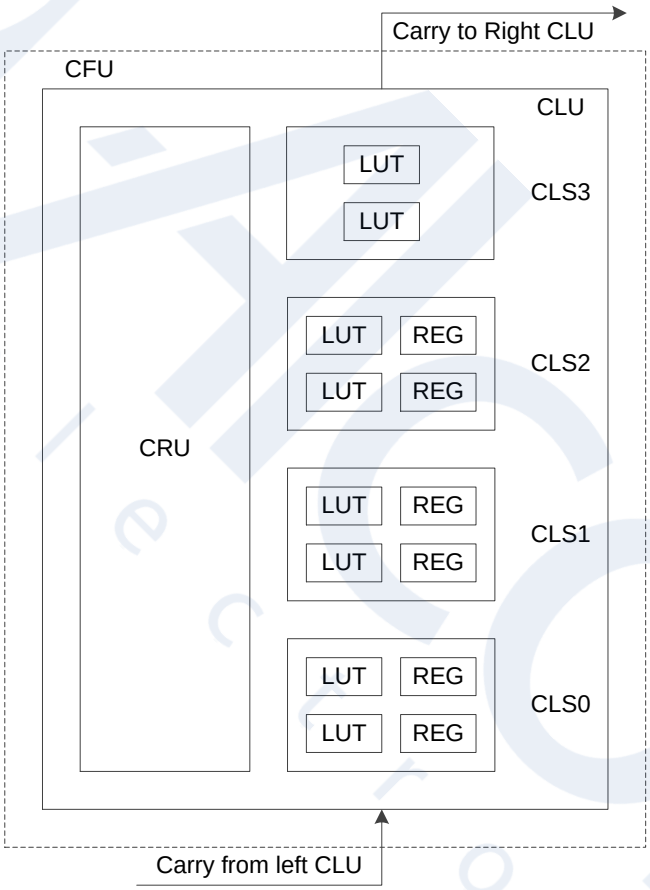
The ARC processor supports a full range of software development tools, including compilers, linkers, debuggers, and free GCC tools.Using the integrated software development environment IDE and the software development kit SDK, users can easily link to functions in ROM, implement patches, implement functions in RAM or OTP, and execute programs from

RAM or OTP. Supports JTAG interface development, debugging and download.

3.3 Configurable Function Unit

Configurable Function Unit (CFU) is the base cell for the array of GW1NRF series of Bluetooth FPGA Products. Each CFU consists of a Configurable Logic Unit (CLU) and its routing resource Configurable Routing Unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-3 below.

Figure 3-3 CFU View



3.3.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four input LUT. A higher input number of LUT can be formed by combining LUT4 together.

- Each CLS can form one five input LUT5.
- Two CLSs can form one six input LUT6.
- Four CLSs can form one seven input LUT7.

- Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

- Adder and subtractor
- Up/down counter
- Comparator, including greater-than, less-than, and not-equal-to
- MULT
- Multiplier

Register

Each configurable logic slice (CLS0~CLS2) has two registers (REG), as shown in Figure 3-4 below.

Figure 3-4 Register in CLS

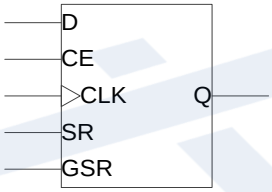


Table 3-1 Register Description in CLS

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1NRF series of Bluetooth FPGA products, GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

3.3.2 CRU

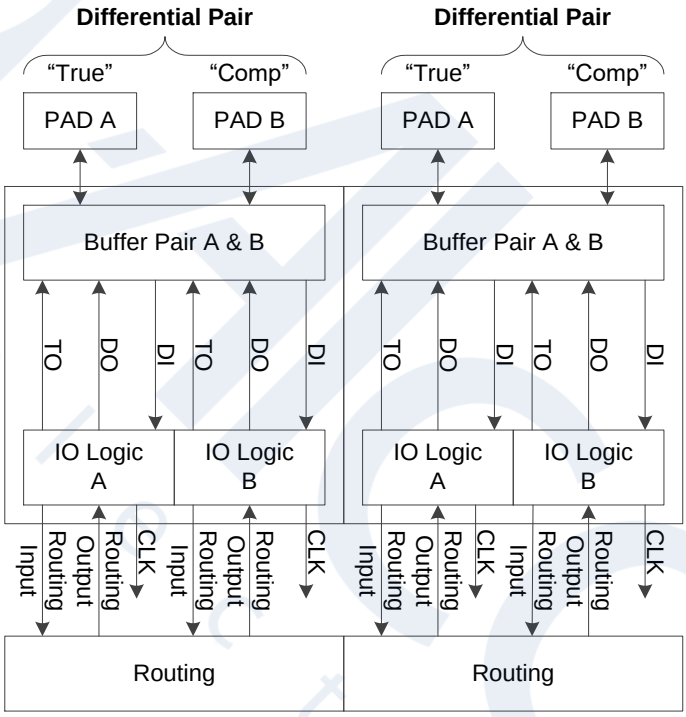
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.4 IOB

The IOB in the GW1NRF series of Bluetooth FPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-5, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

Figure 3-5 IOB Structure View



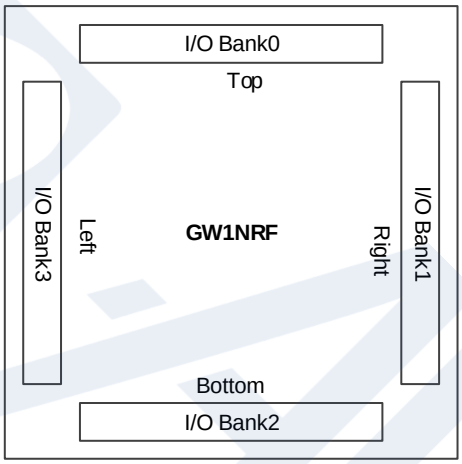
IOB Features:

- V_{CCO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode

3.4.1 I/O Buffer

There are four IO Banks in the GW1NRF series of Bluetooth FPGA products, as shown in Figure 3-6. To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x V_{CCO}) or the external reference voltage using any IO from the bank.

Figure 3-6 GW1NRF I/O Bank Distribution



The GW1NRF series of Bluetooth FPGA products support LV and UV.

LV devices support 1.2V V_{CC} to meet users' low power needs.

V_{CCO} of LV devices can be set as 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V according to requirements[1].

Linear voltage regulator is integrated in UV devices to facilitate single power supply. The core voltage supports 1.8V, 2.5V, and 3.3V.

V_{CCX} supports 2.5 V or 3.3 V power supply.

Note!

- By default, the systemIO is weak pull-up for blank chips.
- For the recommended working conditions for different packages, please refer to 4.1Operating Conditions

For the V_{CCO} requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS33	Single end	3.3	4,8,12,16,24
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25
RSDS	Differential	2.5/3.3	2
MINILVDS	Differential	2.5/3.3	2
PPLVDS	Differential	2.5/3.3	3.5
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8
MIPI	Differential	TBD	TBD

Table 3-3 Output I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
MIPI	Differential	TBD	TBD	TBD

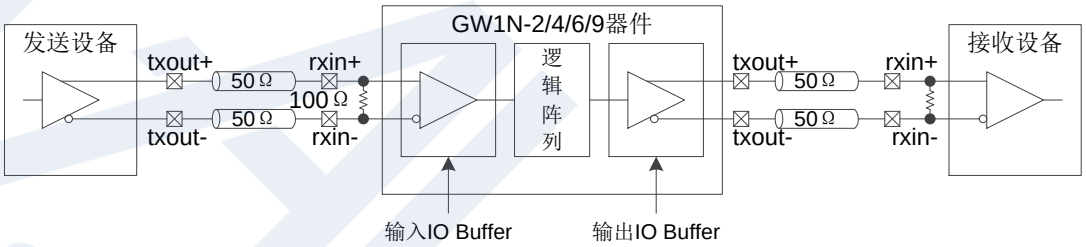
3.4.2 True LVDS Design

BANK1/2/3 in the GW1NRF devices support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistance. Bank0 supports internal 100Ω input differential matched resistance. BANK 0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E,etc. For the detailed information on different levels, please refer to *Gowin systemIO* User Guide.

For more detailed information on true LVDS, please refer to *GW1NRF-4B Pinout*.

True LVDS input I/O needs external 100Ω terminal resistance for matching. SeeFigure 3-7 for the true LVDS design.

Figure 3-7 True LVDS Design



For more detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistance, please refer to *Gowin SystemIO User Guide*.

3.4.3 I/O Logic

Figure 3-8 shows the I/O logic output of the GW1NRF series of Bluetooth FPGA products.

Figure 3-8 I/O Logic Output

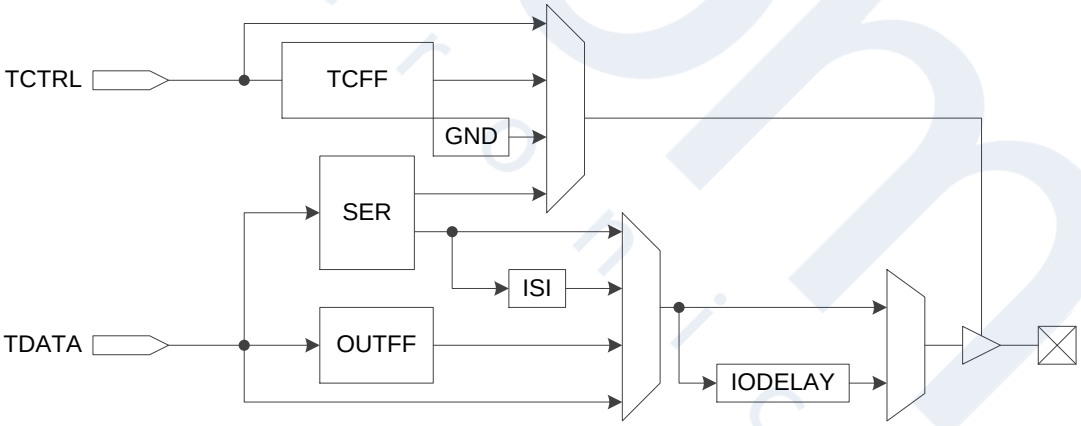
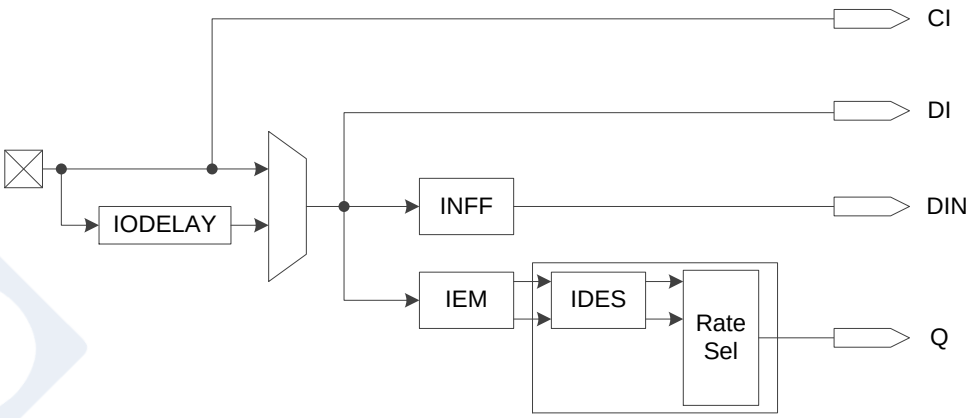


Figure 3-9 shows the I/O logic input of the GW1NRF series of Bluetooth FPGA products.

Figure 3-9 I/O Logic Input

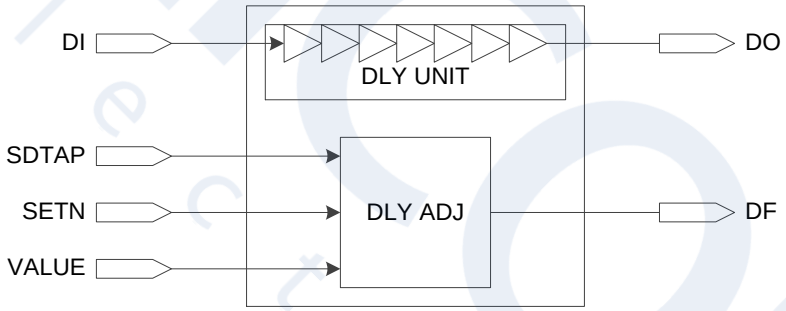


A description of the I/O logic modules of the GW1NRF series of Bluetooth FPGA products is presented below:

IODELAY

See Figure 3-10 for an overview of the IODELAY. Each I/O of the GW1NRF series of Bluetooth FPGA products has an IODELAY cell. The longest delay it can provide is about 128 steps x 30ps = 3840ps.

Figure 3-10 IODELAY



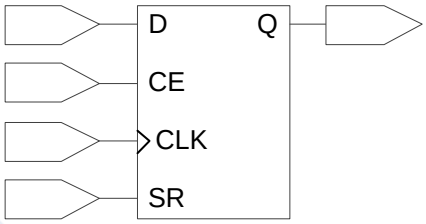
The delay cell can be controlled in two ways:

- Static control:
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure Figure 3-11 for the I/O register in the GW1NRF series of Bluetooth FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

Figure 3-11 Register Structure in I/O Logic



Note!

- CE can be either active low (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-12 for the IEM structure.

Figure 3-12 IEM Structure

De-serializer DES and Clock Domain Transfer

The GW1NRF series of Bluetooth FPGA products provides a simple serializer SER for each output I/O to support advanced I/O protocols.

Serializer SER

The GW1NRF series of Bluetooth FPGA products provides a simple serializer (SER) for each output I/O to support advanced I/O protocols.

3.4.4 I/O Logic Modes

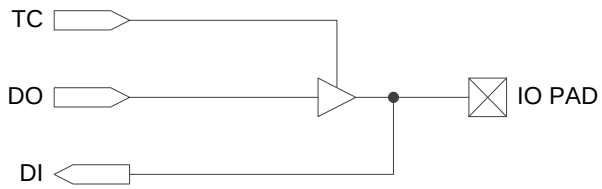
The I/O Logic in the GW1NRF series of Bluetooth FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

Not all the device pins support I/O logic. The pins IOL10 (A, B, C ... .J) and IOR10 (A, B, C ..., J) of GW1NRF-4/GW1NRF-4B do not support IO logic. All GW1NRF-9 pins support IO logic.

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-13, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

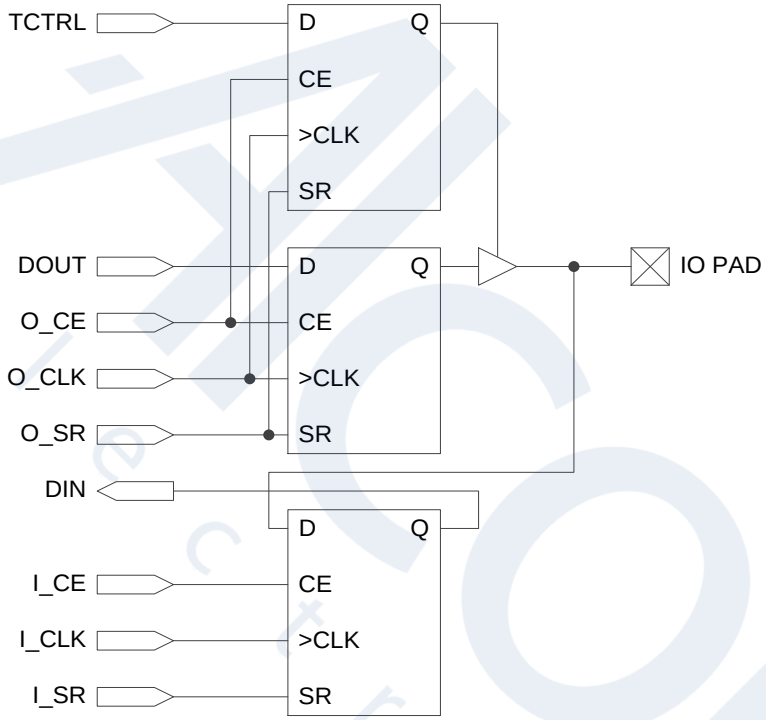
Figure 3-13 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-14. This can effectively improve IO timing.

Figure 3-14 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

Higher speed I/O protocols can be supported in generic DDR mode. GW1NRF-9 devices support IDES16 mode and OSER16 mode. The other devices do not support.

Figure 3-15 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

Figure 3-15 I/O Logic in DDR Input Mode

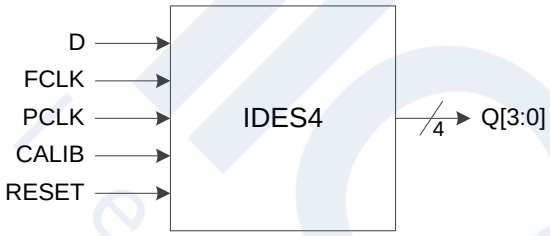
Figure 3-16 shows the generic DDR output, with a speed ratio of the PAD to FPGA internal logic 2:1.

Figure 3-16 I/O Logic in DDR Output Mode

IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

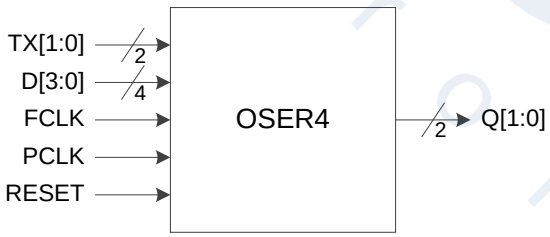
Figure 3-17 I/O Logic in IDES10 Mode



OSER4 Mode

In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

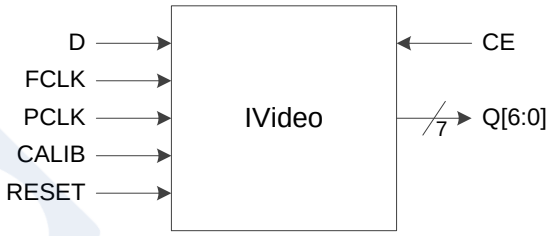
Figure 3-18 I/O Logic in OSER4 Mode



IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

Figure 3-19 I/O Logic in IVideo Mode



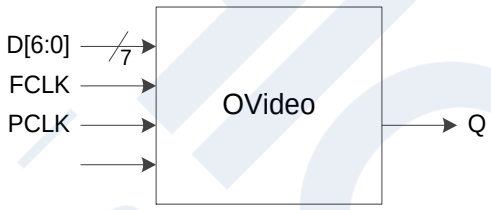
Note!

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

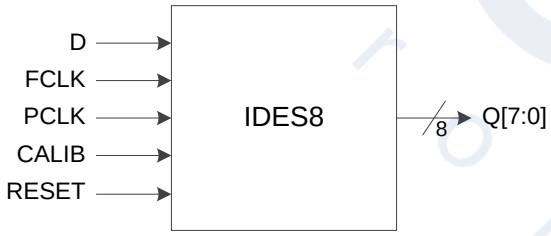
Figure 3-20 I/O Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

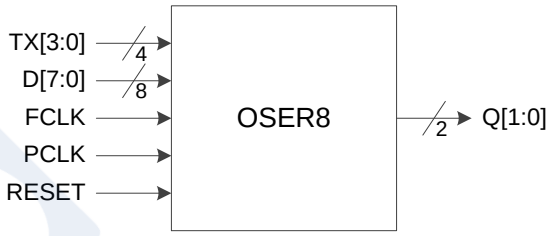
Figure 3-21 I/O Logic in IDES8 Mode



OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

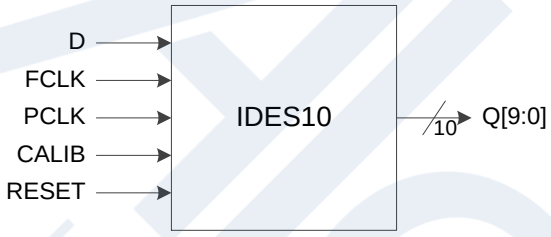
Figure 3-22 I/O Logic in OSER8 Mode



IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

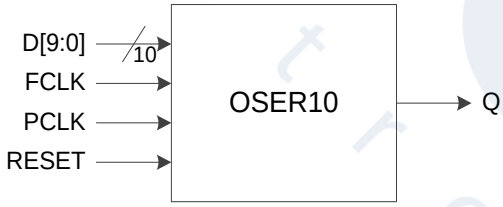
Figure 3-23 I/O Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

Figure 3-24 I/O Logic in OSER10 Mode



3.5 Block SRAM (B-SRAM)

3.5.1 Introduction

GW1NRF series FPGA products provide abundant SRAM. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array. Each B-SRAM has 18,432 bits (18Kbits). There are five operation modes: single port, dual port, semi-dual port, ROM, and FIFO. The signals and functional descriptions of B-SRAM are listed in Table 3-4.

An abundance of B-SRAM resources provide a guarantee for the

user's high-performance design. B-SRAM features include the following:

- Max.18,432 bits per B-SRAM
- B-SRAM itself can run at 190 MHz at max
- Single port
- Dual port
- Semi-dual port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Asynchronous reset, synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A address
ADB	I	Port B address
CEA	I	Clock enable, Port A
CEB	I	Clock enable, Port B
RESETA	I	Register reset, Port A
RESETB	I	Register reset, Port B
WREA	I	Read/write enable, Port A
WREB	I	Read/write enable, Port B
BLKSEL	I	Block select
CLKA	I	Read/write cycle clock for Port A input registers
CLKB	I	Read/write cycle clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

3.5.2 Configuration Mode

The B-SRAM mode in the GW1NRF series of Bluetooth FPGA products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

3.5.3 Mixed Data Bus Width Configuration

B-SRAM in the GW1NRF series of Bluetooth FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-6 and Table 3-7 below.

Table 3-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*" denotes the modes supported.

Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*" denotes the modes supported.

3.5.4 Byte-enable

The B-SRAM in the GW1NRF series of Bluetooth FPGA products supports byte-enable. For data longer than a Byte, the additional bits can be blocked, and only the selected portion is allowed to be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write operation.

3.5.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used as a parity bit or for data storage. However, the parity operation is not yet supported.

3.5.6 Synchronous operation

- All the input registers of B-SRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

3.5.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.5.8 Operation Modes

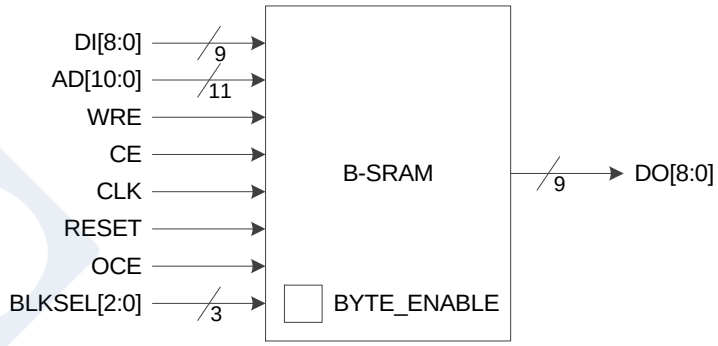
The input registers of B-SRAM can be used for synchronous write. The output registers can be used as pipeline register to improve design performance. In the dual port mode, the two ports of B-SRAM can be operated totally independently. Port A and Port B have their own clock and are write-enabled; as such, both ports can be written to and read independently from each other.

Single Port Mode

In the single port mode, as shown below, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal write mode (Normal-write Mode)

and write-through mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge. For the single port 2 K x 9 bits block memory, see Figure 3-25 below.

Figure 3-25 Single Port Block Memory



The table below shows all the configuration options that are available in the single port mode:

Table 3-8 Single Port Block Memory Configuration

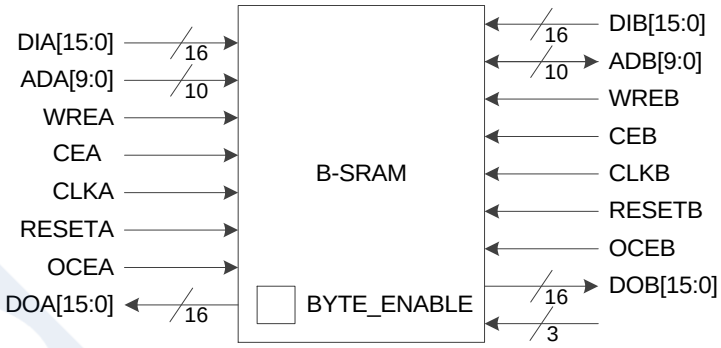
Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SP	B-SRAM_16K_S1	16K	16K x 1	16,384	1
	B-SRAM_8K_S2	16K	8K x 2	8,192	2
	B-SRAM_4K_S4	16K	4K x 4	4,096	4
	B-SRAM_2K_S8	16K	2K x 8	2,048	8
	B-SRAM_1K_S16	16K	1K x 16	1,024	16
	B-SRAM_512_S32	16K	512 x 32	512	32
SPX9	B-SRAM_2K_S9	18K	2K x 9	2,048	9
	B-SRAM_1K_S18	18K	1K x 18	1,024	18
	B-SRAM_512_S36	18K	512 x 36	512	36

Dual Port Mode

B-SRAM support dual port mode, as shown in Figure 3-26. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

Figure 3-26 Dual Port Block Memory



All the configuration options for the dual port mode are as shown in Table 3-9 .

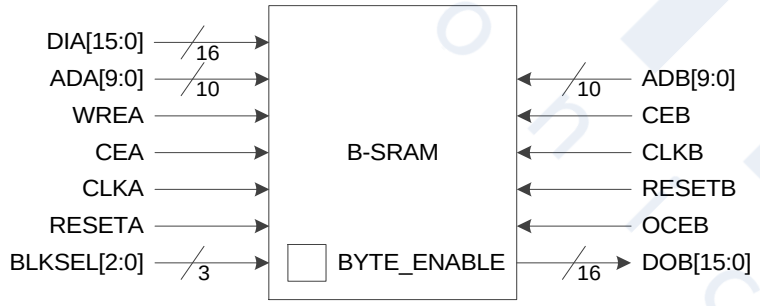
Table 3-9 Dual Port Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
DP	B-SRAM_16K_D1	16K	16K x 1	16384	1
	B-SRAM_8K_D2	16K	8K x 2	8192	2
	B-SRAM_4K_D4	16K	4K x 4	4096	4
	B-SRAM_2K_D8	16K	2K x 8	2048	8
	B-SRAM_1K_D16	16K	1K x 16	1024	16
DPX9	B-SRAM_2K_D9	18K	2K x 9	2048	9
	B-SRAM_1K_D18	18K	1K x 18	1024	18

Semi-Dual Port Mode

The figure below shows the semi Dual Port 1K x 16bit mode. It supports read and write at the same time on different ports. It is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

Figure 3-27 Semi Dual Port Block Memory



All the configuration options for the dual port mode are as shown in Table 3-10.

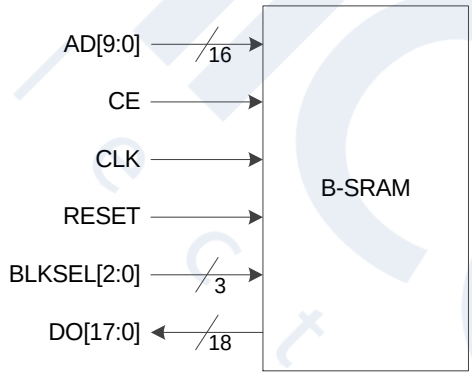
Table 3-10Semi Dual Port Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SDP	B-SRAM_16K_SD1	16K	16K x 1	16,384	1
	B-SRAM_8K_SD2	16K	8K x 2	8,192	2
	B-SRAM_4K_SD4	16K	4K x 4	4,096	4
	B-SRAM_2K_SD8	16K	2K x 8	2,048	8
	B-SRAM_1K_SD16	16K	1K x 16	1,024	16
	B-SRAM_512_SD32	16K	512 x 32	512	32
SDPX9	B-SRAM_2K_SD9	18K	2K x 9	2,048	9
	B-SRAM_1K_SD18	18K	1K x 18	1,024	18
	B-SRAM_512_SD36	18K	512 x 36	512	36

Read Only

B-SRAM can be configured as ROM, as shown in Figure 3-28. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Figure 3-28 ROM Block Memory



Each B-SRAM can be configured as one 16 Kbits ROM. Table 3-11 lists all the configuration options for the ROM mode.

Table 3-11 Block ROM Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
ROM	B-SRAM_16K_O1	16K	16K x 1	16,384	1
	B-SRAM_8K_O2	16K	8K x 2	8,192	2
	B-SRAM_4K_O4	16K	4K x 4	4,096	4
	B-SRAM_2K_O8	16K	2K x 8	2,048	8
	B-SRAM_1K_O16	16K	1K x 16	1,024	16
	B-SRAM_512_O32	16K	512 x 32	512	32
ROMX9	B-SRAM_2K_O9	18K	2K x 9	2,048	9
	B-SRAM_1K_O18	18K	1K x 18	1,024	18
	B-SRAM_512_O36	18K	512 x 36	512	36

Note!

In the ROM mode, the RESET signal can only reset the input and output registers. It cannot clear the ROM content.

3.5.9 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the B-SRAM via output registers or without using the registers.

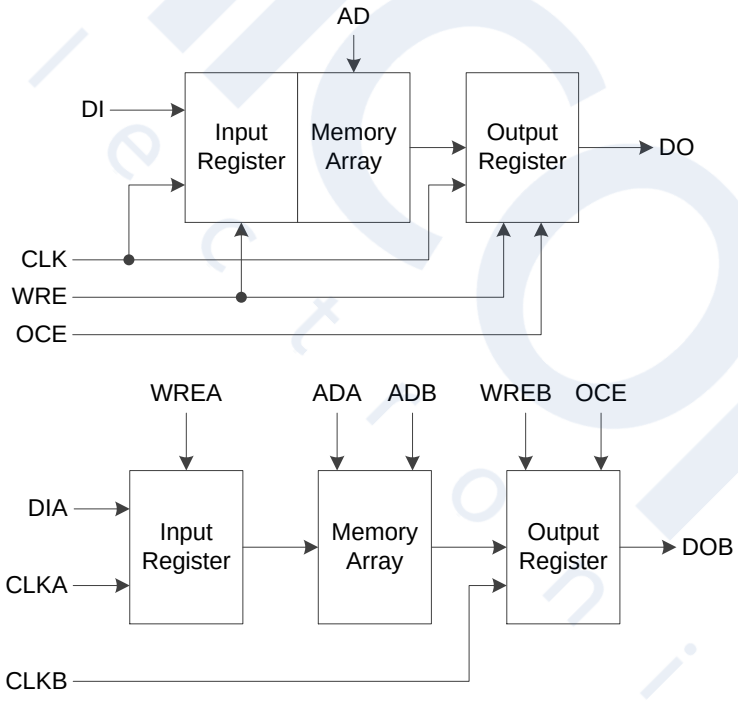
Pipeline Mode

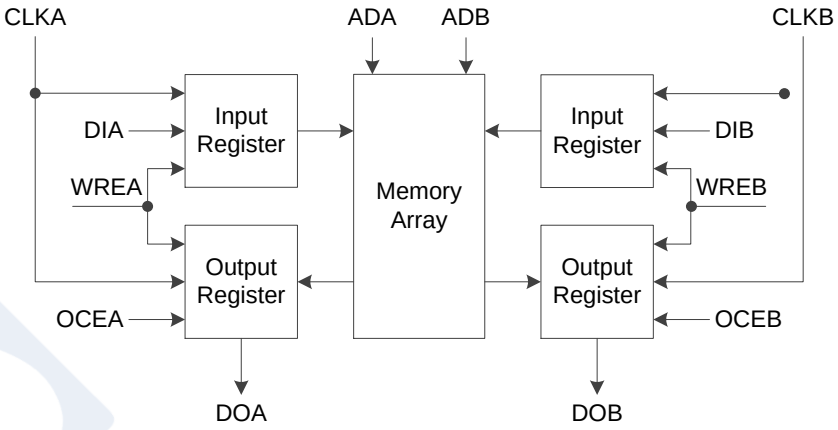
While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of the memory array.

Figure 3-29 Pipeline Mode in Single Port, Dual Port and Semi Dual Port





Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.5.10 Clock Operations

Table 3-12 lists the clock operations in different B-SRAM modes:

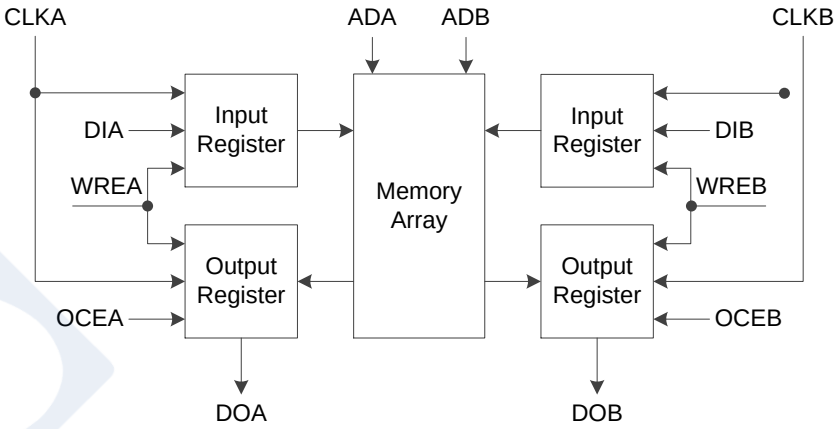
Table 3-12 Clock Operations in Different B-SRAM Modes

Clock Operations	Dual Port Mode	Semi-dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-30 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

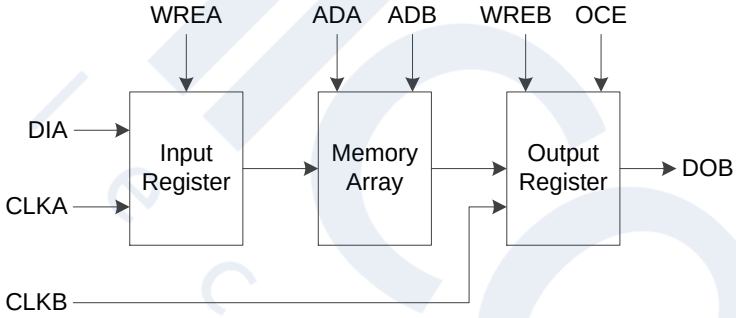
Figure 3-30 Independent Clock Mode



Read/Write Clock Operation

Figure 3-31 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB)controls Port B data output, read address, and read enable signals.

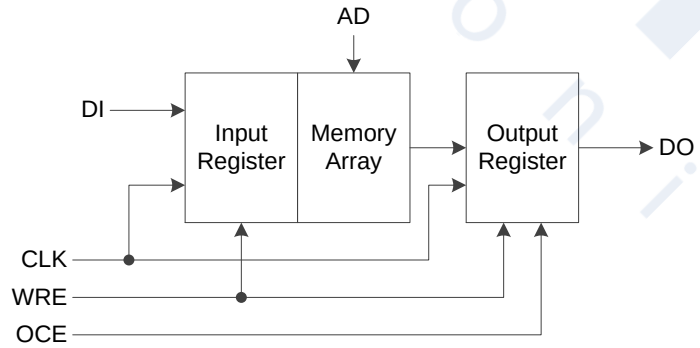
Figure 3-31 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-32shows the clock operation in single port mode.

Figure 3-32 Single Port Clock Mode



3.6 User Flash

3.6.1 Introduction

The GW1NRF series of Bluetooth FPGA products support User Flash. The features are as following:

- 10,000 write cycles
- Greater than10 years data retention at +85 ℃
- Page erase capability: 2,048 bytes per page
- Fast page erasure/word programming operation
- Clock frequency: 40 MHz
- Word programming time:≤16 μs
- Page erasure time:≤120 ms
- Electric current
  - Read current/duration:2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX)
  - Program/erase operation: 12/12 mA(MAX)

3.6.2 User Flash Ports

Figure 3-33 GW1NRF User Flash Ports

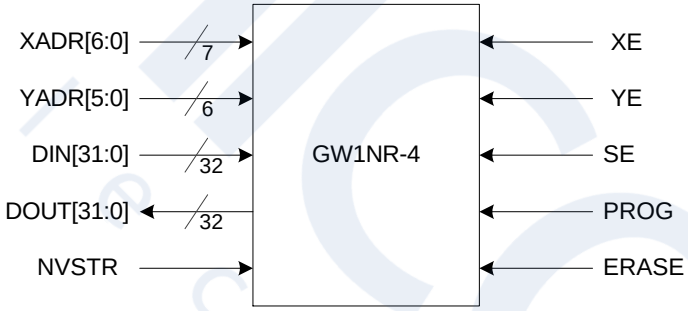


Table 3-13 Flash Module Signal Description

Pin name1	I/O	Description
XADR[n:0][2]	I	n=6, X address bus, used to access the row address. XADR[n:3] is used to select one page. XADR[2:0] is used to select one row within a page of main memory block. One page consists of eight rows, and one row consists of 64 columns.
YADR[5:0][2]	I	Y address bus, used to select one column within a row of memory block.
DIN[31:0]	I	Data input bus.
DOUT[31:0]	O	Data output bus.
XE[2]	I	X address enable signal, if XE is 0, all of row addresses are not enabled.
YE[2]	I	Y address enable signal, if YE is 0, all of column addresses are not enabled.
SE[2]	I	Detect amplifier enable signal, active high.
ERASE	I	Erase port, active-high.
PROG	I	Programming port, active-high.

Pin name1	I/O	Description
NVSTR	I	Flash data storage port, active-high.

Note!

- [1] Port names of Control, address,and data signals;
- [2] The read operation is valid only if XE = YE = V_{CC} and SE meets the pulse timing requirements (T_{pws}, T_{nws}). The address of read data is determined by XADR [5: 0] and YADR [5: 0].

3.6.3 User Flash Mode Truth Table

User Modes

Table 3-14 Truth Table in User Mode

Mode	XE	YE	SE	PROG	ERASE	NVSTR
Read mode	H	H	H	L	L	L
Programming mode	H	H	L	H	L	H
Page erasure mode	H	L	L	L	H	H

Note!

"H" and "L" means high level and low level of VCC.

3.7 DSP

3.7.1 Introduction

The GW1NRF series of Bluetooth FPGA products have abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

Macro

DSP blocks are embedded as a row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macro, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Figure 3-34 shows the structure of one Macro:

Figure 3-34 DSP Macro

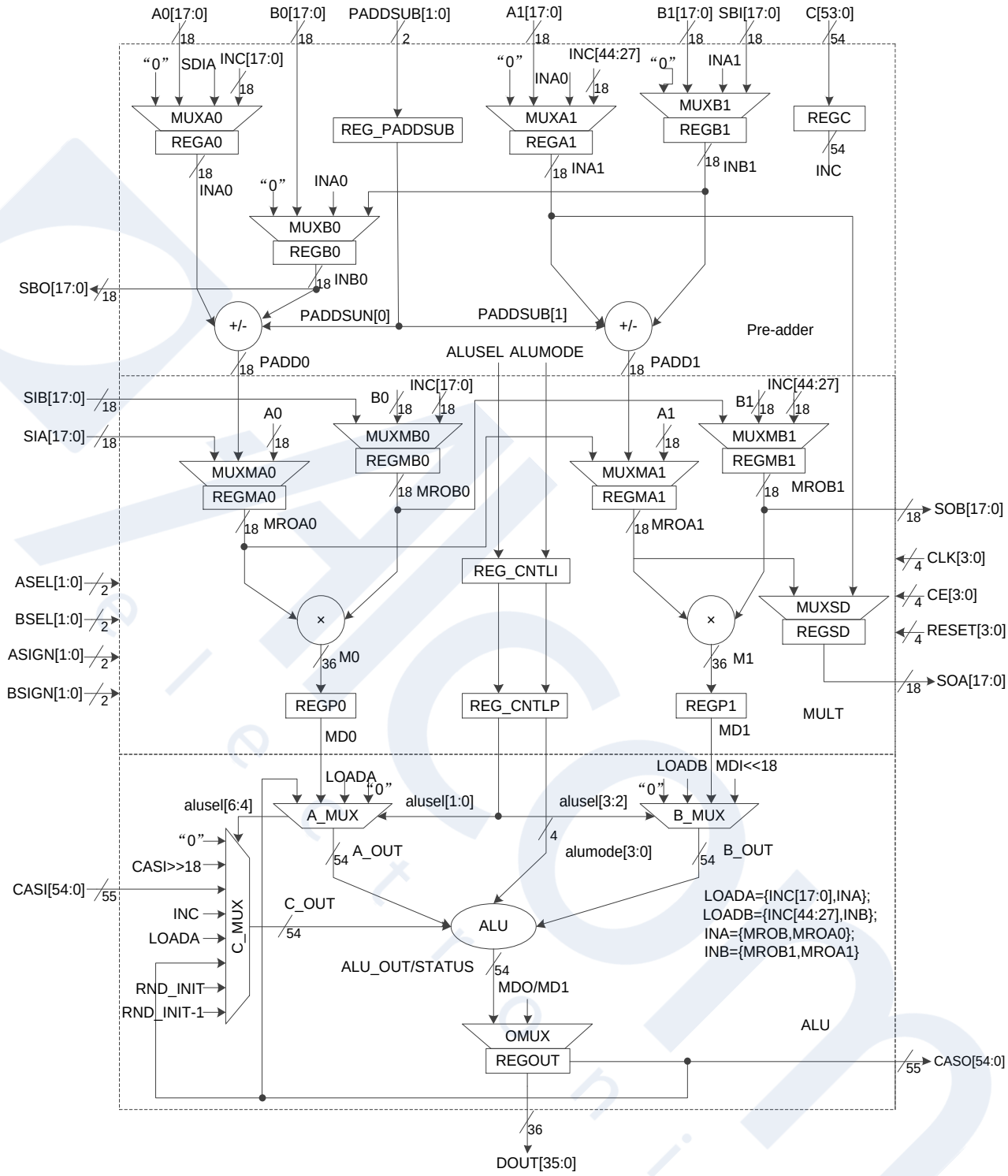


Table 3-15 shows DSP ports description.

Table 3-15 DSP Ports Description

Port Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0
A1[17:0]	I	18-bit data input A1
B1[17:0]	I	18-bit data input B1

Port Name	I/O	Description
C[53:0]	I	54-bit data input C
SIA[17:0]	I	Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle.
SIB[17:0]	I	Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle.
SBI[17:0]	I	Pre - adder logic shift input, backward direction.
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection.
PADDSI0[1:0]	I	Source select for Multiplier or pre-adder input A
BSEL[1:0]	I	Source select for Multiplier input B
ASIGN[1:0]	I	Sign bit for input A
BSIGN[1:0]	I	Sign bit for input B
PADDSUB[1:0]	I	Operation control signals of pre-adder, used for pre-adder logic add/subtract selection
CLK[3:0]	I	Clock input
CE[3:0]	I	Clock Enable
RESET[3:0]	I	Reset input, synchronous or asynchronous
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B
SBO[17:0]	O	Pre - adder logic shift output, backward direction.
DOUT[35:0]	O	DSP output data
CASO[54:0]	O	ALU output to next DSP block for cascade connection, the highest bit is sign-extended.

Table 3-16 Internal Registers Description

Register	Description and Associated Attributes
A0 register	Registers for A0 input
A1 register	Registers for A1 input
B0 register	Registers for B0 input
B1 register	Registers for B1 input
C register	C register
P1_A0 register	Registers for A0 input of left multiplier
P1_A1 register	Registers for A1 input of right multiplier
P1_B0 register	Registers for B0 input of left multiplier
P1_B1 register	Registers for B1 input of right multiplier
P2_0 register	Registers for pipeline of left multiplier
P2_1 register	Registers for pipeline of right multiplier
OUT register	Registers for DOUT output
OPMODE register	Registers for operation mode control
SOA register	Registers for shift output at port SOA

PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs:

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

Each input end supports pipeline mode and bypass mode. GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

MULT

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Pipeline Mode and Bypass Mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two adjacent DSP macros can form a 36 x 36 multiplier.

ALU

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. Registered Mode and Bypass Mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

3.7.2 DSP Operations

- Multiplier
- Accumulator
- MULTADDALU

3.8 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1NRF series of Bluetooth FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW1NRF series of Bluetooth FPGA products provide high-speed clock HCLK. PLL, DLL, etc are also provided.

3.8.1 Global Clock

The GCLK is distributed in GW1NRF series of Bluetooth FPGA products as two quadrants, L and R. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure 3-35 GW1NRF-4B Clock Resources

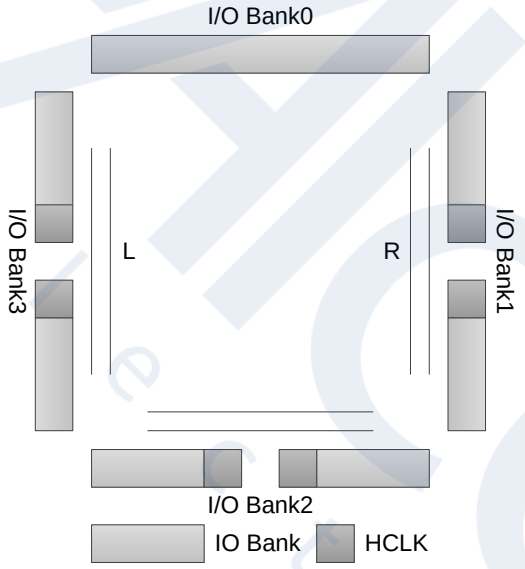
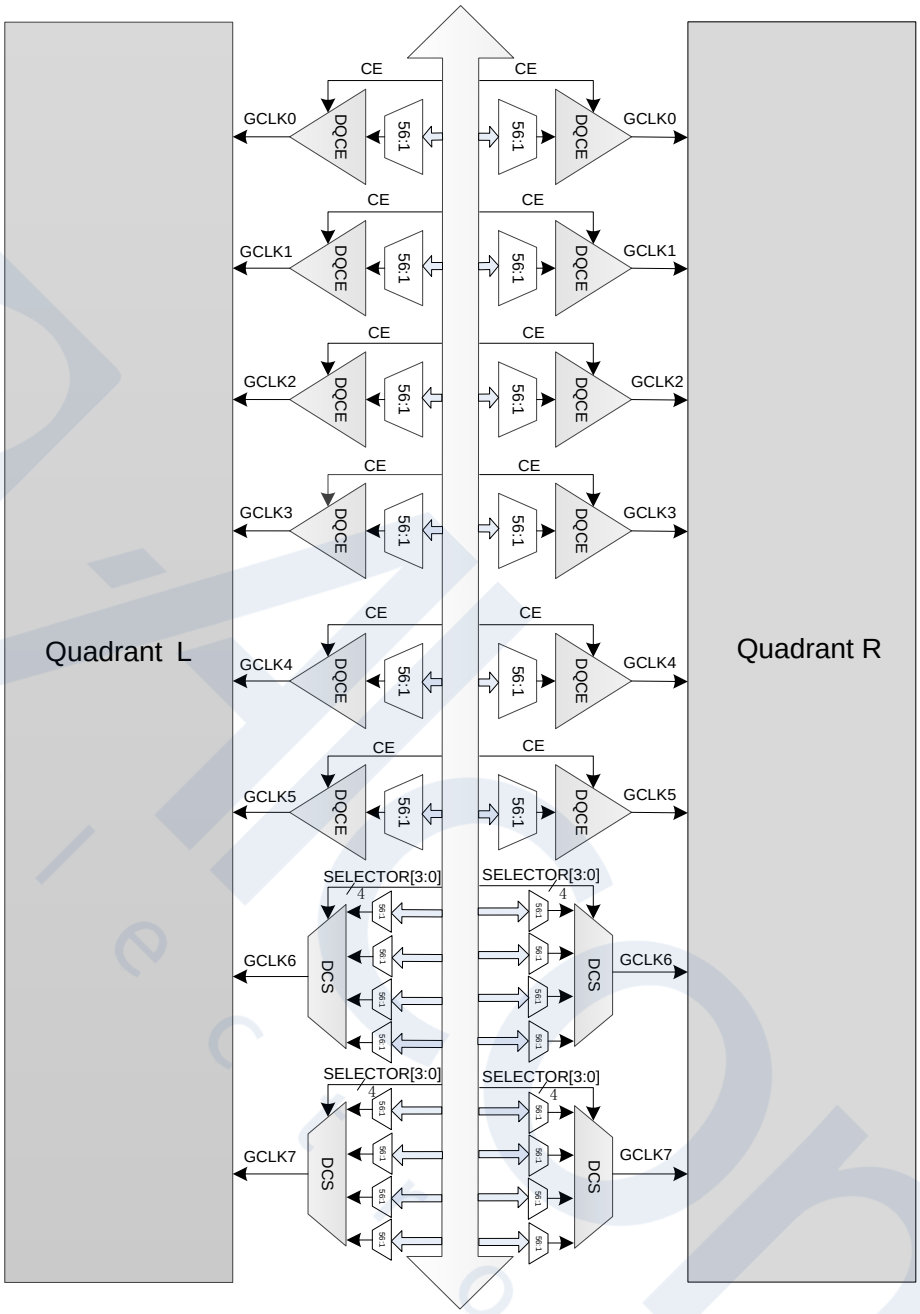
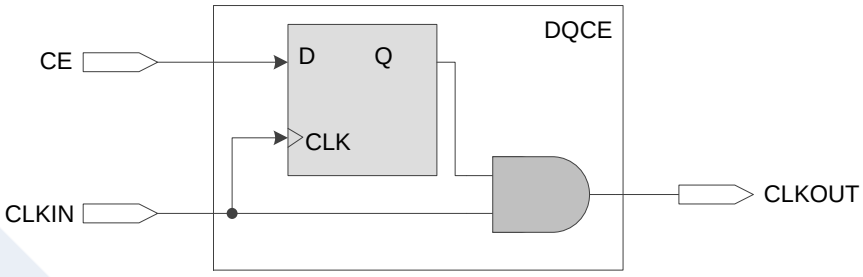


Figure 3-36 GCLK Quadrant Distribution



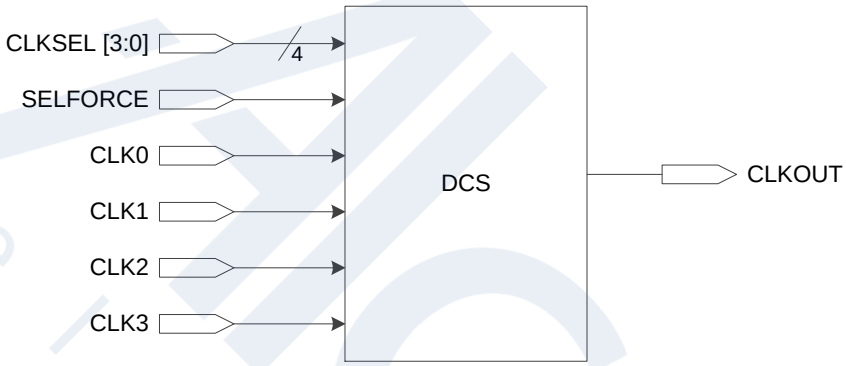
GCLK0~GCLK5 can be turned on or off by dynamic quadrant clock enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-37 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-38. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-38 DCS Concept

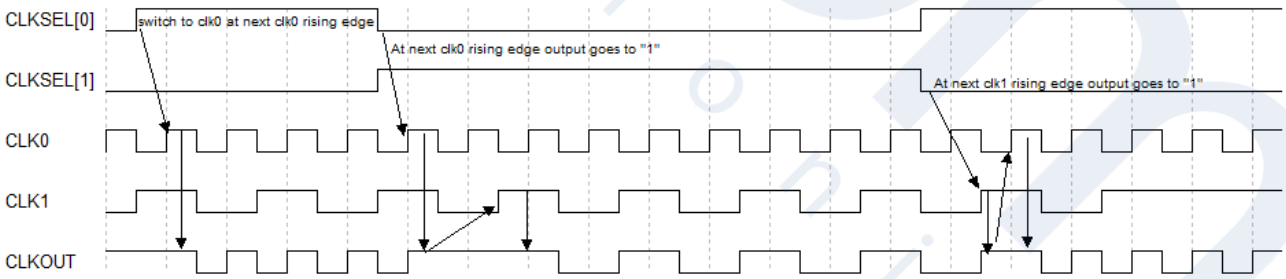


DCS can be configured in the following modes:

1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-39.

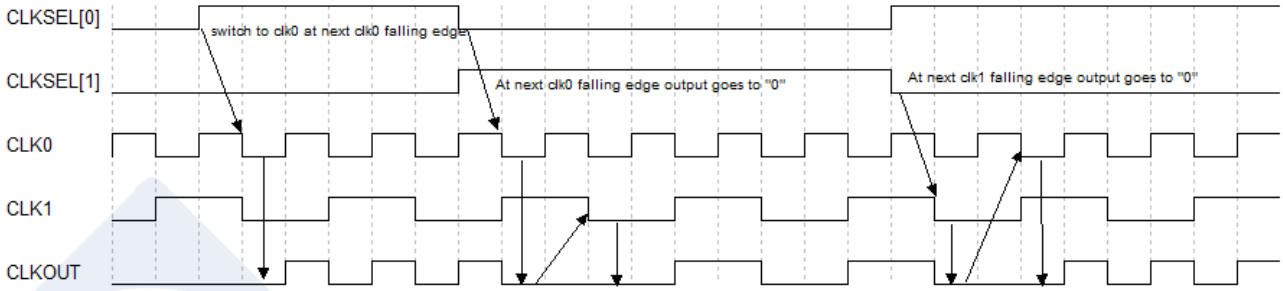
Figure 3-39 DCS Rising Edge



2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-40.

Figure 3-40 DCS Falling Edge



3. Clock Buffer Mode

   In this mode, DCS acts as a clock buffer.

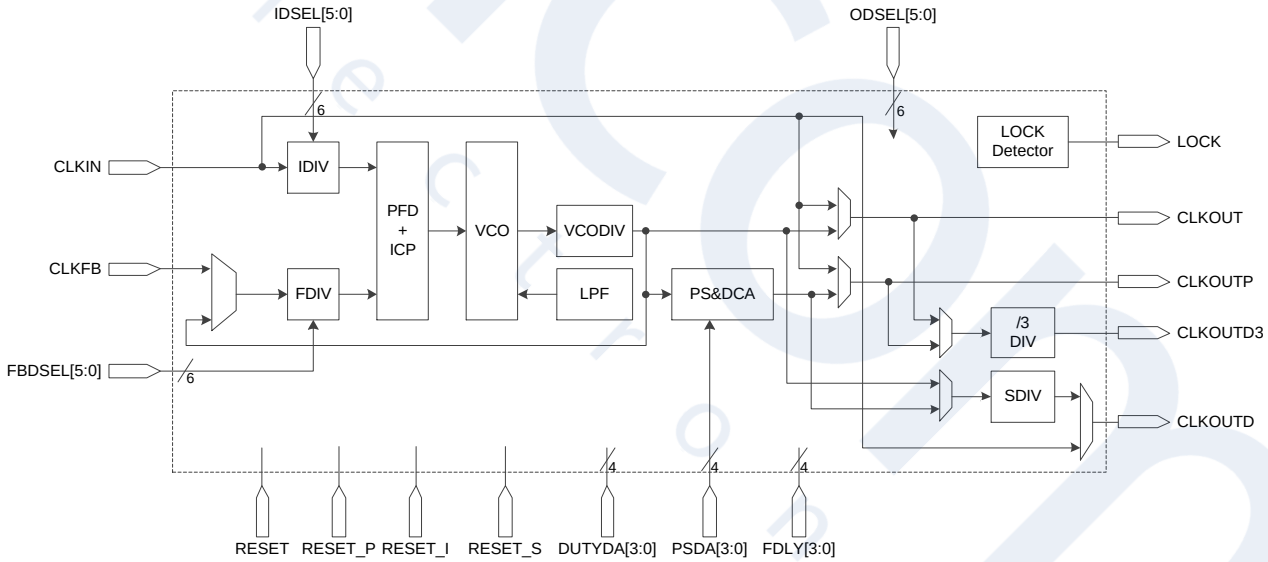
3.8.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-41 for the PLL structure.

Figure 3-41 PLL Structure



The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

PLL features are as follows:

- Input frequency:3 MHz~450 MHz
- VCO vibration frequency: 400 MHz~900 MHz

- CLKOUT output frequency: 3.125 MHz~450 MHz

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. $f_{CLKOUT} = (f_{CLKIN}*FDIV)/IDIV$
2. $f_{VCO} = f_{CLKOUT}*ODIV$
3. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
4. $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FDIV$

Note!

- f_{CLKIN}: The frequency of the input clock CLKIN
- f_{CLKOUT}: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Phase Comparison Frequency

Adjust IDIV, FDIV, ODIV, and SDIV to achieve the required clock frequency.

See Table 3-17 for a definition of the PLL ports.

Table 3-17 PLL Ports Definition

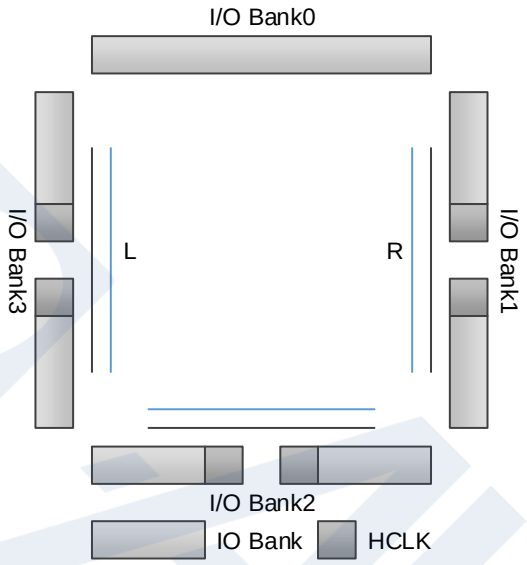
Port Name	Signal	Description
CLKIN [5：0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
RESET_I	I	IDIV reset
RESET_S	I	SDIV and DIV3 reset
INSEL[2：0]	I	Dynamic clock control selector: 0~5
IDSEL [5：0]	I	Dynamic IDIV control: 1~64
FBDSEL [5：0]	I	Dynamic FDIV control:1~64
PSDA [3：0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3：0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	Clock output with no phase and duty cycle adjustment
CLKOUTP	O	Clock output with phase and duty cycle adjustment
CLKOUTD	O	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1: locked, 0: unlocked

3.8.3 HCLK

HCLK is the high-speed clock in the GW1NRF series of Bluetooth FPGA products. It can support high-performance data transfer and is

mainly suitable for source synchronous data transfer protocols. See Figure Figure 3-42.

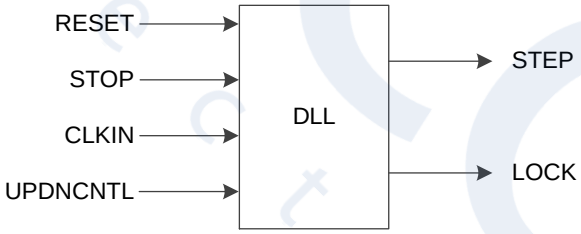
Figure 3-42 GW1NRF HCLK Distribution



3.8.4 DLL

The GW1NRF series of Bluetooth FPGA products support DLL. For DLL function, see Figure 3-43.

Figure 3-43 GW1NRF DLL Function



The source of CLKIN can come from GCLK and the neighboring HCLK.

The calculated STEP will be sent to the neighboring Banks. For example, the signal STEP of DLL can be sent to HCLK in Bank2. At the same time, the signal STEP can also be sent to the user logic through the CRU.

3.9 Long Wire (LW)

As a supplement to the CRU, the GW1NRF series of Bluetooth FPGA products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

3.10 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW1NRF series of Bluetooth FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset, registers in CFU and I/O can be configured independently.

3.11 Programming Configuration

The GW1NRF series of Bluetooth FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash.

Besides JTAG, the GW1NRF series of Bluetooth FPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For the detailed information, please refer to *Gowin series of FPGA products Programming and Configureation User Guide*.

3.11.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the deviece.

3.11.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start/Instant Start”.

GW1NRF devices have the feature of transparent transmission. That is to say, GW1NRF devices can program the on-chip Flash or off-chip Flash via the JTAG interface without affecting the current working state. During programming, the device works according to the previous configuration. After programming, provide one low pulse for RECONFIG_N to complete the online upgrade. This feature applies to the applications with long online time and irregular upgrades.

The GW1NRF series of Bluetooth FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *Gowin FPGA Products Programming and Configuration Guide* for more detailed information.

3.12 On Chip Oscillator

There is an internal oscillator in each of the GW1NRF series of Bluetooth FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-18 for the output frequency.

Table 3-18 GW1NRF-4B Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.1MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] Default Frequency.
- [2] 125MHz is not suitable for MSPI programming mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formual is employed to get the output clock frequency for GW1NRF-4B device:

f_{out}=210MHz/Param

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

4 AC/DC Characteristics

Note!

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

4.1 Operating Conditions

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	-0.5V	1.32V
	UV:Core Power	-0.5V	3.75V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary Power	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃
Junction Temperature	Junction Temperature	-40 ℃	+125 ℃
SoC Operating Temperature Range	SoC Operating Temperature Range	-40℃	+85℃
SoC Operating Temperature for OTP write	SoC Operating Temperature for OTP write	-40℃	+85℃

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
V_{CCOx}	I/O Bank Power	1.14V	3.465V
V_{CCX}	Auxiliary voltage	2.375V	3.465V
T_{JCOM}	Junction temperature Commercial operation	0℃	+85℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃
T_{RAMP}	Power supply ramp rates for all power supplies	0.01mV/μs	10mV/μs

Name	Description	Min.	Max.
VBAT1	SoC Battery voltage 1	2.3V	3.6V
VBAT2	SoC Battery voltage 2, TX Power Level 0~14	1.05V	3.6V
	SoC Battery voltage 2, TX Power Level 15	1.25V	3.6V
	SoC Battery voltage 2, TX Power Level 16	1.45V	3.6V
	SoC Battery voltage 2, TX Power Level 17	1.7V	3.6V
SoC Operating Temperature Range	SoC Operating Temperature Range	-40℃	+85℃
SoC Operating Temperature for OTP write	SoC Operating Temperature for OTP write	-40℃	+85℃

Table 4-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Min.
T_{RAMP}	Power supply ramp rates for all power supplies	0.01mV/μs	-	10mV/μs
T_{RAMP_B}	Battery ramp-up slope	1V/μs	-	3.6V/μs

Table 4-4 Hot Socket Specifications

Name	Description	Condition	Max.
I_{HS}	Input or I/O leakage current	V_{IN}=V_{IL} (MAX)	TBD

4.2 ESD

Table 4-5 GW1NRF ESD – HBM

Device	GW1NRF-4B
QN48	HBM>1,000V

Table 4-6 GW1NRF ESD - CDM

Device	GW1NRF-4B
QN48	CDM>500V

Table 4-7 DC Electrical Characteristics under Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	V_{CCO}<V_{IN}<V_{IH} (MAX)	-	-	210 μA
		0V<V_{IN}<V_{CCO}	-	-	10 μA

Name	Description	Condition	Min.	Typ.	Max.
I_{PU}	I/O Active Pull-up Current (I/O Active Pull-up Current)	$0<V_{IN}<0.7V_{CCO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current (I/O Active Pull-up Current)	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30 μA	-	150 μA
I_{BHLS}	Bus Hold Low Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN}=V_{IL}$ (MAX)	30 μA	-	-
I_{BHHO}	Bus Hold High Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN}=0.7V_{CCO}$	-30 μA	-	-
I_{BHLO}	Bud HoldLow Overdrive Current (Bus Hold Low Sustaining Current)	$0\leq V_{IN}\leq V_{CCO}$	-	-	150 μA
I_{BHHO}	BusHoldHigh Overdrive Current	$0\leq V_{IN}\leq V_{CCO}$	-	-	-150 μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance (I/O Capacitance)			5 pF	8 pF
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-
		V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

4.3 DC Characteristics

4.3.1 Static Current

Table 4-8 Static Supply Current[1]

Name	Description	LV/UV	Device	Typ.
I_{CC}	Core current V_{CCX}=3.3V, V_{CCX}=2.5V	LV/UV	GW1NRF-4B	TBD
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V)	LV/UV	GW1NRF-4B	TBD
	V_{CCX} current（V_{CCX}=2.5V)	LV/UV	GW1NRF-4B	TBD
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	LV/UV	ALL	TBD

Note!

[1] T_J = 25℃

Table 4-9 DC Characteristics, DCDC Step-Down Configuration, VBAT2=3.0V

Parameter	Min	Typ	Max	Unit
RX Mode	-	3.0	-	mA
TX mode, TX Power Level 0	-	2.2	-	mA
TX mode, TX Power Level 1	-	2.4	-	mA
TX mode, TX Power Level 2	-	2.8	-	mA
TX mode, TX Power Level 3	-	2.9	-	mA
TX mode, TX Power Level 4	-	3.0	-	mA
TX mode, TX Power Level 5	-	3.1	-	mA
TX mode, TX Power Level 6	-	3.2	-	mA
TX mode, TX Power Level 7	-	3.3	-	mA
TX mode, TX Power Level 8	-	3.4	-	mA
TX mode, TX Power Level 9	-	3.6	-	mA
TX mode, TX Power Level 10	-	3.8	-	mA
TX mode, TX Power Level 11	-	4.1	-	mA
TX mode, TX Power Level 12	-	4.3	-	mA
TX mode, TX Power Level 13	-	4.6	-	mA
TX mode, TX Power Level 14	-	5.2	-	mA
TX mode, TX Power Level 15	-	5.6	-	mA
TX mode, TX Power Level 16	-	7.5	-	mA
TX mode, TX Power Level 17	-	9.9	-	mA
1 Active RC	-	0.2	-	mA
Active XTAL1	-	0.4	-	mA
ECC ROM execution in a loo p	-	0.7	-	mA
Coremark test from IRAM1	-	1.2	-	mA
Coremark test from OTP	-	1.6	-	mA

Parameter	Min	Typ	Max	Unit
Sleep mode, LF RC	-	1.0	-	uA
Sleep mode, LF XTAL	-	0.95	-	uA
Deep Sleep mode	-	0.65	-	uA
Chip Disable	-	5	-	nA
Battery peak current2	-	10.3	-	mA

Table 4-10 DC Characteristics, DCDC Step-Up Configuration, VBAT2=1.5V

Parameter	Min	Typ	Max	Unit
RX Mode	-	5.8	-	mA
TX mode, TX Power Level 0	-	4.1	-	mA
TX mode, TX Power Level 1	-	4.5	-	mA
TX mode, TX Power Level 2	-	5.3	-	mA
TX mode, TX Power Level 3	-	5.5	-	mA
TX mode, TX Power Level 4	-	5.7	-	mA
TX mode, TX Power Level 5	-	5.8	-	mA
TX mode, TX Power Level 6	-	6.1	-	mA
TX mode, TX Power Level 7	-	6.3	-	mA
TX mode, TX Power Level 8	-	6.6	-	mA
TX mode, TX Power Level 9	-	6.9	-	mA
TX mode, TX Power Level 10	-	7.3	-	mA
TX mode, TX Power Level 11	-	7.8	-	mA
TX mode, TX Power Level 12	-	8.3	-	mA
TX mode, TX Power Level 13	-	8.8	-	mA
TX mode, TX Power Level 14	-	9.9	-	mA
TX mode, TX Power Level 15	-	10.7	-	mA
TX mode, TX Power Level 16	-	12.7	-	mA
TX mode, TX Power Level 17 1	-	14.8	-	mA
Active RC2	-	0.3	-	mA
Active XTAL2	-	0.7	-	mA
ECC ROM execution in a loo p	-	1.3	-	mA
Coremark test from IRAM1	-	2.4	-	mA
Coremark test from OTP	-	3.2	-	mA
Sleep mode, LF RC	-	1.0	-	uA
Sleep mode, LF XTAL	-	0.95	-	uA
Deep Sleep mode	-	0.65	-	uA
Chip Disable	-	5	-	nA
Battery peak current	-	21.2	-	mA

4.3.2 RF Parameters

Table 4-11 Low Frequency Crystal Oscillator Specifications

Parameters	Comments	Symb.	Min	Typ	Max	Units
Crystal frequency	Fundamental	f_{LFXTAL}	32.768			KHz
Crystal deviation	Including frequency tolerance, stability over temperature, aging, and total tolerances of external capacitances	$df0/f0_{LFXTAL}$	-300	-20	-	ppm
Typical supported crystal parameters	Equiv. series Res.	ESR_{LFXTAL}	-	55	100	kΩ
	Differential equivalent load capacitance (13)	CL_{LFXTAL}	-	6	-	pF

Table 4-12 High Frequency Crystal Oscillator Specifications

Parameters	Comments	Symb.	Min	Typ	Max	Units
Crystal frequency	Fundamental	f_{XTAL}	48			MHz
Crystal deviation	Including frequency tolerance, stability over temperature, aging, and total tolerances of external capacitances	df0/f0	-	-	±50	ppm
Typical supported Xta parameters	Equiv. series Res.	ESR_{XTAL}	20	-	80	kΩ
	Differential equivalent load capacitance (13)	CL_{XTAL}	6	8	10	pF

Table 4-13 General RF Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
RF input impedance	Single ended	Z_{IN}	-	50	-	Ω
Input reflection coefficient	All channels	S_{11}	-	-	-8	dB
Data rate	BT LE 1M PHY	R_{BT}	-	1000	-	Kbps

Table 4-14 Transmitter Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
Output power	TX Power Level 0	P_{TX0}	-	-33.5	-	dBm

Parameters	Comments	Symb.	Min	Typ	Max	Units
	TX Power Level 1	P_{TX1}	-	-29.0	-	dBm
	TX Power Level 2	P_{TX2}	-	-17.9	-	dBm
	TX Power Level 3	P_{TX3}	-	-16.4	-	dBm
	TX Power Level 4	P_{TX4}	-	-14.6	-	dBm
	TX Power Level 5	P_{TX5}	-	-13.1	-	dBm
	TX Power Level 6	P_{TX6}	-	-11.4	-	dBm
	TX Power Level 7	P_{TX7}	-	-9.9	-	dBm
	TX Power Level 8	P_{TX8}	-	-8.4	-	dBm
	TX Power Level 9	P_{TX9}	-	-6.9	-	dBm
	TX Power Level 10	P_{TX10}	-	-5.5	-	dBm
	TX Power Level 11	P_{TX11}	-	-4.0	-	dBm
	TX Power Level 12	P_{TX12}	-	-2.6	-	dBm
	TX Power Level 13	P_{TX13}	-	-1.4	-	dBm
	TX Power Level 14	P_{TX14}	-	0.4	-	dBm
	TX Power Level 15	P_{TX15}	-	2.5	-	dBm
	TX Power Level 16	P_{TX16}	-	4.6	-	dBm
	TX Power Level 17	P_{TX17}	-	6.2	-	dBm
Power in 2nd harmonic	Output power step = 17 50 Ω for "Typ" value.	P_{TX2}	-	-50	-	dBm
Power in 3rd harmonic		P_{TX3}	-	-60	-	dBm
Power in 4th harmonic		P_{TX4}	-	-50	-	dBm
Deviation from the channel center frequency		Δf_c	-150	-	150	KHz
Frequency drift for any packet length		Δfc_pkt	-	-	50	KHz
Drift rate		$\Delta f_c/\Delta T$	-	-	400	Hz/μs
Modulated frequency deviation		Δf_{mod}	-	±250	-	KHz
In-band spurious emission, power transmitted outside the selected channel, at a frequency offset foffs	$\lvert f_{offs} \rvert$ = 2MHz	P_{out} (f_c+f_{offs})	-	-	-20	dBm
	$\lvert f_{offs} \rvert \geq$ 3MHz		-	-	-30	dBm

Table 4-15 Receiver Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
Sensitivity	1Mbps, 37 byte payload	-	-	-94	-	dBm
	1Mbps, 255 byte payload	-	-	-93	-	dBm
Maximum input power	1Mbps, 255 byte payload	R_{BT}	-	0	-	dBm
In-band blocking (-67dBm desired signal)	Co-channel interference (i.e.0MHz)	C/I0_MHz	-	6	-	dB
	Adjacent ±1MHz interference	C/I±1_MHz	-	-4	-	dB
	Adjacent +2MHz interference	C/I+2_MHz	-	-25	-	dB
	Adjacent -2MHz interference	C/I-2_MHz	-	-18	-	dB
	Adjacent +3MHz interference	C/I+3_MHz	-	-33	-	dB
	Adjacent -3MHz interference	C/I-3_MHz	-	-32	-	dB
	Adjacent ≥±4MHz and ≤±10MHz interference	C/I4-10_MHz	-	-35	-	dB
	Adjacent ≥±10MHz interference	$C/I_{\geq 10\_MHz}$	-	-43	-	dB
Out-of-band blocking (-67dBm desired signal)	30MHz – 2000MHz		-30	-	-	dBm
	2003MHz – 2399MHz		-35	-	-	dBm
	2484MHz – 2997MHz		-35	-	-	dBm
	3000MHz – 12.75GHz		-30	-	-	dBm
Intermodulation	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm3$MHz	-	-	-45	-	dBm
	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm4$MHz	-	-	-45	-	dBm
	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm5$MHz	-	-	-45	-	dBm
Spurious emissions	F=30MHz – 88MHz	-	-	-	-57.4	dBm
	F=88MHz-1GHz	-	-	-	-57	dBm
	F=1GHz-12.75GHZ	-	-	-	-47	dBm

4.3.3 I/O Characteristics

Table 4-16 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Table 4-17 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Table 4-18 IOB Differential Electrical Characteristics

LVDS25 (GW1NRF-1does not support.)

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	-	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T =	250	350	450	mV

		100Ω				
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristics

4.4.1 Internal Switching Characteristics

Table 4-19 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

Table 4-20 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

Table 4-21 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from input register	-	4.80	ns
t_{COPR_DSP}	Clock to output from pipeline register	-	2.40	ns
t_{COOR_DSP}	Clock to output from output register	-	0.84	ns

4.4.2 External Switching Characteristics

Table 4-22 External Switching Characteristics

Name	Description	Device	-4		-5		-6		Unit
			Min	Max	Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

Table 4-23 On chip Oscillator Output Frequency

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to +85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

4.5 User Flash Characteristics

4.5.1 DC Characteristics[1]

(T_J = -40~+100℃, V_{CC} = 1.08~1.32V, V_{CCX} = 1.62~3.63V, V_{SS} = 0V)

Table 4-24 User Flash DC Characteristics

Name	Parameter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode (w/I 25ns)[1]	I_{CC1}[2]	2.19	0.5	mA	NA	Min. Clcok period, duty cycle 100%, VIN = "1/0"
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page Erasure Mode		0.1	12	mA	NA	
Read mode static current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE="1", between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Caculated in different T_{new} clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns x I_{CC2}/T_{new} + I_{SB}
  - t > 50ns, I_{CC2} = I_{SB}
- [3] V_{CC} must be greater than 1.08V from the zero wake-up time.

4.5.2 Timing Parameters[1,5,6]

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-25 User Flash Timing Parameters

User Modes	Parameter	Name	Min.	Max.	Unit
Access time[2]	WC1	T_{acc}[3]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time (Overall erase)		T_{nvh1}	100	-	μs

User Modes	Parameter	Name	Min.	Max.	Unit
Time from data storage to program setup		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Write time		T_{prog}	8	16	μs
Write ready time		T_{wpr}	>0	-	ns
Erase hold time		T_{whd}	>0	-	ns
Time from control signal to write/Erase setup		T_{cps}	-10	-	ns
Time from SE to read setup		T_{as}	0.1	-	ns
E pulse high level time		T_{pws}	5	-	ns
Adress/data setup time		T_{ads}	20	-	ns
Adress/data hold time		T_{adh}	20	-	ns
Data hold-up time		T_{dh}	0.5	-	ns
Read mode address hold time[3]	WC1	T_{ah}	25	-	ns
	TC		22	-	ns
	BC		21	-	ns
	LT		21	-	ns
	WC		25	-	ns
SE pulse low level time		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[4]	-	6	ms
Erasure time		T_{erase}	100	120	ms
Overall erase time		T_{me}	100	120	ms
Wake-up time from power down to standby mode		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note!

- [1] The parameter values may change;
- [2] The values are simulation data only.
- [3]After XADR, YADR, XE, and YE are valid, T_{acc} start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]T_{hv} is the time between write and the next erasure.The same address can not be written twice before erasure, so does the same register. This limitation is for safety;
- [5]Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be T_{acc} at leaset, and T_{acc} start from SE rising edge.

4.5.3 Operation Timing Diagrams

Figure 4-1 GW1NRF User Flash Read Operation

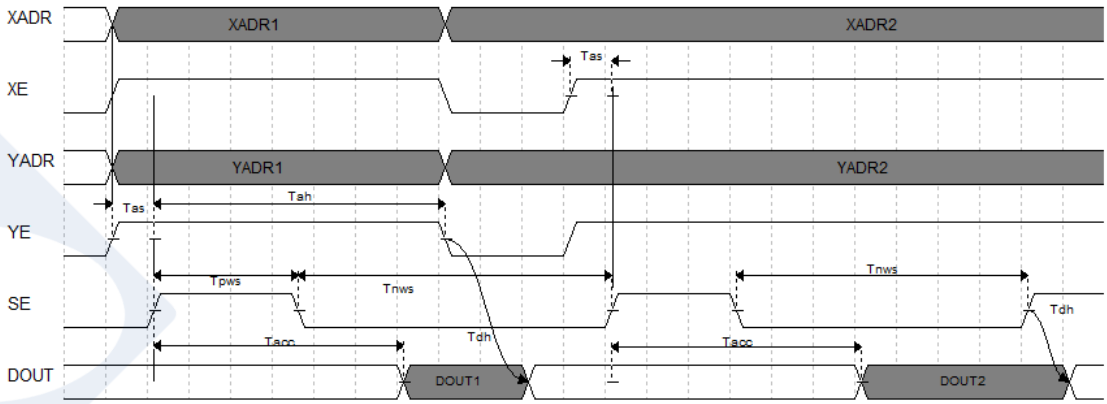


Figure 4-2 GW1NRF User Flash Program Operation

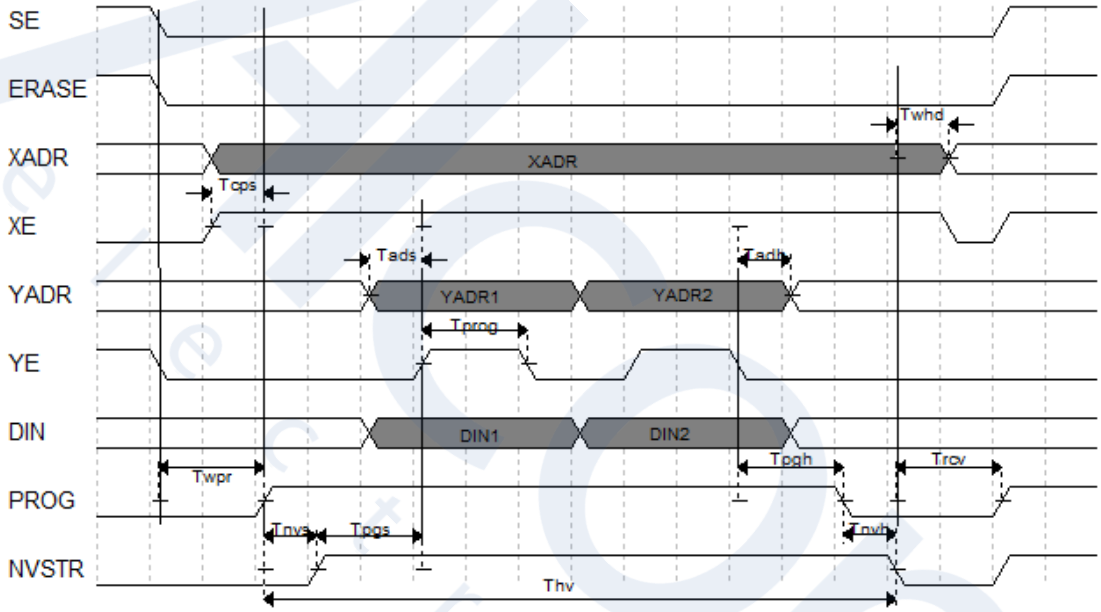
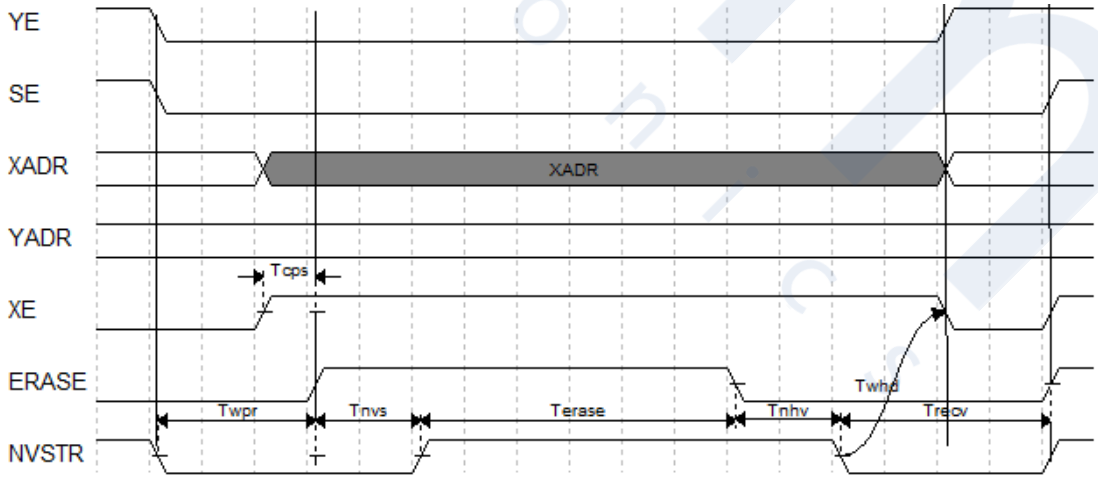


Figure 4-3 GW1NRF User Flash Erase Operation



4.6 Configuration Interface Timing Specification

The GW1NRF series of Bluetooth FPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more detailed information, please refer to *Gowin FPGA products Programming and Configureation User Guide*.

4.6.1 JTAG Port Timing Specifications

The JTAG mode of the GW1NRF series of Bluetooth FPGA products complies with IEEE1532 and IEEE1149.1 boundary scan standards.

JTAG mode downloads the bitstream to SRAM, and the data is lost after power off.

See Figure 4-4 for JTAG timing.

Figure 4-4 JTAG Timing

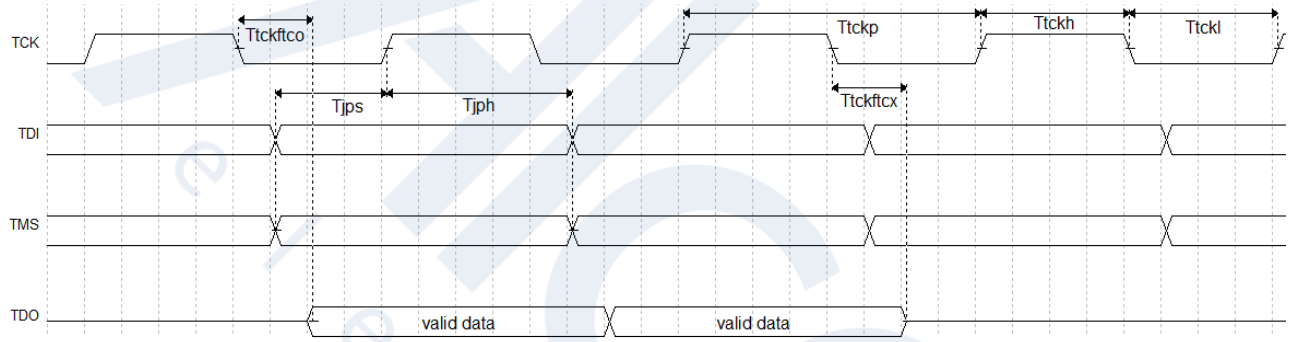


Table 4-26 JTAG Timing Parameters

Name	Description	Min.	Max.
$T_{tckftco}$	Time from TCK falling edge to output		10ns
$T_{tckftcx}$	Time from TCK falling edge to high impedance		10ns
T_{tckp}	TCK clock period	40ns	-
T_{tckh}	TCK clock high time	20ns	-
T_{tckl}	TCK clock low time	20ns	-
T_{jps}	JTAG PORT setup time	10ns	
T_{jph}	JTAG PORT hold time	8ns	

Other than the power requirements, the following conditions need to be met to use the MSPI configuration mode:

- MSPI port enable

Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin

RECONFIG_N.

4.6.2 AUTO BOOT Port Timing Specifications

The AUTOBOOT mode offers instant-on feature for the GW1NRF series of Bluetooth FPGA products. In this mode, FPGA reads data from the on-chip Flash directly for the program to load after the chip is powered on.

On-chip Flash is configured via the JTAG interface. After the configuration, RECONFIG_N is triggered by a low level pulse, or auto boot configuration starts after power recycle. Figure 4-5 shows the timing.

Figure 4-5 Power Recycle Timing

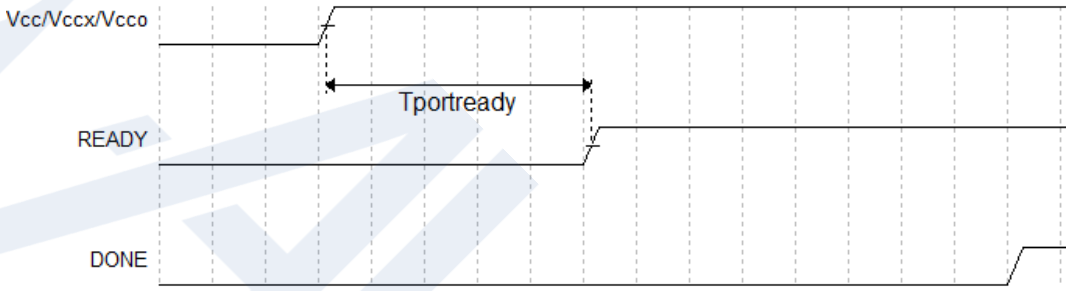


Figure 4-6 RECONFIG_N Trigger Timing

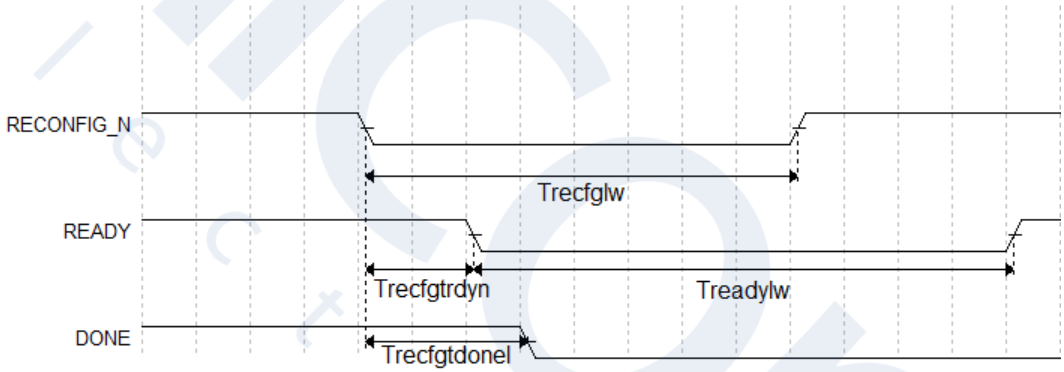


Table 4-27 shows the timing parameters.

Table 4-27 Parameters for Power Recycle and RECONFIG_N Trigger Timing

Name	Description	Min.	Max.
$T_{portready}$ [1]	Time from application of V_{CC}, V_{CCX} and V_{CCO} to the rising edge of READY	50μs	200μs
$T_{recfglw}$	RECONFIG_N low pulse width	25ns	
$T_{recfgtrdyn}$	Time from RECONFIG_N falling edge to READY low	-	70ns
$T_{readylw}$	READY low pulse width	TBD	
$T_{recfgtdonel}$	Time from RECONFIG_N falling edge to DONE low	-	80ns

Note!

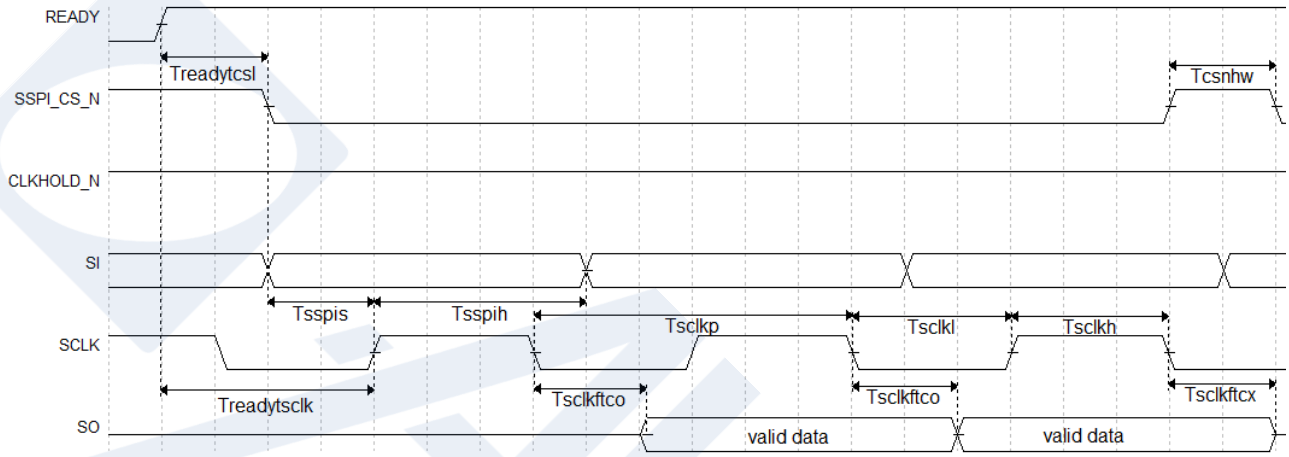
MODE0=0, the device power-up waiting time is 200 μs; MODE0=1, the device power- up waiting time is 50 μs.

4.6.3 SSPI Port Timing Specifications

In the slave SSPI mode, the GW1NRF series of Bluetooth FPGA products are configured by the hardware processer via SPI.

See Figure 4-7 for the SSPI timing diagram.

Figure 4-7 SSPI Timing Diagram



See Table 4-28 for the timing parameters.

Table 4-28 SSPI Timing parameters

Name	Description	Min.	Max.
T_{sclkp}	SCLK clock period	15 ns	-
T_{sclkh}	SCLK clock high time	7.5 ns	-
T_{sclkl}	SCLK clock low time	7.5 ns	-
T_{sspis}	SSPI PORT setup time	2 ns	-
T_{sspih}	SSPI PORT hold time	0 ns	-
$T_{sclkftco}$	Time from SCLK falling edge to output	-	10 ns
$T_{sclkftcx}$	Time from SCLK falling edge to high impedance	-	10 ns
T_{csnhw}	CSN high time	25 ns	-
$T_{readytcsl}$	Time from READY rising edge to CSN low		
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Other than the power requirements, the following conditions need to be met to use the SSPI configuration mode:

- SSPI port enabled
  Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power up or the previous programming activity.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.4 MSPI Port Timing Specifications

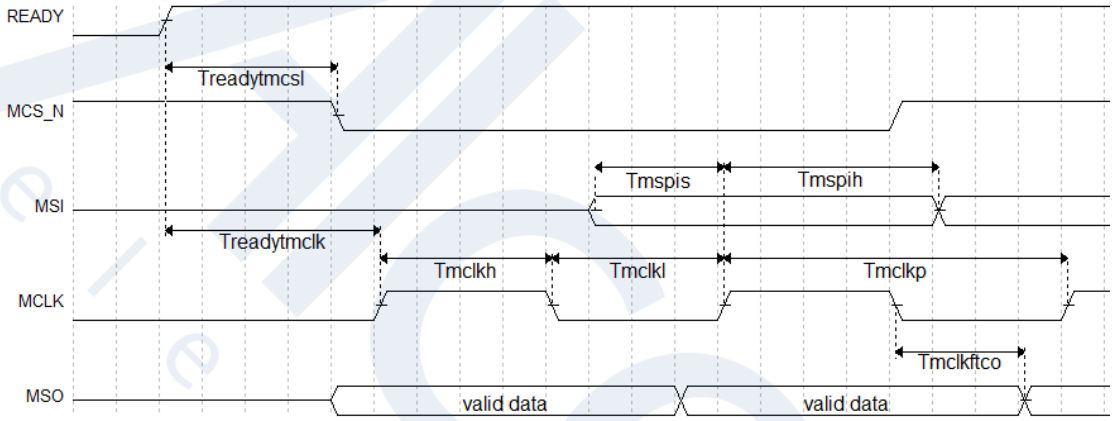
In master MSPI mode, the configuration data is retrieved automatically from the off-chip SPI Flash. The default MCLK frequency of the GW1NRF-1 and GW1NRF-9 is 2.5 MHz; the default MCLK frequency of GW1NRF-4 is 2.1MHz. The MCLK accuracy is +/- 5%.

After MSPI writes the configuration data to the off-chip Flash, power recycle or RECONFIG_N will trigger device configuration. GW1NRF-1 and GW1NRF-4 only support one auto MSPI configuration; if this fails, power recycle or RECONFIG_N will trigger device configuration.

GW1NRF-9 supports multiple auto MSPI configurations; if this fails for the first time, FPGA automatically reads external Flash twice. Users can set the address, and the default address is 0.

See Figure 4-8 for the MSPI Timing Diagram.

Figure 4-8 MSPI Timing Diagram



See Table 4-29 for the MSPI timing diagram.

Table 4-29 MSPI Timing Parameters

Name	Description	Min.	Max.
T_{mclkp}	MCLK clock period	15 ns	-
T_{mclkh}	MCLK clock high time	7.5 ns	-
T_{mclkl}	MCLK clock low time	7.5 ns	-
T_{mspis}	MSPI PORT setup time	5 ns	-
T_{mspih}	MSPI PORT hold time	1 ns	-
$T_{mclkftco}$	Time from MCLK falling edge to output	-	10 ns
$T_{readytmcsl}$	Time from READY rising edge to MCS_N low	100 ns	200 ns
$T_{readytmclk}$	Time from READY rising edge to first MCLK edge	2.8 µs	4.4 µs

4.6.5 DUAL BOOT

In DUAL BOOTmode, the configuration data is retrieved automatically from the off chip Flash or from on chip Flash.

See *DUAL BOOT Download Solution based on GW1N-4 Device* for the DUAL BOOT Config Mode implementation of GW1NRF-4B.

4.6.6 CPU

In CPU mode, the GW1NRF series of Bluetooth FPGA products are configured by hardware processor via DBUS interface. Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power up or the previous programming activity.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.7 SERIAL

In SERIAL mode, the GW1NRF series of Bluetooth FPGA products are configured by the hardware processor via serial interface. Other than the power requirements, the following conditions need to be met to use the SERIAL configuration mode:

- SERIAL port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Naming–ES

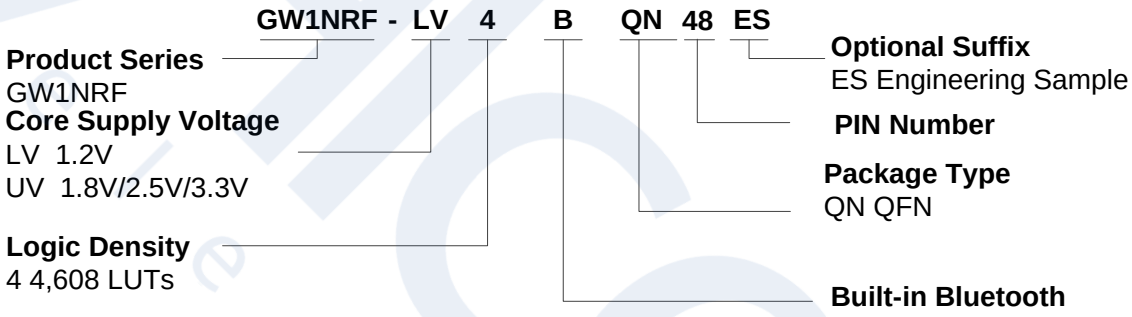
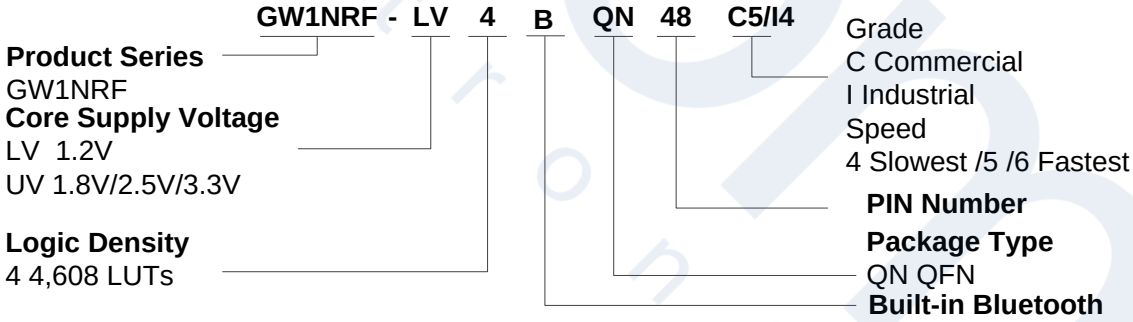


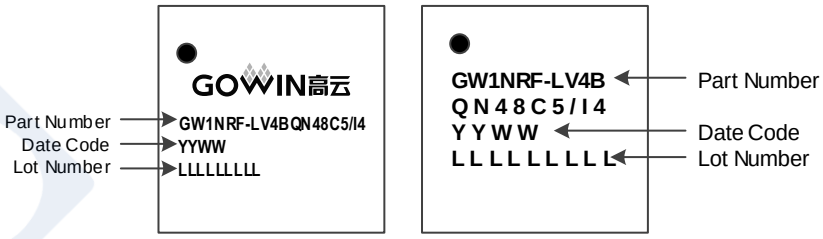
Figure 5-2 Part Naming–Production



5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure Figure 5-3.

Figure 5-3 Package Mark



Note!

The first two lines in the right figure above are the "Part Number".

Singel 3 | B-2550 Kontich | Belgium | Tel. +32 (0)3 458 30 33 | info@alcom.be | www.alcom.be
Rivium 1e straat 52 | 2909 LE Capelle aan den Ijssel | The Netherlands | Tel. +31 (0)10 288 25 00 | info@alcom.nl | www.alcom.nl