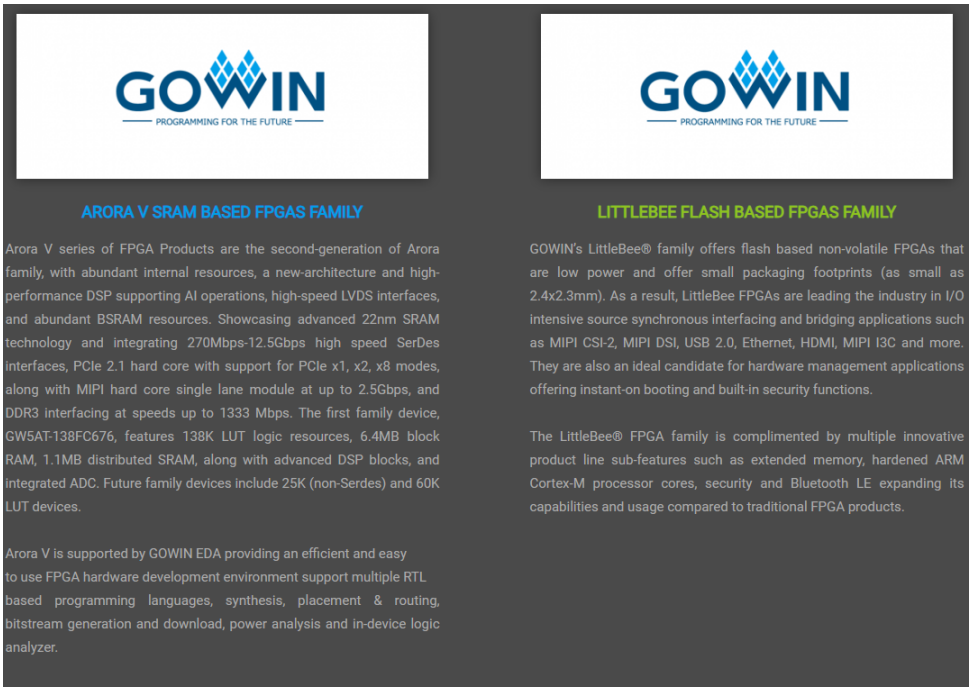


Arora V SRAM Based FPGAs

GOWINSEMI's Arora V FPGA series provides SRAM-based FPGA devices with increased logic resources, interfaces and performance. Arora V FPGAs include DDR3 memory interfacing, 12.5Gbps CDR-based SERDES supporting multiple protocols and flexible packaging options making it the ideal choice for communications, server, imaging, and automotive applications requiring high interface and computing throughput by providing best performance/watt.

Arora V is supported by GOWIN EDA providing an efficient and easy-to-use FPGA hardware development environment support multiple RTL-based programming languages, synthesis, placement & routing, bitstream generation and download, power analysis and in-device logic analyzer.

Arora V FPGA Product Features:

FPGA Fabric Architecture

- Up to 138K LUTs(GW5A(S)(T)-138)
- Up to 23K LUTs(GW5A-25)
- Block SRAM with multiple modes
    - Single Port, Semi-Dual Port, True Dual Port, and Semi Dual Port with ECC function
    - Byte write enable

    - ECC error detection and correction
- High performance DSP
    - Multipliers support 12x12, 27x36, 27x18-bit modes
    - Includes 48-bit accumulator
    - Supports DSP cascading
    - Embedded pipeline and bypass registers
    - Pre-addition operation for filter function
    - Internal feedback loop and barrel shifter
- Advanced Clocking
    - Up to 16 global clocks
    - Up to 6/12 high-performance PLLs
    - Up to 16/24 high speed edge clocks

Flexible GPIO

- Adjustable drive strength
    - 4mA, 8mA, 12mA, 16mA, 24mA drive
- Bus keeper, pull up/down, and open drain
- Hot Socket and input hysteresis
- Slew Rate option for output signal

ADC

- 60dB SNR and 1kHz Signal Bandwidth
- Flexible X-channel oversampling ADC
- No external voltage source required

Configuration & Programming

- JTAG, SSPI, MSPI, CPU, and SERIAL
    - Background programming
    - SPI Flash Programming and Boot
    - Multi-boot
- Bitstream encryption and Security
- Configuration Memory Soft Error Recovery(CMSER)

- mDRP(GW5A)
- Supports OTP, each device has a unique 64-bit DNA identifier

High Speed Interfaces

- SERDES(GW5AT, GW5AST)
    - 270Mbps-12.5Gbps operation
    - CDR (Clock Data Recovery)
    - Dedicated RX and TX Channels
    - Integrated 8b/10b encoder/decoder
    - PCI 2.0 hardcore
        - x1, x2, x4, x8 lanes
        - Supports root complex and end point
- GW5AST series of FPGA products provide a hardcore processor RiscV AE350_SOC
- MIPI D-PHY RX hardcore(GW5A(S)(T)-138)
    - 20Gbps D-PHY RX Hard PHY
    - 8 data lanes + 2 clock lanes
    - 2.5Gbps/lane
    - Built-in SoT HS-Sync, word and lane alignment
    - MIPI DSI and MIPI CSI-2 RX link layer IPs
- MIPI D-PHY RX/TX hardcore(GW5A-25)
    - 4 data lanes + 1 clock lane
    - 2.5Gbps/lane(RX/TX)
    - Built-in SoT HS-Sync, word and lane alignment
    - MIPI DSI and MIPI CSI-2 RX link layer IPs
- GPIOs supports D-PHY RX/TX(GW5A-25)
    - 1.2Gbps/lane
    - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX/TX device interface
- GPIOs support MIPI D-PHY RX(GW5A(S)(T)-138)
    - 1.5Gbps/lane
    - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX device interface
- External DRAM Interfaces
    - Supports various memory types
        - DDR2, DDR3, PSRAM, HyperRAM, RPC
    - Up to 1333 Mbps (GW5A(S)(T)-138) or 1066 Mbps (GW5A-25

LittleBee Flash Based FPGAs

GOWIN's LittleBee® product family offers flash based, non-volatile FPGAs with an abundance of logic resources, multiple IO standards, embedded RAM, DSPs, PLLs, embedded security and additional user flash while being optimized for low power, low cost and small footprint applications requiring instant-on, high IO count, high throughput and low latency programmable computing.

As a result, LittleBee® FPGAs are leading the industry in I/O intensive source synchronous interfacing and bridging applications such as MIPI CSI-2, MIPI DSI, USB 2.0, Ethernet, HDMI, MIPI I3C and more. They are also an ideal candidate for hardware management applications offering instant-on booting and built-in security functions.

The LittleBee® FPGA family is complimented by multiple innovative product line sub-features such as extended memory, hardened ARM Cortex-M processor cores, security and Bluetooth LE expanding its capabilities and usage compared to traditional FPGA products.

GOWIN Semiconductor also provides highly optimized and easy to use FPGA development software supporting the LittleBee® product family including synthesis, mapping, placement, routing and bitstream generation along with programming tools, embedded logic analyzer, and power calculator.

LittleBee FPGA Product Features:

-
  - Small Form Factor

-As small as 2.3x2.4mm2

-
  - Embedded Flash

-Bitstream

-User

-
  - Extensive Pipeline Computing Resources

-Higher DSP Ratio

-Higher RAM Ratio

-

- Flexible Programming Interface

-JTAG, MSPI, SSPI, I2C, CPU

-Multi-Boot

-

- Serialized Interface Support

-MIPI CSI-2, MIPI DSI, LVDS, HDMI

-USB 2.0, PCI, Ethernet

-DDR3, HyperRAM, PSRAM

-

- Embedded Security

- Bitstream Encryption

- Device Locking

-

- Extension Features

- Integrated PSRAM

-Hardened ARM Cortex-M3 and Synopsys ARC MCU Cores

-Bluetooth Low Energy Transceiver

-PUF Based Asynchronous Application Security

-AEC-100Q Automotive Qualified

Arora SRAM Based FPGAs

GOWIN's Arora family of FPGA ICs offer a 'best-in-class' performance/cost ratio making it the ideal choice for compute intensive consumer, industrial, automotive and test equipment applications.

These mid-density SRAM based FPGAs offer optimized LUTs, DSPs, BSRAM, serialized I/O for real-time SoC, co-processing and signal processing development.

The Arora family is complemented by multiple innovative product line sub-features such as embedded PSRAM, DDR and Flash expanding its capabilities and usage compared to traditional FPGA products.

Arora FPGA Product Features:

- Small Form Factor

-As small as 8x8mm2

- High IO Count

-Up to 607 User IO

- Serialized Interface Support

-MIPI CSI-2, MIPI DSI, LVDS, HDMI

-USB 2.0, PCI, Ethernet

-DDR3, HyperRAM, PSRAM

- Extensive Pipeline Computing Resources

-Higher DSP Ratio

-Higher RAM Ratio

- Flexible Programming Interface

-JTAG, MSPI, SSPI, I2C, CPU

-Multi-Boot

- Embedded Security

-Bitstream Encryption

-Device Locking

- Extension Features

-Integrated PSRAM and DDR3

-Integrated FLASH

-AEC-100Q Automotive Qualified

GoBridge ASSP

GoBridge ASSPs are highly integrated, low-power, single-chip devices for interfacing and communicating between various types of peripheal interfaces. The GoBridge ASSPs are ideal for converting from one type of peripheal interface to another, multiplexing between multiple interfaces or demultiplexing to multiple interfaces.

The first two devices in the GoBridge ASSP product line are the GWU2X and GWU2U ASSPs, which provide interface conversion between USB and SPI, JTAG, I2C, GPIO and UART. Future ASSP's will be added to the Gowin GoBridge product line soon.

Bult-in Interface conversion processing and data buffering
I/O independent power supply, supports 3.3V, 2.5V, 1.8V level standards
Configurable register map
Independent clock adjustment
API provided in C/C++ for host device usage

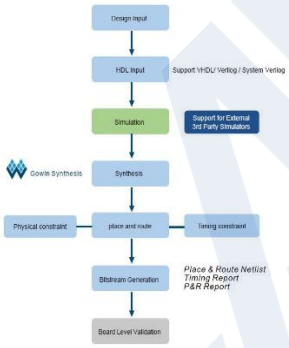
- Supports full-speed USB device interface, compatible with the Universal Serial Bus v1.1 specification
- Built-in USB protocol processing, without device firmware programming
- I/O independent power supply, supports 3.3V, 2.5V, 1.8V level standards
- 16 general-purpose input and output pins
- Supports I2C, SPI and JTAG host interfaces with independent clock adjustment and receive buffer
- API provided in C/C++ for host device usage
- Can be used to program Gowin FPGA products using Gowin Programmer

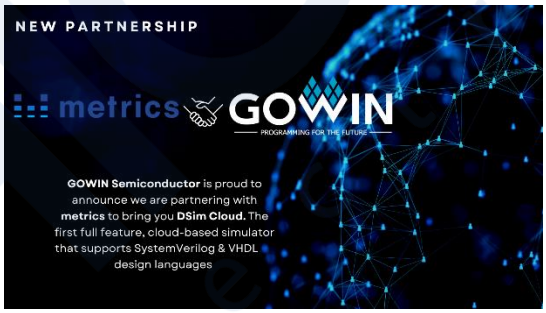
GOWIN EDA Home

GOWIN EDA (Gowin® EDA) – our easy to use integrated design environment provides design engineers one-stop solution from design entry to verification.

Features:

- Complete GUI based environment from FPGA design entry, code synthesis, place & route, bitsteam generation to download on the GOWIN FPGA on your boards.
- Integrates in-house GowinSynthesis for front end design synthesis
- Supports creating RTL and Post-Synthesis.
    - RTL input files are RTL file complied with Hardware Description
- Language and constraints file that users require;
    - Post-synthesis input files are netlist file generated by user RTL
- Synthesis and constraints files that users require.
- Integrates IP Core Generator
- Online debug tool Gowin Analysis Oscilloscope (GAO) for instant analyze of signal design





GOWIN's official choice in simulation solutions is Metrics Design Automation's DSim. Designers never have to think again about whether they can afford to simulate or whether their simulator is up to the job. Now all GOWIN FPGA designers have a world-class simulator with unlimited resources at their fingertips from a single server to thousands of nodes if they need to finish a large test very quickly. True freedom to design and deliver.