Arora V series of FPGA Products

Data Sheet

DS981-1.0E, 09/26/2022

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
09/26/2022	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the Arora V series of FPGA Products, which helps you to understand the Arora V series of FPGA Products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG983, Arora V series of FPGA Products Package and Pinout Manual
- UG982, GW5AT-138 Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ADC	Analog to Digital Converter
AER	Advanced Error Reporting
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
CSI	Camera Serial Interface
CTC	Clock Tolerance Compensation

Terminology and Abbreviations	Full Name
DCS	Dynamic Clock Selector
DFF	D Flip-flop
DNA	Device Identifier
DP	True Dual Port 16K BSRAM
DSI	Display Serial Interface
DSP	Digital Signal Processing
ECC	Error Correcting Code
ECRC	End-to-End Cyclic Redundancy Check
ESD	Electro-Static Discharge
FIFO	First In First Out
FPG	FCPBGA
FPGA	Field Programmable Gate Array
GCLK	Global Clock
GPIO	Gowin Programmable IO
GSR	Global Set/Reset
HCLK	High Speed Clock
IOB	Input/Output Block
LUT	Look-up Table
LW	Long Wire
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable
PCIe	Peripheral Component Interface Express
PCS	Physical Coding Sublayer
PLL	Phase-locked Loop
PMA	Physical Medium Attachment
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 General Description

2.1 Features

FPGA Fabric Architecture

- Up to 138K LUTs(GW5A(T)-138)
- Up to 23K LUTs(GW5A-25)
- Block SRAM with multiple modes
  - Single Port, Semi-Dual Port, True Dual Port, and Semi Dual Port with ECC function
  - Byte write enable
  - ECC error detection and correction
- High performance DSP
  - Multipliers support 12x12, 27x36, 27x18-bit modes
  - Includes 48-bit accumulator
  - Supports DSP cascading
  - Embedded pipeline and bypass registers
  - Pre-addtion operation for filter function
  - Internal feedback loop and barrel shifter
- Advanced Clocking
  - Up to 32 global clocks
  - Up to 6/12 high-performance PLLs
  - Up to 16/24 high speed edge clocks

Flexible GPIO

- Adjustable drive strength
  - 4mA, 8mA, 12mA, 16mA, 24mA drive
- Bus keeper, pull up/down and open drain
- Hot Socket and input hysteresis
- Slew Rate option for output signal

ADC

- 60dB SNR and 1kHz Signal Bandwidth
- Flexible X-channel oversampling ADC
- No external voltage source required

Configuration & Programming

- JTAG, SSPI, MSPI, CPU, and SERIAL
  - Background programming
  - SPI Flash Programming and Boot
  - Multi-boot
- Bitstream encryption and Security
- SEU error detection and correction

High Speed Interfaces

- SERDES(GW5AT-138)
  - 270Mbps-12.5Gbps operation
  - CDR (Clock Data Recovery)
  - Dedicated RX and TX Channels
  - Integrated 8b/10b encoder/decoder
  - PCIe2.0 hardcore
    - x1, x2, x4, x8 lanes
    - Supports root complex and end point
- MIPI D-PHY RX hardcore(GW5A(T)-138)
  - 20Gbps D-PHY RX Hard PHY
  - 8 data lanes + 2 clock lanes
  - 2.5Gbps/lane
  - Built-in SoT HS-Sync, word and lane alignment
  - MIPI DSI and MIPI CSI-2 RX link layer IPs
- MIPI D-PHY RX/TX hardcore(GW5A-25)
  - 4 data lanes + 1 clock lane
  - 2.5Gbps/lane(RX/TX)
  - Built-in SoT HS-Sync, word and lane alignment
  - MIPI DSI and MIPI CSI-2 RX link layer IPs
- GPIOs support MIPI C-PHY RX/TX and D-PHY RX/TX(GW5A-25)
  - 1.2Gbps/lane
  - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX/TX device interface
- GPIOs support MIPI D-PHY RX(GW5AT-138)
  - 1.5Gbps/lane
  - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX device interface
- External DRAM Interfaces
  - Supports various memory types
    - DDR2, DDR3, PSRAM, HyperRAM, RPC
  - Up to 1333 Mbps (GW5A(T)-138) or 1066 Mbps (GW5A-25)

- Supports OTP, each device has a unique 64-bit DNA identifer

GOWINSEMI's Arora V FPGA series provides SRAM based FPGA devices with increased logic resources, interfaces and performance. Arora V FPGAs include DDR3 memory interfacing, 12.5Gbps CDR based SERDES supporting multiple protocols and flexible packaging options making it the ideal choice for communications, server, imaging and automotive applications requiring high interface and computing throughput by providing best performance/watt.

Arora V is supported by GOWIN EDA providing an efficient and easy to use FPGA hardware development environment support multiple RTL based programming languages, synthesis, placement & routing, bitstream generation and download, power analysis and in-device logic analyzer.

2.2 Product Resources

Table 2-1 Product Resources

Device	GW5A-25	GW5AT-60	GW5A-138	GW5AT-138
LUT4	23040	57600	138240	138240
REG	23040	57600	138240	138240
Distributed Static Random Access Memory SSRAM(Kb)	180	450	1080	1080
Block Static Random Access Memory BSRAM(Kb)	1008	2322	6120	6120
Number of BSRAM	56	129	340	340
DSP	28	120	298	298
Phase Locked Loop (PLLs)[1]	6	10	12	12
Global Clock	32	32	32	32
HCLK	16	20	24	24
Transceivers	0	4	0	8
Transceivers Rate	N/A	270Mbps-12.5Gbps	N/A	270Mbps-12.5Gbps
PCIe 2.0 Hardcore	0	1, x1, x2, x4 PCIe 2.0	0	1, x1, x2, x4, x8 PCIe2.0
LVDS Gbps	1.25	1.25	1.25	1.25
DDR3 Mbps	1066	1333	1333	1333
MIPI DPHY Hardcore	2.5G(RX/TX), 4 data lanes, 1 clock lane	2.5G(Rx/Tx), 8 data lanes, 2 clock lane	2.5G(RX) 8 data lanes, 2 clock lanes	2.5G(RX) 8 data lanes, 2 clock lanes
ADC	1	1	2	2
Number of GPIO Banks	9[2]	5	6	6
Max. I/O	236	250	376	376
Core Voltage	0.9V/1.0V	0.9V/1.0V	0.9V/1.0V	0.9V/1.0V

Note!

- [1] Different packages support different numbers of PLLs; up to 12 PLLs can be supported.
- [2] One of the Banks is a JTAG Bank with 4 IOs.

Table 2-2 Package Information and Max. User I/O

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5AT-138	GW5A-138	GW5AT-60	GW5A-25
FPG676A	1.0	27 x 27	-	312(150)	-	-	-

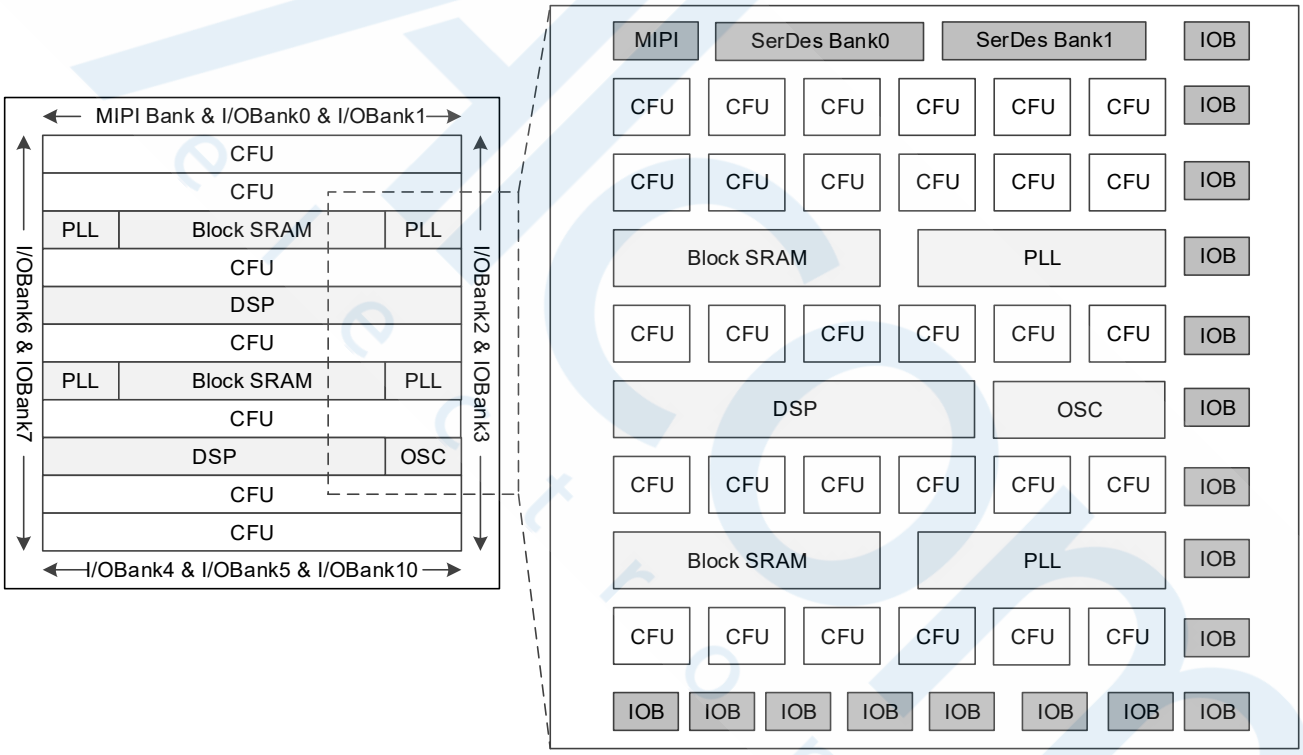
Note!

The package types in this Arora V sheet are written with abbreviations. See 5.1 Part Name for further information.

3 Architecture

3.1 Architecture

Figure 3-1 Architecture Diagram(GW5AT-138)



See Figure 3-1 for an overview of the architecture of the Arora V series of FPGA Products (GW5AT-138). Please refer to Table 2-1 for GW5AT-138 devices internal resources. The core of device is an array of Configurable Function Unit (CFU) surrounded by IO blocks. Besides, Arora V provides BSRAM, DSP Gigabit Transceiver, MIPI D-PHY, ADC, PLL, and on chip oscillator.

Configurable Function Unit (CFU) is the base cell for the array of the Arora V series of FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see

3.2 Configurable Function Unit.

The I/O resources in the Arora V series of FPGA Products are arranged around the periphery of the devices in groups referred to as banks. I/O resources support multiple I/O standards, and support regular mode, SDR mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see 3.3 Input/Output Block.

The BSRAM is embedded as a row in Arora V series of FPGA Products. Each BSRAM has 18,432 Kbits and supports multiple configuration modes and operation modes. For more detailed information, see 3.4 Block SRAM (BSRAM).

Arora V series of FPGA Products are embedded with a brand-new DSP, which can meet your high-performance digital signal processing requirements. For details, refer to 3.5 DSP.

Arora V series of FPGA Products(GW5AT-138) include two Gigabit Transceiver Quads, each of which supports up to 4 transceivers. For details, refer to 3.6 Gigabit Transceiver.

Arora V series of FPGA Products provide a MIPI D-PHY hardcore supporting MIPI Alliance Standard for D-PHY Specification V1.2. For details, refer to 3.8 MIPI D-PHY.

Arora V series of FPGA Products integrate a new and flexible oversampling ADC. For details, refer to 3.9 Analog to Digital Converter

Arora V series of FPGA Products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the Arora V series of the FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 105MHz, providing the clock resource for the MSPI mode. It also provides programmable user clocks. For more detailed information, please refer to 3.14 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the Arora V series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more details, see 3.11 Long Wire (LW), 3.12 Global Set/Reset (GSR), 3.13 Programming Configuration.

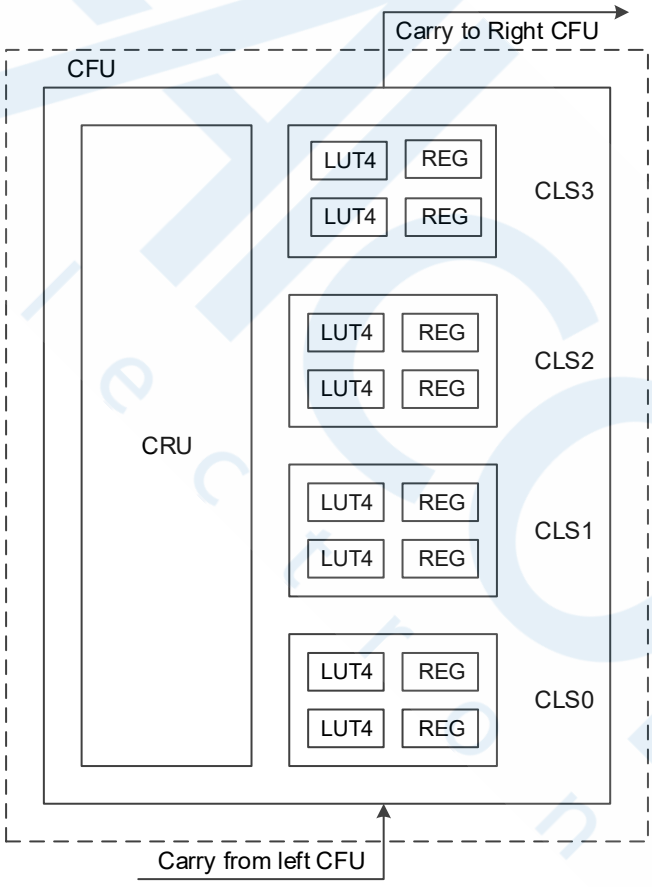
3.2 Configurable Function Unit

Configurable Function Units (CFUs) are the basic cells for the array of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLS) and their routing resource Configurable Routing Unit (CRU). Each CLS includes two 4 input look-up-tables (LUT) and two registers (REG), as shown in Figure 3-2.

CLS in the CFU can be configured as basic look-up table, arithmetic logic unit, static random access memory, and read only memory according to application scenarios.

For more details on the CFU, please see *UG303, Arora V series Configurable Function Unit (CFU) User Guide*.

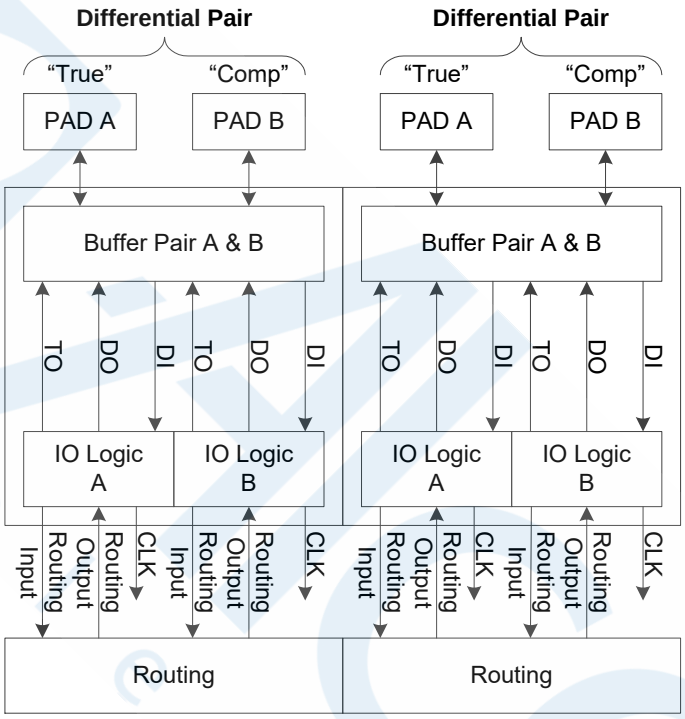
Figure 3-2 CFU View



3.3 Input/Output Block

The IOB in the Arora V series of FPGA Products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-3, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a single end input/output.

Figure 3-3 IOB Structure View



IOB Features:

- V_{CCO} supplied with each bank
- All banks support True differential input
- Supports multiple levels: LVCMOS, PCI, LVTTL, SSTL, HSTL, LVDS, Mini_LVDS, RSDS, PPDS, BLVDS
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SDR mode, and generic DDR mode

3.3.1 I/O Buffer

GW5AT-138 includes six GPIO Banks (Bank2~7), two SERDES Banks and a Bank for configuration (Bank 10), as shown in Figure 3-4. Bank 10 can also be used as I/O Bank.

GW5A-138 includes six GPIO Banks (Bank2~7) and a Bank for configuration (Bank 10), as shown in Figure 3-5. Bank 10 can also be used as I/O Bank.

Figure 3-4 Bank Distribution View of Arora V (GW5AT-138)

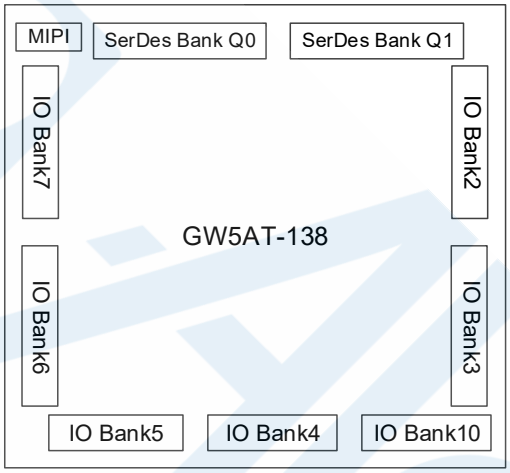
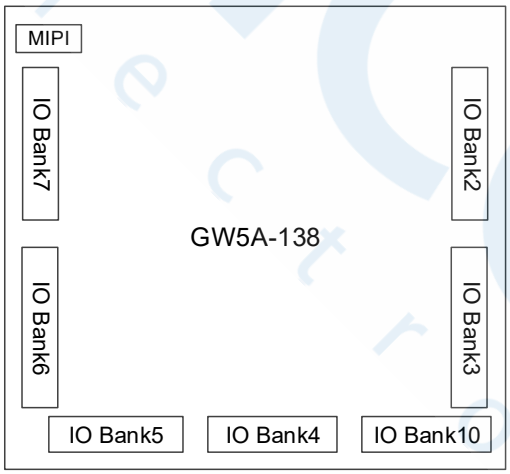
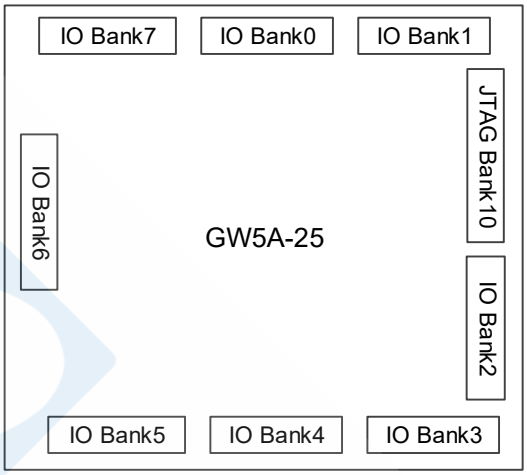


Figure 3-5 Bank Distribution View of Arora V (GW5A-138)



GW5A-25 includes nine GPIO Banks, as shown in Figure 3-6. One of the GPIO Banks is JTAG Bank, including four IOs.

Figure 3-6 Bank Distribution View of Arora V (GW5A-25)



Each Bank has independent I/O power supply V_{CCO}. V_{CCO} can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, 1.2V, or 1V.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.675V, 0.75V, 0.9V, and (33%,42%,50%,58%)Vcco) or the external reference voltage using any IO from the bank.

Auxiliary voltage V_{CCX} is 1.8V only.

Different banks in the Arora V series of FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O. Differential resistor is set for LVDS/PPDS/ RSDS input. For more details, refer to *UG304, Arora V series Programmable IO (GPIO) User Guide*.

Note!

GPIO is tri-stated weak pull-up by default.

For the V_{CCO} requirements of different I/O standards, see Table 3-1.

Table 3-1 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Output Driver Strength (mA)	Typical Applications
LVDS25	Differential Pair (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
BLVDS25	Differential Pair (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	Multi-point high-speed data transmission
RSDS	Differential Pair (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	High-speed point-to-point data transmission
MINILVDS	Differential Pair (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	LCD timing driver interface and

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Output Driver Strength (mA)	Typical Applications
				column driver interface
PPLVDS	Differential Pair (TLVDS)	2.5/3.3	3.5/2.5/4.5/6	LCD row/column driver
LVDS25E	Differential	2.5	8/4/12/16/24	High-speed point-to-point data transmission
BLVDS25E	Differential	2.5	8/4/12/16/24	Multi-point high-speed data transmission
MLVDS25E	Differential	2.5	8/4/12/16/24	LCD timing driver interface and column driver interface
RSDS25E	Differential	2.5	8/4/12/16/24	High-speed point-to-point data transmission
LVPECL33E	Differential	3.3	8/4/12/16/24	Universal interface
HSUL12D	Differential	1.2	8/4/12	LPDDR2
HSUL12D_I	Differential	1.2	8/4/12	LPDDR2
HSTL15D_I	Differential	1.5	8/4/12/16	Memory interface
HSTL15D_II	Differential	1.5	8/4/12/16	Memory interface
HSTL18D_I	Differential	1.8	8/4/12/16	Memory interface
HSTL18D_II	Differential	1.8	8/4/12/16	Memory interface
SSTL135D	Differential	1.35	8/4/12	Memory interface
SSTL15D	Differential	1.5	8/4/12/16	Memory interface
SSTL18D_I	Differential	1.8	8/4/12/16/24	Memory interface
SSTL18D_II	Differential	1.8	8/4/12/16/24	Memory interface
LVCMOS10D	Differential	1.0	4	Universal interface
LVCMOS12D	Differential	1.2	8/4/12	Universal interface
LVCMOS15D	Differential	1.5	8/4/12/16	Universal interface
LVCMOS18D	Differential	1.8	8/4/12/24[1]	Universal interface
LVCMOS25D	Differential	2.5	8/4/12/24[1]	Universal interface
LVCMOS33D	Differential	3.3	8/4/12/24[1]	Universal interface
HSUL12	Single end	1.2	8/4/12	Memory interface
HSTL12_I	Single end	1.2	8/4/12	Memory interface
HSTL15_I	Single end	1.5	8/4/12/16	Memory interface
HSTL15_ II	Single end	1.5	8/4/12/16	Memory interface
HSTL18_I	Single end	1.8	8/4/12/16/24	Memory interface
HSTL18_II	Single end	1.8	8/4/12/16/24	Memory interface
SSTL135	Single end	1.35	8/4/12	Memory interface
SSTL15	Single end	1.5	8/4/12/16	Memory interface

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Output Driver Strength (mA)	Typical Applications
SSTL18_I	Single end	1.8	8/4/12/16/24	Memory interface
SSTL18_II	Single end	1.8	8/4/12/16/24	Memory interface
LVCMOS10	Single end	1.0	4	Universal interface
LVCMOS12	Single end	1.2	8/4/12	Universal interface
LVCMOS15	Single end	1.5	8/4/12/16	Universal interface
LVCMOS18	Single end	1.8	8/4/12/16/24[1]	Universal interface
LVCMOS25	Single end	2.5	8/4/12/16/24[1]	Universal interface
LVCMOS33/LVTTL33	Single end	3.3	8/4/12/16/24[1]	Universal interface
LPDDR	Single end	1.8	8/4/12/16/24[1]	LPDDR and Mobile DDR
PCI33	Single end	3.3	8/4/12/16/24[1]	PC and embedded system

Note!

GW5A-25 does not support 24mA LVCMOS.

Table 3-2 Input I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
MIPI	Differential	1.2	No	No
LVDS25	Differential	2.5/1.0/1.2/1.5/1.8/3.3	No	No
RSDS	Differential	2.5/1.0/1.2/1.5/1.8/3.3	No	No
MINILVDS	Differential	2.5/1.0/1.2/1.5/1.8/3.3	No	No
PPLVDS	Differential	2.5/1.0/1.2/1.5/1.8/3.3	No	No
HSUL12D	Differential	1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL12D_I	Differential	1.2/1.0/1.5/1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL15D_II	Differential	1.5/1.0/1.2/1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL135D	Differential	1.35/1.0/1.2/1.5/1.8/2.5/3.3	No	No
SSTL15D	Differential	1.5/1.0/1.2/1.8/2.5/3.3	No	No
SSTL18D_I	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
LPDDRD	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
LVCMOS10D	Differential	1.0/1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS12D	Differential	1.2/1.0/1.5/1.8/2.5/3.3	No	No
LVCMOS15D	Differential	1.5/1.0/1.2/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/1.0/1.2/1.5/2.5/3.3	No	No
HSUL12	Single end	1.2	Yes	No

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
HSTL12_I	Single end	1.2	Yes	No
HSTL15_I	Single end	1.5	Yes	No
HSTL15_II	Single end	1.5	Yes	No
HSTL18_I	Single end	1.8	Yes	No
HSTL18_II	Single end	1.8	Yes	No
SSTL135	Single end	1.35	Yes	No
SSTL15	Single end	1.5	Yes	No
SSTL18_I	Single end	1.8	Yes	No
SSTL18_II	Single end	1.8	Yes	No
LVCMOS10	Single end	1.0	Yes	No
LVCMOS10UD12	Single end	1.2	Yes	No
LVCMOS10UD15	Single end	1.5	Yes	No
LVCMOS10UD18	Single end	1.8	Yes	No
LVCMOS10UD25	Single end	2.5	Yes	No
LVCMOS10UD33	Single end	3.3	Yes	No
LVCMOS12	Single end	1.2	Yes	No
LVCMOS15	Single end	1.5	Yes	No
LVCMOS15OD10	Single end	1.0	Yes	No
LVCMOS15OD12	Single end	1.2	Yes	No
LVCMOS15UD18	Single end	1.8	Yes	No
LVCMOS15UD25	Single end	2.5	Yes	No
LVCMOS15UD33	Single end	3.3	Yes	No
LVCMOS18	Single end	1.8	Yes	No
LVCMOS18OD10	Single end	1.0	Yes	No
LVCMOS18OD12	Single end	1.2	Yes	No
LVCMOS18OD15	Single end	1.5	Yes	No
LVCMOS18UD25	Single end	2.5	Yes	No
LVCMOS18UD33	Single end	3.3	Yes	No
LVCMOS25	Single end	2.5	Yes	No
LVCMOS25UD33	Single end	3.3	No	No
LVCMOS33/ LVTTL33	Single end	3.3	Yes	No
LVCMOS33OD25	Single end	2.5	Yes	No
LPDDR	Single end	1.8	Yes	No
PCI33	Single end	3.3	Yes	No
VREF1_DRIVER	Single end	1.8/1.2/1.35/1.5	No	Yes

3.3.2 I/O Logic

Figure 3-7 shows the I/O logic output of Arora V series of FPGA Products.

Figure 3-7 I/O Logic Output

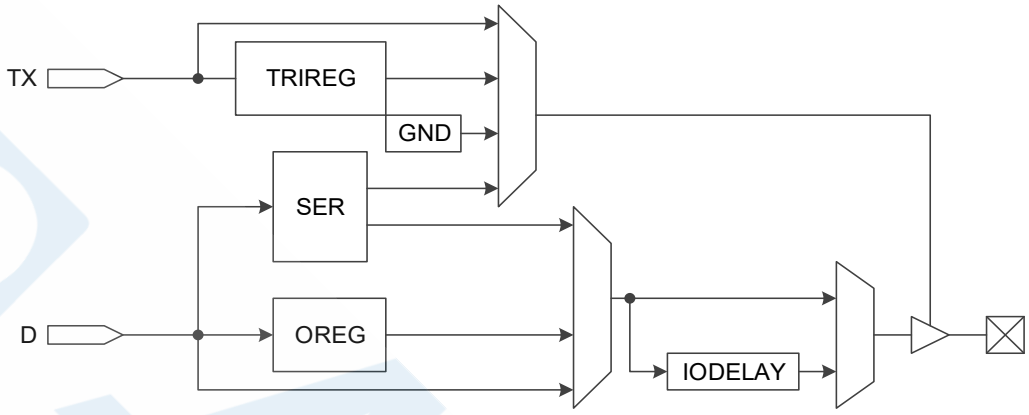


Figure 3-8 shows the I/O logic input of the Arora V series of FPGA Products.

Figure 3-8 I/O Logic Input

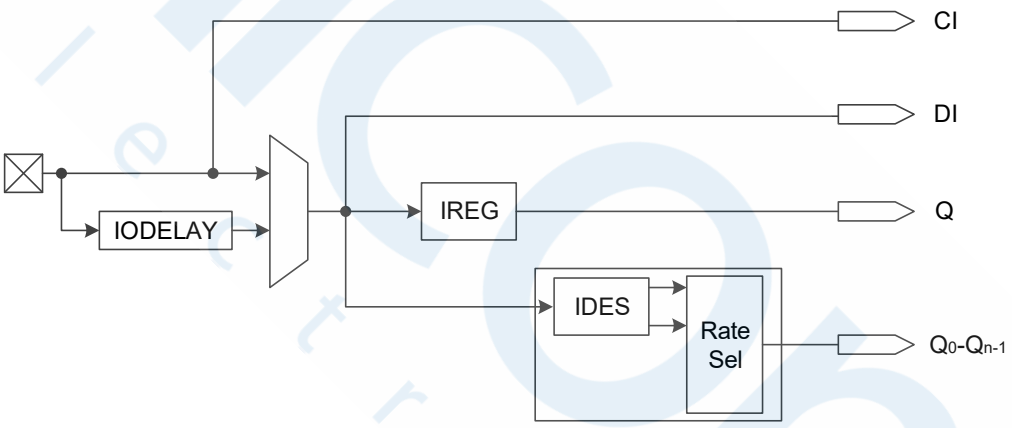


Table 3-3 Port Description

Port Name	I/O	Description
CI[1]	Input	GCLK Input Signal For the number of GCLK input signals, refer to *UG982, GW5AT-138 Pinout*.
DI	Input	IO port low-speed input signal, entering into Fabric directly.
Q	Output	IREG output signal in SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in DDR module.

Note!

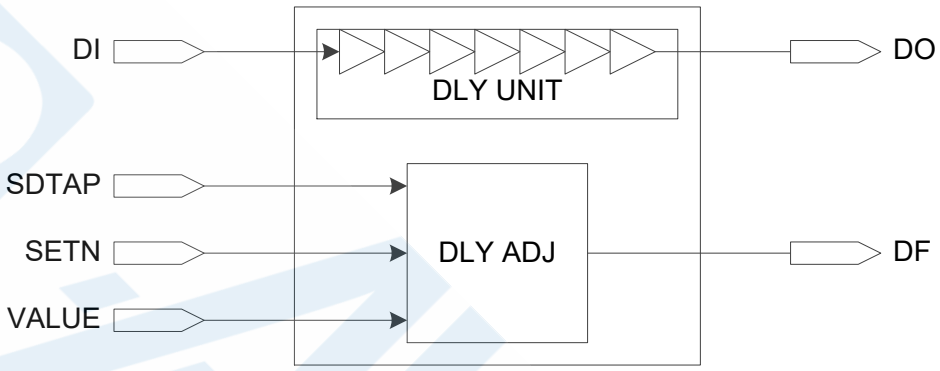
When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

Descriptions of the I/O logic modules of Arora V series of FPGA Products are presented below.

Delay Module

See Figure 3-9 for an overview of the IODELAY. Each I/O of Arora V includes IODELAY, providing a total of 128 (0~127) delays, with a single-step delay time of about 18ps.

Figure 3-9 IODELAY



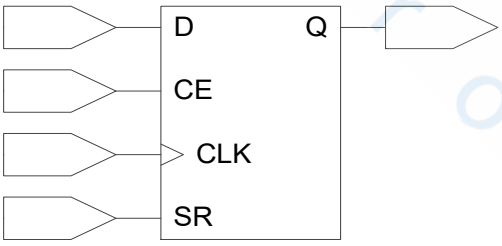
There are three ways to control the delay cell:

- Static control.
- Dynamic control: can be realized by combing the integrated logic circuit.
- Adaptive control

I/O Register

See Figure 3-10 for the I/O register in Arora V series of FPGA Products. Each I/O provides one input register (IREG), one output register (OREG), and a tristate Register (TREG).

Figure 3-10 Register Structure in I/O Logic



Note!

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as DFF or latch.

De-serializer DES and Clock Domain Transfer

The Arora V series of FPGA Products provide a simple De-serializer DES for each input I/O to support advanced I/O protocols. The clock domain transfers module of the input clock in DES provides the ability to safely switch the external sampling clock to the internal continuous running clock. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. The function is applied to the interface of DDR memory.
- For the DDR3 memory interface standard, align the data after DQS read-leveling.
- In regular DDR mode, when DQS.RCLK is used for sampling, clock domain transfer module also needs to be used.

Each DQS provides WADDR and RADDR signals to the same group in the clock domain transfer module.

Serializer SER

The Arora V series of FPGA Products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

IDES and OSER

The Arora V series of FPGA Products support serialization and deserialization of various ratios, as shown in the following table:

Table 3-4 Serialization and deserialization ratio modes supported by The Arora V series of FPGA Products

IOL type	ratio modes supported
IOL single	IDES：SDR/ 1:2/ 1:4/ 1:7/ 1:8/ 1:10/ 1:14/1:16 OSER：SDR/2:1/4:1/7:1/8:1/
IOL pair	IDES: 1:32 OSER: 10:1/16:1/14:1[1]

Note!

14:1 OSER is only supported on GW5A-25.

3.3.3 I/O Logic Modes

The I/O Logic in Arora V series of FPGA Products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

For more details, see *UG304, Arora V series Programmable Input/Output (GPIO) User Guide*.

3.4 Block SRAM (BSRAM)

3.4.1 Introduction

Arora V series of FPGA Products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array. Therefore, it is called block static random memory (BSRAM). Up to 36Kbits can be configured for each BSRAM. There are five operation modes: Single Port, Dual Port, Semi Dual Port, Semi Dual Port with ECC function, and ROM modes.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features:

- Max.36Kbits per BSRAM
- BSRAM itself can run at 380MHz at max (typical, Read-before-write is 230MHz)
- Support Single Port Mode
- Support Dual Port Mode
- Support Semi Dual Port Mode
- Supports ECC detection and error correction Function
- Support ROM Mode
- Data width up to 72bits
- Dual Port and Semi Dual Port support independent read/write clock and independent data width
- Read Mode supports register output or bypass output
- Write Mode supports Normal Mode, read-before-write Mode, write-through Mode

3.4.2 Configuration Mode

The BSRAM mode in the Arora V series of FPGA Products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Capacity	Single Port Mode	Dual Port Mode	Semi Dual Port Mode	Semi Dual Port with ECC function	Read Only
16Kbits	16K x 1	16K x 1	16K x 1	–	16K x 1
	8K x 2	8K x 2	8K x 2	–	8K x 2
	4K x 4	4K x 4	4K x 4	–	4K x 4
	2K x 8	2K x 8	2K x 8	–	2K x 8
	1K x 16	1K x 16	1K x 16	–	1K x 16
	512 x 32	–	512 x 32	–	512 x 32
18Kbits	2K x 9	2K x 9	2K x 9	–	2K x 9
	1K x 18	1K x 18	1K x 18	–	1K x 18

Capacity	Single Port Mode	Dual Port Mode	Semi Dual Port Mode	Semi Dual Port with ECC function	Read Only
	512 x 36	–	512 x 36	–	512 x 36
36Kbits	–	–	–	1K x 36	–
	–	–	–	512 x 72	–

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. Normal-Write Mode and Write-through Mode can be supported. In Normal-Write Mode, the written data will be stored in the internal memory array. In Write-through Mode, the written data will not only be stored in the internal memory array, but also be written to the output of BSRAM. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further description of the block diagram and related description in single port mode, please refer to *UG300, Arora V series BSRAM & SSRAM User Guide*.

Dual Port Mode

BSRAM supports Dual Port mode. The applicable operations are as follows:

- Two independent read, reading data from any given address.
- Two independent write, writing data to any address that is different.
- An independent read and an independent write at different clock frequencies.

Note!

- In Dual-port mode, Port A and Port B can read from or write to the same address. Null or repeated reads do not damage the storage module.
- In Dual-port mode, when Port A and Port B write to the same address at the same time, the dual ports writing fail at the same time.
- When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Dual Port supports independent read/write clocks and independent read/write data width. For further description of the block diagram and related description in dual port mode, please refer to *UG300, Arora V series BSRAM & SSRAM User Guide*.

Semi Dual Port Mode

Semi-dual ports support independent read/write operations in the form of A port write-only ("normal write mode") and B port read-only. When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Semi-dual Port supports independent read/write clocks and independent read/write data width. For further description of the block

diagram and related description in semi-dual port mode, please refer to *UG300, Arora V series BSRAM & SSRAM User Guide*.

Semi Dual Port Mode with ECC Function

Semi-dual ports with ECC Function support independent read/write operations in the form of A port write-only ("normal write mode") and B port read-only. This mode supports ECC error detection and correction. For further details, please refer to *UG300, Arora V series BSRAM & SSRAM User Guide*.

Read Only

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further description of the block diagram and details description in ROM mode, please refer to *UG300, Arora V series BSRAM & SSRAM User Guide*.

3.4.3 Data Bus Width Configuration

The BSRAM in the Arora V series of FPGA products supports independent data bus width of write/read operation. In the Dual Port, Semi Dual Port, Semi Dual Port with ECC function modes, the data bus width for read and write can be different. For the data width supported by Port A and Port B, see Table 3-6, Table 3-7, and Table 3-8.

Table 3-6 Read/Write Data Width Configuration in Dual Port Mode

Capacity	Port B	Port A						
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16Kbits	16K x 1	*	*	*	*	*	N/A	N/A
	8K x 2	*	*	*	*	*	N/A	N/A
	4K x 4	*	*	*	*	*	N/A	N/A
	2K x 8	*	*	*	*	*	N/A	N/A
	1K x 16	*	*	*	*	*	N/A	N/A
18Kbits	2K x 9	N/A	N/A	N/A	N/A	N/A	*	*
	1K x 18	N/A	N/A	N/A	N/A	N/A	*	*

Table 3-7 Read/Write Data Width Configuration in Semi Dual Port Mode

Capacity	Port B	Port A										
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x 32	2K x 9	1K x18	512 x 36	1K x 36	512 x 72
16Kbits	16K x 1	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A
	8K x 2	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A
	4K x 4	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A

Capacity	Port B	Port A										
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x 32	2K x 9	1K x18	512 x 36	1K x 36	512 x 72
	2K x 8	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A
	1K x 16	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A
	512 x 32	*	*	*	*	*	*	N/A	N/A	N/A	N/A	N/A
18Kbits	2K x 9	N/A	N/A	N/A	N/A	N/A	N/A	*	*	*	N/A	N/A
	1K x 18	N/A	N/A	N/A	N/A	N/A	N/A	*	*	*	N/A	N/A

Table 3-8 Read/Write Data Width Configuration in Semi Dual Port with ECC Function Mode

Capacity	Port B	Port A	
		1K x 36	512 x 72
36Kbits	1K x 36	*	N/A
	512 x 72	N/A	*

3.4.4 ECC (GW5A(T)-138)

The BSRAM of Arora V series GW5A(T)-138 FPGA products has a built-in ECC hardcore module, which is mainly used for data detection and correction during data transfer and storage. The features as follows:

- Supports ECC error detection and correction in SDP 512 x 64 and SDP 1024 x 36 modes only;
- Supports 1-bit error correction and 2-bit error alarm in 64-bit SRAM data;
- 72-bit ECC module contains 64-bit data bits and 8-bit parity bits;
- Support 1-bit and 2-bit error injection for bit 31 and bit 63.

3.4.5 Byte-enable

The BSRAM in the Arora V series of FPGA Products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The byte-enable function can only be used for writing and is available when the data width is 16/18, 32/36 bits. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte parameter options can be used to control the BSRAM write operation.

3.4.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write.
- The output register can be used as a pipeline register to improve design performance.
- The output registers are bypass-able.

3.4.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.4.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and read-before-write Mode).

Read Mode

Read data from the BSRAM via output registers or without using the registers.

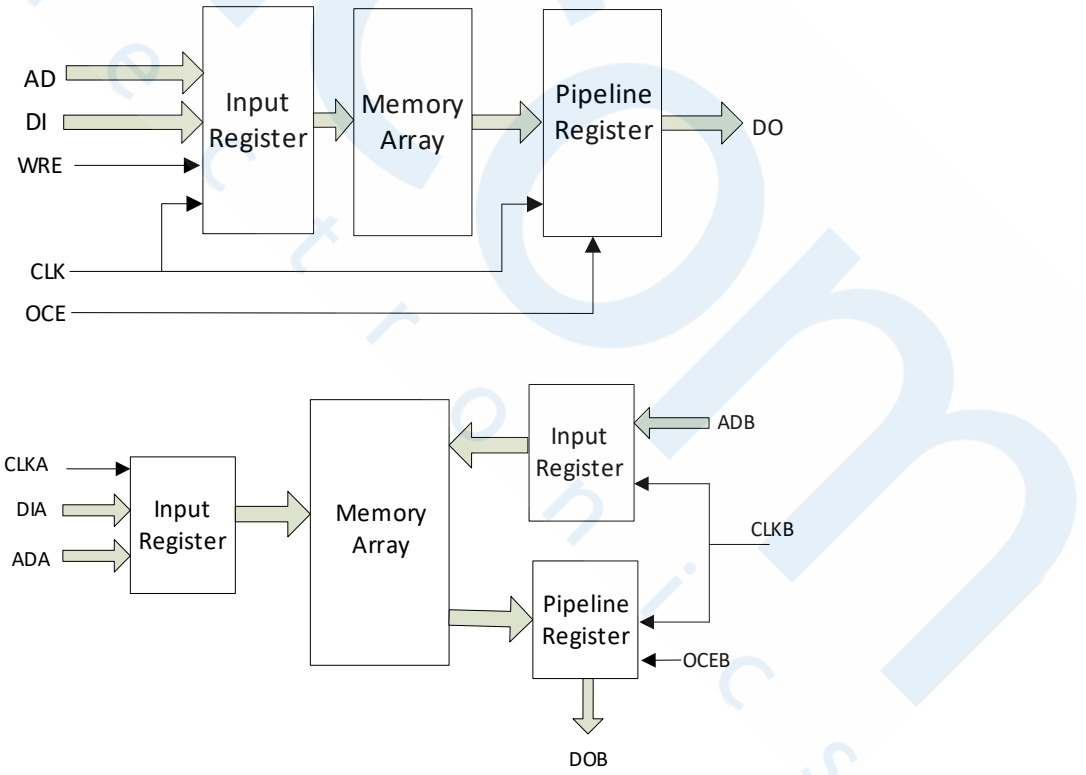
Pipeline Mode

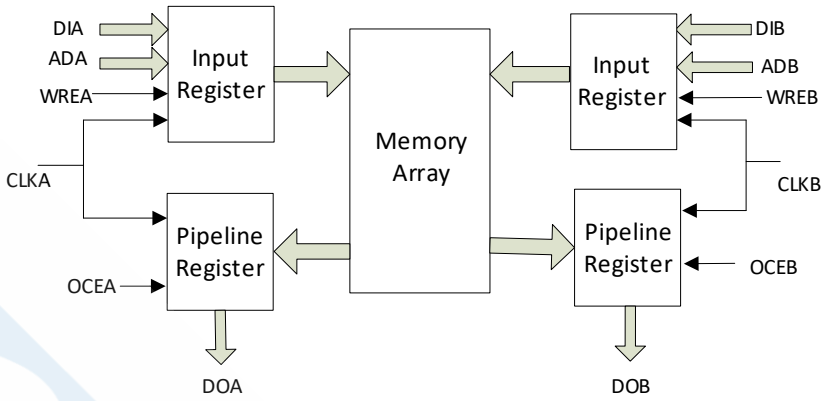
When reading data, the data is synchronously read out via the output register according to the clock beat. This mode supports up to 72-bit data width.

Bypass Mode

The output register is not used. When reading data, the data is directly sent to the output port.

Figure 3-11 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port





Write Mode

Normal Write Mode

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

Write-through Mode

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

Read-before-write Mode

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.4.9 Clock Operations

Table 3-9 lists the clock operations in different BSRAM modes:

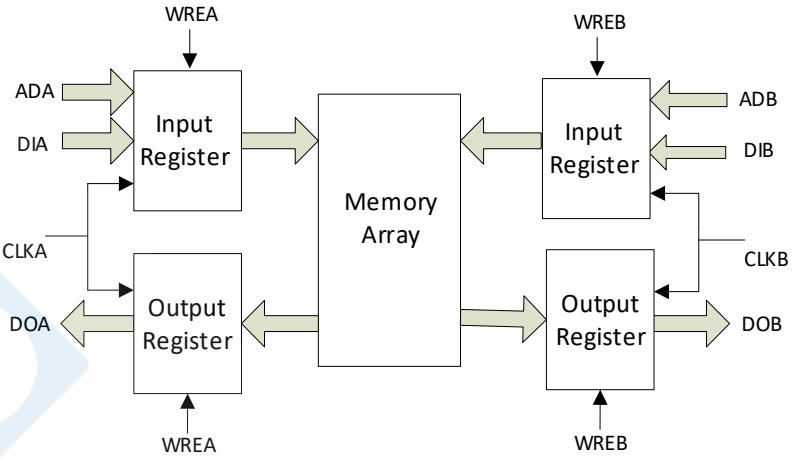
Table 3-9 Clock Operations in Different BSRAM Modes

Clock Operations	BSRAM Mode		
	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-12 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

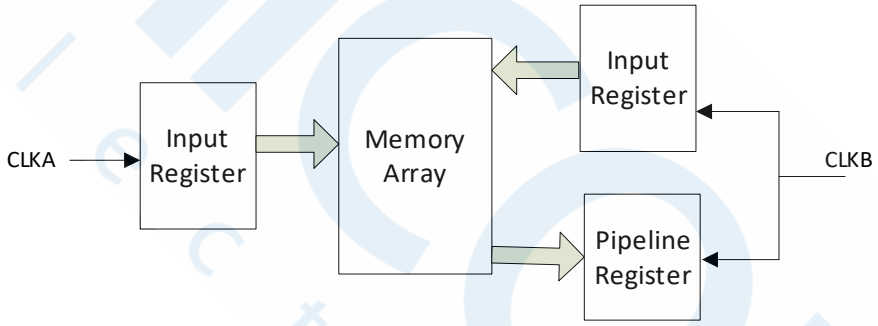
Figure 3-12 Independent Clock Mode



Read/Write Clock Operation

Figure 3-13 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

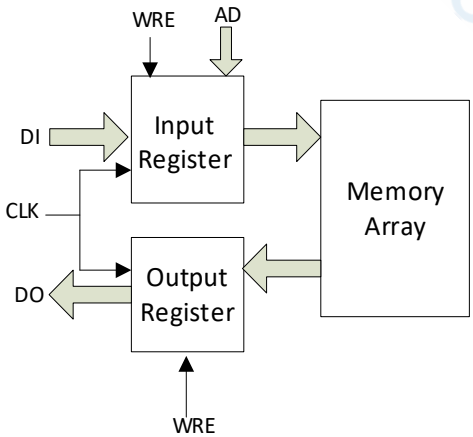
Figure 3-13 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-14 shows the clock operation in single port mode.

Figure 3-14 Single Port Clock Mode



3.5 DSP

Arora V series of FPGA Products integrate brand new DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

The DSP features are as follows:

- Can be configured as 12 x 12, 27 x 28, and 27 x 36 signed multipliers
- 48-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Supports pipeline mode and bypass mode
- Data is operated by signs
- All operands for arithmetic operation are signed numbers

Each DSP consists of three stages:

- Input multiplexer and input registers
- One pre-adder, two multipliers, and pipeline registers
- ALU, output multiplexers, and output registers

3.5.1 PADD

Each DSP features one PADD(pre-adder) to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs:

- 26-bit input C
- Parallel 26-bit input A or SIA

Each input end supports pipeline mode and bypass mode.

3.5.2 MULT

Each DSP has one 27 x 18 multiplier M0 and one 12 x 12 multiplier M1, locating after the pre-adder, which can further enhance MULT's functions. Registered Mode and Bypass Mode are supported both in input and output ports.

Multiplier M0 can be configured as:

- One 27 x 18 multiplier
- One 12 x 12 multiplier
- Two DSPs can form a 27 x 36 multiplier

Multiplier M1 can only be configured as one 12 x 12 multiplier.

When multiplier M0 and multiplier M1 are configured as both 12 x 12

multipliers and the ALU is enabled, 12 x 12SUM mode can be achieved.

3.5.3 ALU

Each Macro has one four-input 48-bit ALU, which can further enhance MULT's functions. The registered and bypass mode are supported both in input and output ports. The 56-bit ALU supports multiplier M0 output, multiplier M1 output (or 48bit operand D), ALU cascade input, and ALU output feedback or addition/subtraction operations of static PRE LOAD value.

3.5.4 Operating Mode

Based on control signals, DSP can be configured as different operation modes. Operation Modes:

- Multiplier
- Accumulator
- MULTADDALU

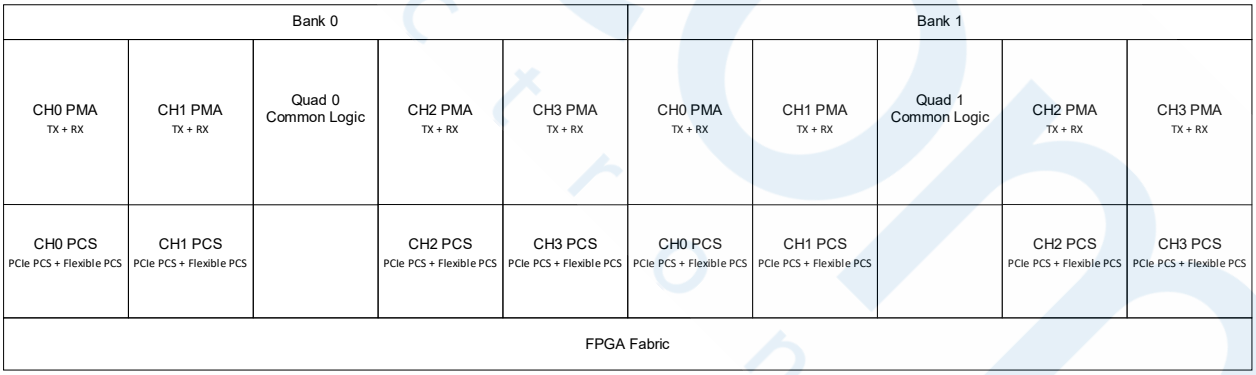
For further detailed information about the DSP, please refer to *UG305, Arora V series DSP User Guide*.

3.6 Gigabit Transceivers (GW5AT-138)

Gowin Arora V series of FPGA Products(GW5AT-138) support two Transceiver Quads. Each Quad supports up to four transceivers, and each transceiver is comprised of one TX and one RX, with the data rate raging from 270Mbps to 12.5Gbps, and supports flexible PMA and PCS. The structure View is as shown in Figure 3-15. The protocols supported are as follows:

- PCI Express, V2.0 (2.5 Gbps /5.0 Gbps)
- 10 Gigabit Attachment Unit Interface (XAUI) (3.125Gbps)
- RXAUI (Reduced XAUI) (6.25Gbps)
- CEI-6G-SR (6.375Gbps)
- SATA Rev3.2 (6Gbps/3Gbps/1.5Gbps) (need soft IP support)
- Serial GMII(SGMII) (1.25Gbps)
- CPRI (need soft IP support; soft IP available)
- JESD204B (need soft IP support; soft IP available)
- Rapid-IO (need soft IP support; soft IP available)
- 1000Base-X (need soft IP support; soft IP available)
- 10G-Base-R (need soft IP support; soft IP available)
- SDI-Tx/Rx (need soft IP support; soft IP available)
- SLVS-EC(Rx) (need soft IP support; soft IP available)

Figure 3-15 Gigabit Transceiver Architecture View



Physical Medium Attachment (PMA)

- Two shared PLLs per Quad (one is LC PLL and the other is ring oscillator PLL).
- Transmitter through tracking of spread reference clock.
- Lane driver with programmable transmitter equalization with 1 tap pre-cursor and 1 tap post-cursor to improve signal integrity.
- Voltage mode/current mode lane driver with board AC coupling.

- Programmable continuous time linear equalizer (CTLE) with auto-adaption.
- Receiver CDR track SSC data and tolerance +/- 5000ppm variation.
- Beacon signaling generation and detection for PCI Express.

Physical Coding Sublayer (PCS)

- Dedicated hard PCIe PCS
- Flexible PCS to support PCS customization
- 8b/10b encoder/decoder
- Supports TX channel bonding
- Supports RX channel bonding and CTC
- Utilize IF FIFO to simply user system design
- Supports flexible parallel data widths of 8/10/16/20/32/40/64/80 bits

For further detailed information about Gowin Gigabit Transceiver, please refer to *UG299, Arora V series Gigabit Transceiver User Guide.*

3.7 PCIe 2.0 (GW5AT-138)

GW5AT-138 FPGA Products include one integrated block for PCI Express technology. It allows custom FPGA-to-FPGA communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fiber Channel HBAs (Host Bus Adapter), to the FPGA.

Features of the PCIe integrated block are as follows:

- Dedicated hard core IP, Compliant to the PCI Express Base Specification 2.0
- Supports x1, x2, x4, x8 lanes
- Supports Root Complex port and End Point
- Supports Gen1 (2.5Gb/s), Gen2 (5Gb/s)
- Up to six BARs, resizable
- Lane reversal
- Receiver supports polarity inversion
- Supports CrossLink connection mode
- Supports Multicast
- Supports ARI (Alternative Routing-ID Interpretation)
- Supports IDO (ID-based Ordering)
- Retimer (extension device) presence detection
- Supports TPH (TLP Processing Hints)
- Supports ACS (Access Control Services)

- Supports DPC (Downstream Port Containment)
- Supports PTM (Precision Time Measurement)
- Supports Autonomous link speed/width change
- Supports advanced configuration options, Advanced Error Reporting (AER), and End-to-End Cyclic Redundancy Check (ECRC)
- Configurable parameters: channel width, maximum payload size, FPGA logical interface speeds, reference clock frequency, base address register decoding and filtering, etc.

For more details on PCIe 2.0, please refer to *UG298, Arora V series Hardened PCIe Controller User Guide*.

3.8 MIPI D-PHY

3.8.1 MIPI D-PHY RX (GW5A(T)-138)

GW5A(T)-138 FPGA Products provide a MIPI D-PHY RX hardcore supporting MIPI Alliance Standard for D-PHY Specification V1.2. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features of the MIPI D-PHY RX hardcore are as follows:

- High Speed RX at up to 20 Gbps (eight data channels).
- One Bank supports up to four data lanes and one clock lane. Up to two banks supported.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers

For further detailed information on Gowin MIPI D-PHY RX/TX, pleae refer to *UG296, Arora V series Hardened MIPI D-PHY RX User Guide.*

3.8.2 MIPI D-PHY RX/TX(GW5A-25)

GW5A-25 FPGA Products provide a MIPI D-PHY RX/TX hardcore supporting MIPI Alliance Standard for D-PHY Specification V1.2. The dedicated D-PHY core supports MIPI DSI (Display Serial Interface) and CSI-2 (Camera Serial Interface) mobile video interfaces for cameras and displays. The main features of the MIPI D-PHY RX/TX hardcore are as follows:

- High Speed RX/TX up to 10 Gbps with four data lanes.
- Supports up to four data lanes and one clock lane.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface

- Supports MIPI DSI and MIPI CSI-2 link layers

For further detailed information on Gowin MIPI D-PHY RX/TX, pleae refer to *UG296，Arora V series Hardened MIPI D-PHY RX User Guide*.

3.9 Analog to Digital Converter (ADC)

Arora V integrates a new flexible analog interface as temperature and power sensor. When combined with the programmable logic capability of the FPGA, the sensor can address the data acquisition and monitoring requirements for temperature and power monitoring.

Highlights of the sensor architecture include:

- On-chip reference, no off-chip voltage reference required
- 60dB SNR
- 10-bit oversampling @ 2MHz
- 1kHz Signal Bandwidth
- two dedicated analog channels, able to detect input signals from GPIO at the same time
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous access to ADC measurements

The sensor optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails.

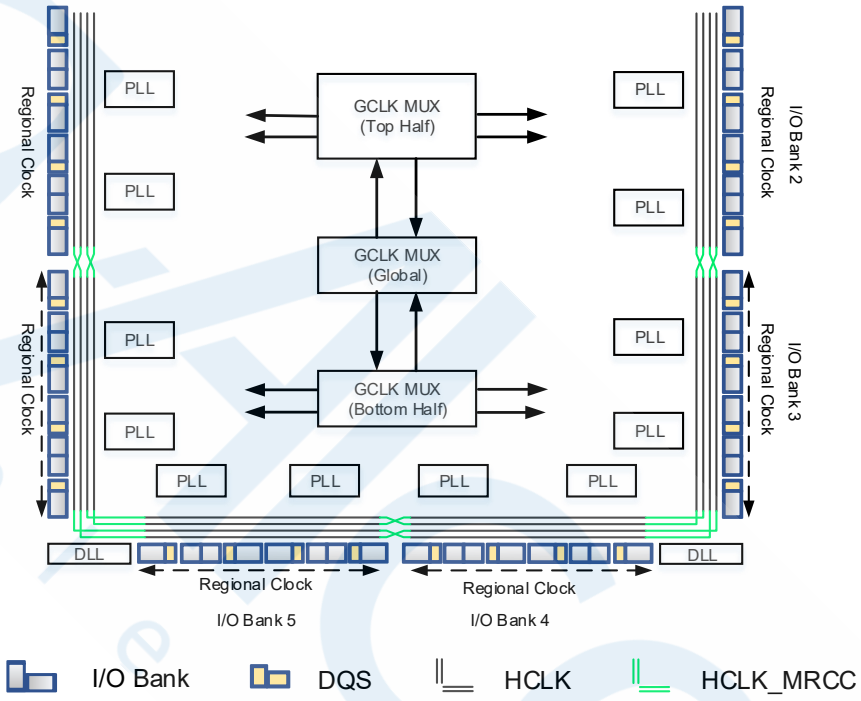
The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the user interface.

For further detailed information about ADC, please refer to *UG299, Arora V series ADC User Guide*.

3.10 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. Arora V series of FPGA Products provide the global clock network (GCLK) which connects to all the registers directly. Besides GCLK, clock resources such as PLL, high speed clock HCLK, DDR memory interface, and DQS, etc are also provided.

Figure 3-16 Arora V series Clock Resources



Please refer to 3.10.1 ~ 3.10.4 for a brief introduction. For further detailed information on the GCLK, HCLK, DDR memory interface, and DQS, please refer to *UG306, Arora V series Clock User Guide*.

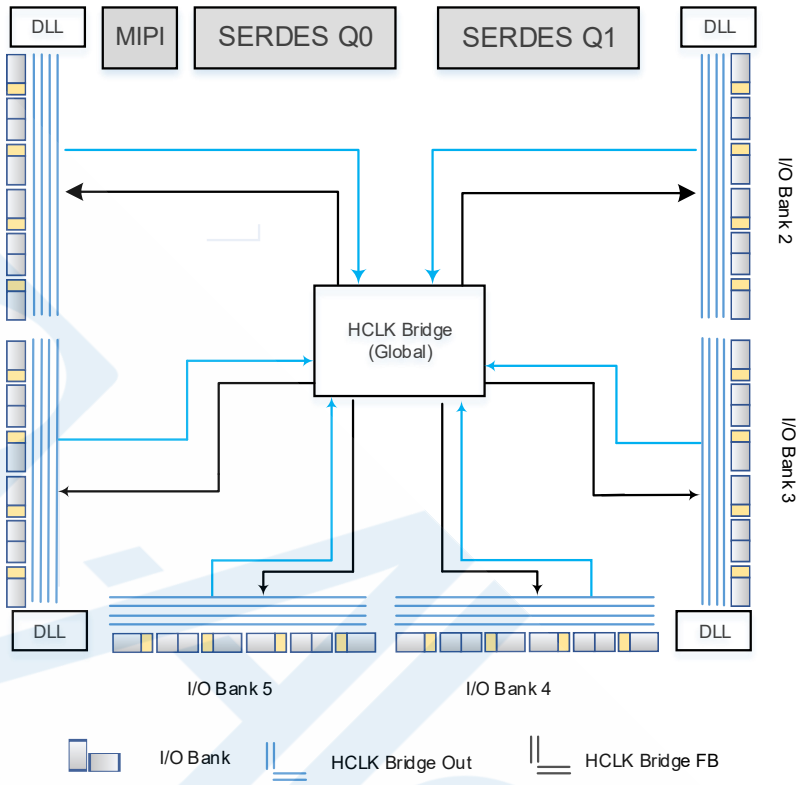
3.10.1 Global Clock

The GCLKs are distributed as 8 clock regions in Arora V series of FPGA Products. Each Clock provides 16 GCLKs. The clock sources of GCLK include dedicated clock pins, PLL output, SERDES clock, HCLK output, and common routing resources. You can use dedicated pins as clock resources to achieve better clock performance.

3.10.2 HCLK

HCLK is the high-speed clock in the Arora V series of FPGA Products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-17.

Figure 3-17 GW5AT HCLK Distribution



As shown in Figure 3-17, through the global high-speed clock HCLK bridge MUX module in the center of the device, the HCLK signal can be sent to any bank. In addition, the HCLK signal can also cross into the clock tree of the adjacent IO Bank after entering from the IO Bank (not shown in the above figure). The above features make the use of HCLK more flexible.

GCLK/HCLK can provide users with the function modules as follows:

- Dynamic high-speed clock enable module. Able to dynamically turn on/off high-speed clock signal.
- High speed clock frequency division module, generating a divided clock of the input clock. Used in the IO logic mode.
- Dynamic high speed clock selector.
- Dynamic delay adjustment module, producing the clock signal for the dedicated clock pin input.

3.10.3 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks in the Arora V series FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

PLL features are as follows:

- Supports seven clock output channels
- Integer PLL, the first lane and feedback clock output support 1/8 fractional output divider
- Phase shift and duty cycle adjustment supported
- Frequency Lock detection
- Supports spread spectrum clock generation
- VCO working Range: 800 MHz ~ 2000 MHz
- CLKIN frequency range: 10 MHz~400 MHz

3.10.4 DDR Memory Interface Clock Management DQS

DQS module of the Arora V series of FPGA Products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module supports multiple operating modes to meet the needs of different I/O interfaces.

3.11 Long Wire (LW)

As a supplement to the CRU, the Arora V series of FPGA Products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

3.12 Global Set/Reset (GSR)

A global set/rest (GSR) network is built in the Arora V series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

3.13 Programming Configuration

The Arora V series of FPGA Products support SRAM. Each time the device is powered on, the bit stream needs to be downloaded to configure the device. Users can select to keep backup data in external Flash chip according to requirements. After power-up, the Arora V device reads configuration data from external Flash and writes into the SRAM.

Besides JTAG, the Arora V series of FPGA Products also support

GOWINSEMI's own GowinCONFIG modes: SSPI, MSPI, CPU, and SERIAL. The FPGAs also support background programming, datastream file encryption and security bit setting, SEU detection and error correction, and OTP. For the detailed information, please refer to *UG704, Arora V series of FPGA Products Programming and Configuration User Guide*.

Background Programming

Arora V series of FPGAs support background programming by JTAG/SSPI/QSSPI or Fabric, that is, the device supports programming embedded Flash or external Flash operation without affecting the existing working state, the device can work normally according to the original configuration during the programming process. And after the programming is completed, trigger RECONFIG_N low to complete the online programming. This feature is suitable for applications with long online time but need to program from time to time.

Bitstream File Encryption & Security Bit Setting

Arora V series of FPGA products support bitstream data encryption with 128-bit AES encryption algorithm. At the same time, GOWINSEMI adds CRC and sets security bits in the bitstream file of FPGA products by default in order to guarantee the safe and accurate transmission of configuration data. During the data configuration process, the input data is verified in real time for errors, and the device cannot be woken up for incorrect data. After the configuration of the bitstream data with the security bit set, no user can perform a readback operation.

SEU Detection and Error Correction

The configuration SRAM of Arora V series FPGA products supports ECC and CRC, which are mainly used for data detection and correction of the FPGA configuration data and are disabled by default. With the following features.

- Support ECC and CRC error detection and correction, the chip turns on automatic mode according to the user configuration aftet wakeup or through the user design logic control to turn on/off error detection and correction
- Support 1-bit error location report and error correction per 64-bit SRAM data, 2-bit error alarm
- CRC supports multi-bit error alarm
- Support 1-bit arbitrary position error injection
- Automatically turn off the detection and correction of SRAM in the storage area when the user turns on the SSRAM storage function

OTP

Arora V series of FPGAs provide 128-bit of OTP space and support one-time programming. Bit0~Bit31 is the user area, which can be used by the system manufacturer to store security and other important information, and Bit32~Bit95 is the DNA area, where the 64-bit unique identification information of the memory device is stored.

3.14 On Chip Oscillator

There is an internal oscillator in each of the Arora V series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. See Table 3-10 for the output frequency. The following formula is employed to get the output clock frequency:

f_{out}=210MHz/Param.

Note!

"Param" is configuration parameter. It is 3 or an even number between 2 and 126.

Table 3-10 Oscillator Output Frequency Options

Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
1.67	2.56	5.53
1.69	2.63	5.83
1.72	2.69	6.18
1.75	2.76	6.56
1.78	2.84	7.00
1.81	2.92	7.50
1.84	3.00	8.08
1.88	3.09	8.75
1.91	3.18	9.55
1.94	3.28	10.50
1.98	3.39	11.67
2.02	3.50	13.13
2.06	3.62	15.00
2.10	3.75	17.50
2.14	3.89	21.00
2.19	4.04	26.25
2.23	4.20	35.00
2.28	4.38	52.50
2.33	4.57	70
2.39	4.77	105.00
2.44	5.00	-
2.50[1]	5.25	-

Note!

[1] Default output frequency is 2.5MHz.

4 AC/DC Characteristic

Note!

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage	-0.5V	1.05V
V_{CCO}	I/O Bank Voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	1.98V
V_{REF}	Input Voltage Reference	-0.5V	2V
V_{IN}	Single-ended input	-0.4V	3.75V
	Differential input	-0.4V	2.625V
Gigabit Transceiver			
V_{ddha}	Analog high power supply	-0.5V	1.98V
V_{dda}	Analog core power supply	-0.5V	1.05V
$V_{dd\_ln0\sim 4}$	Tx power supply	-0.5V	1.05V
MIPI			
V_{dda}	Analog core power supply	-0.5V	1.05V
V_{ddx_dphy}	Analog high voltage power supply	-0.5V	1.98V
Temperature			
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃
Junction Temperature	Junction Temperature	-40 ℃	+125 ℃

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Range

Name	Description	Min.	Max.
V_{CC}	Core voltage	0.87V	1.0V
V_{CCO}	I/O Bank Voltage	1.0V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	1.89V
V_{IN}	Single-ended input	-0.2V	Vcco+0.2 V
	Differential input	-0.2V	1.98V
Gigabit Transceiver			
V_{ddha}	Analog high power supply	1.71V	1.89V
V_{dda}	Analog core power supply	0.87V	1.0V
V_{ddt}	Tx power supply	0.87V	1.0V
MIPI			
V_{dda}	Analog core power supply	0.87V	1.0V
V_{ddx_dphy}	Analog high voltage power supply	1.71V	1.89V
Temperature			
T_{JCOM}	Junction temperature Commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃
T_{JAUT}	Junction temperature Automotive operation	-40℃	+105℃

Note!

For the power supply information for different packages, please refer to *UG982, GW5AT-138 Pinout*.

4.1.3 Power Rising Slope

Table 4-3 Power Supply Ramp Rate

Name	Description	Min.	Typ.	Max.
T_{RAMP}	Power supply ramp rates	0.02mV/μs	-	50mV/μs

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I_{HS}	Input leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	I/O	TBD
I_{HS}	Input leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	TDI, TDO TMS,TCK	TBD

4.1.5 POR Specifications

Table 4-5 POR Paramrters

Name	Description	Name	Min.	Max.
POR Voltage	Power on reset voltage	V_{CC}	TBD	TBD
		V_{CCX}	TBD	TBD
		V_{CCIO}	TBD	TBD

4.2 Electro-Static Discharge (ESD)

Table 4-6 Arora V ESD - HBM

Device	GW5AT-138
TBD	TBD
TBD	TBD

Table 4-7 Arora V ESD - CDM

Device	GW5AT-138
TBD	TBD
TBD	TBD

4.3 DC Characteristic

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	TBD	TBD
		$0V<V_{IN}<V_{CCO}$	-	TBD	TBD
I_{PU}	I/O Active Pull-up Current (I/O Active Pull-up Current)	$0<V_{IN}<0.7V_{CCO}$	-	TBD	TBD
I_{PD}	I/O Active Pull-down Current (I/O Active Pull-up Current)	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	-	TBD	TBD
C1	I/O Capacitance (I/O Capacitance)	TBD	TBD	TBD	TBD
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCO}=3.3V, Hysteresis=L2H	-	250	TBD
		V_{CCO}=2.5V, Hysteresis=L2H	-	90	TBD
		V_{CCO}=1.8V, Hysteresis=L2H	-	50	TBD
		V_{CCO}=1.5V, Hysteresis=L2H	-	40	TBD
		V_{CCO}=1.2V, Hysteresis=L2H		40mV	TBD

Name	Description	Condition	Min.	Typ.	Max.
		V_{CCO}=3.3V, Hysteresis=H2L	-	310	TBD
		V_{CCO}=2.5V, Hysteresis=H2L	-	130	TBD
		V_{CCO}=1.8V, Hysteresis=H2L	-	50	TBD
		V_{CCO}=1.5V, Hysteresis=H2L	-	30	TBD
		V_{CCO}=1.2V, Hysteresis=H2L		30mV	TBD
		V_{CCO}=3.3V,Hysteresis=High	-	560	TBD
		V_{CCO}=2.5V,Hysteresis=High	-	220	TBD
		V_{CCO}=1.8V,Hysteresis=High	-	100	TBD
		V_{CCO}=1.5V,Hysteresis=High	-	70	TBD
		V_{CCO}=1.2V,Hysteresis=High		70mV	TBD

4.3.2 Static Current

Table 4-9 Static Current

Name	Description	LV/UV	Device	Typ.
I_{CC}	Core Current	LV	TBD	TBD
			TBD	TBD
I_{CCX}	V_{CCX} current (VCCX=2.5V)	LV	TBD	TBD
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	LV	TBD	TBD

4.3.3 Recommended I/O Operating Conditions

Table 4-10 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E[1]	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

Bank VCCO with True LVDS is recommended to set to 2.5V.

4.3.4 Single ended I/O DC Characteristic

Table 4-11 Single-ended DC Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.45V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.45V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.45V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.45V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.45V	0.4V	V_{CCO}-0.4V	2	-2
							4	-4
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS10	-0.3	0.35 x V_{CCO}	0.65 x V_{CCO}	1.1V	0.4V	V_{CCO}-0.4V	4	-4
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	V_{CCIO}+0.3	0.4V	V_{CCO}0.4V	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
SSTL135	-0.3	V_{REF}-0.09V	V_{REF}+0.09V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	V_{CCIO}+0.3	0.40V	V_{CCO}-0.40V	NA	NA
HSUL12	-0.3	V_{REF}-0.13V	V_{REF}+ 0.13V	V_{CCIO}+0.3	0.40	V_{CCO}-0.40V	0.1	-0.1

Note!

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

4.3.5 Differential I/O DC Characteristic

Table 4-12 Differential I/O DC Characteristic

Name	Description	Conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)	TBD	-0.4		2.625	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.3	1.2	1.5	V
V_{THD}	Differential Input Threshold	Difference Between the Two	±70	±200	±300	mV

Name	Description	Conditions	Min.	Typ.	Max.	Unit
		Inputs				
I_{IN}	Input Current	Power On or Power Off	TBD	TBD	TBD	μA
V_{OH}	Output High Voltage for VOP or VOM	R_T = 100Ω	TBD	TBD	1.675	V
V_{OL}	Output High Voltage for VOP or VOM	R_T = 100Ω	0.7	TBD	TBD	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	600	mV
ΔV_{OD}	Change in VOD Between High and Low	TBD	TBD	TBD	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.000	1.250	1.425	V
ΔV_{OS}	Change in VOS Between High and Low	TBD	TBD	TBD	TBD	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	TBD	TBD	TBD	mA

4.4 AC Switching Characteristic

4.4.1 CFU Switching Characteristic

Table 4-13 CFU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	TBD	ns
t_{SR_CFU}	Set/Reset to Register output	-	TBD	ns
t_{CO_CFU}	Clock to Register output	-	TBD	ns

4.4.2 BSRAM Switching Characteristic

Table 4-14 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	TBD	ns
t_{COOR_BSRAM}	Clock to output from output register	-	TBD	ns

4.4.3 DSP Switching Characteristic

Table 4-15 DSP Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from input register	-	TBD	ns
t_{COPR_DSP}	Clock to output from pipeline register	-	TBD	ns
t_{COOR_DSP}	Clock to output from output register	-	TBD	ns

4.4.4 Clock and I/O Switching Characteristic

Table 4-16 External Switching Characteristics

Name	Description	Device	-8		-7		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay(1)	Pin(IOxA) to Pin(IOxB) delay	GW5AT-138	-	TBD	-	TBD	ns
$T_{HCLKdly}$	HCLK tree delay	GW5AT-138	-	TBD	-	TBD	ns
$T_{GCLKdly}$	GCLK tree delay	GW5AT-138	-	TBD	-	TBD	ns

4.4.5 On chip Oscillator Switching Characteristic

Table 4-17 On chip Oscillator Switching Characteristic

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to 85℃)	TBD	TBD	TBD
	Output Frequency (-40 to +100℃)	TBD	TBD	TBD
t_{DT}	Output Clock Duty Cycle	TBD	TBD	TBD
t_{OPJIT}	Output Clock Period Jitter	TBD	TBD	TBD

4.4.6 PLL Switching Characteristic

Table 4-18 PLL Switching Characteristic

Device	Speed Grade	Name	Min.	Max.
GW5AT-138	TBD	CLKIN	TBD	TBD
		PFD	TBD	TBD
		VCO	TBD	TBD
		CLKOUT	TBD	TBD
	TBD	CLKIN	TBD	TBD
		PFD	TBD	TBD
		VCO	TBD	TBD
		CLKOUT	TBD	TBD

4.5 Configuration Interface Timing Specification

The Arora V series of FPGA Products support seven GowinCONFIG modes: SSPI, MSPI, SERIAL, and CPU. For more detailed information, please refer to *UG704, Arora V series of FPGA Products Programming and Configuration Guide*.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Naming Examples–ES

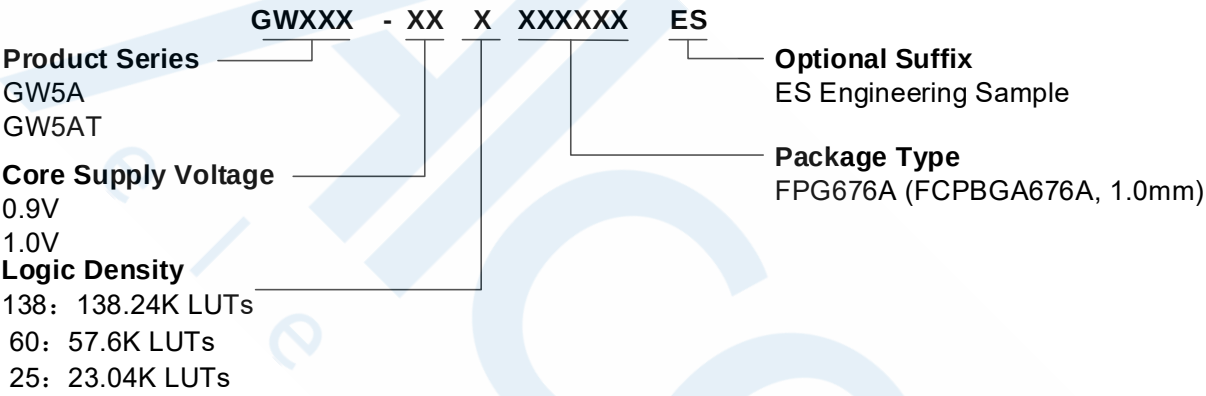
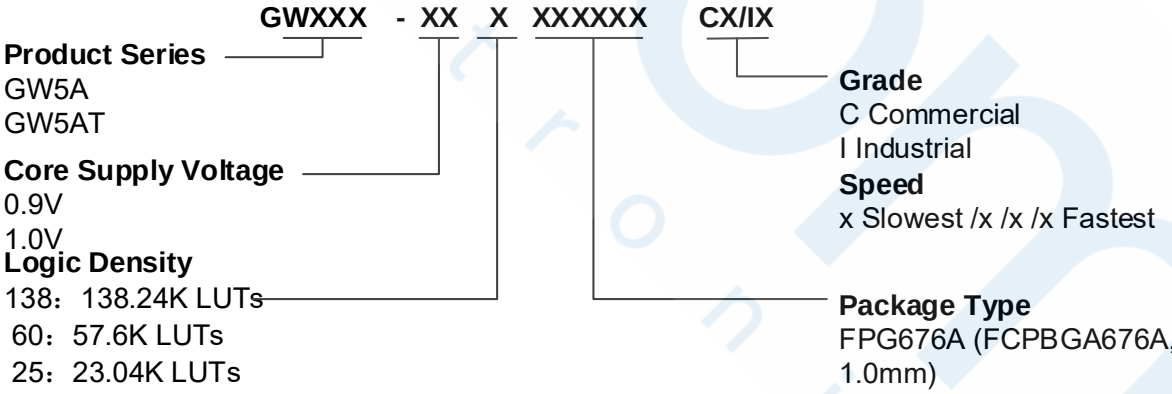


Figure 5-2 Part Naming Examples–Production



Note!

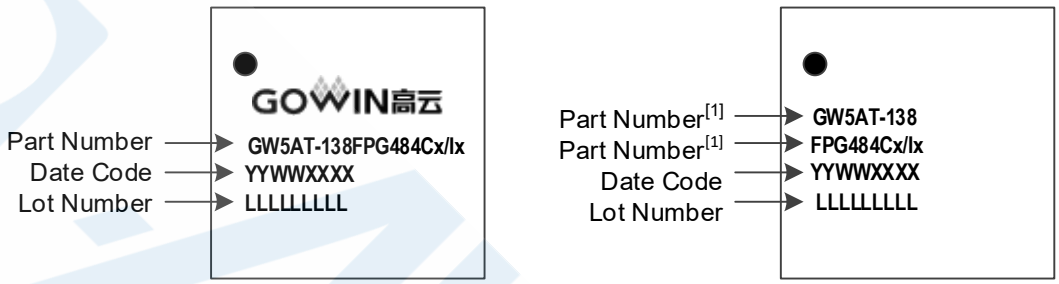
- For the further detailed information about the package information, please refer to Table 2-2_Package Information and Max. User I/O.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one device, such as C8/I7, C6/I5, etc. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The

maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the same chip meets the speed grade 8 in the commercial grade application, the speed grade is 7 in the industrial grade application.

5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

Figure 5-3 Package Mark Examples



Note!

[1] The first two lines in the right figure above are the “Part Number”.

Alcom electronics

Singel 3 | B-2550 Kontich | Belgium | Tel. +32 (0)3 458 30 33
info@alcom.be | www.alcom.be
Rivium 1e straat 52 | 2909 LE Capelle aan den IJssel | The Netherlands
Tel. +31 (0)10 288 25 00 | info@alcom.nl | www.alcom.nl

GOWIN
PROGRAMMING FOR THE FUTURE