V4/24

GigaDevice Semiconductor Inc.

GD32VW553xx
RISC-V 32-bit MCU

Datasheet

Revision 1.1

(Nov. 2023)

Singel 3 | B-2550 Kontich | Belgium | Tel. +32 (0)3 458 30 33
info@alcom.be | www.alcom.be
Rivium 1e straat 52 | 2909 LE Capelle aan den IJssel | The Netherlands
Tel. +31 (0)10 288 25 00 | info@alcom.nl | www.alcom.nl

Table of Contents

List of Figures

List of Tables

1. General description

The GD32VW553xx is a highly integrated 2.4GHz Wi-Fi and BLE System-on-Chip (SoC) that includes an RISC-V processor, a single stream IEEE 802.11b/g/n/ax MAC/baseband/radio, a power amplifier (PA), and a receive low-noise amplifier (LNA). It is an optimized SoC designed for a broad array of smart devices for Internet of Things (IoT) applications.

The GD32VW553xx device incorporates the RISC-V 32-bit processor core operating at 160 MHz frequency to obtain maximum efficiency. It provides up to 4096 KB on-chip Flash memory and 320KB (288 KB + 32KB Shared) SRAM memory. An extensive range of enhanced I/Os and peripherals connect to two APB buses. The devices offer a 12-bit ADCs, up to four general 16-bit timers, one basic timers, one PWM advanced timer, as well as standard and advanced communication interfaces: one SPI, two I2Cs, one USARTs, two UARTs, a Wireless (BLE / Wi-Fi). Additional peripherals as cryptographic acceleration unit (CAU), hash acceleration unit (HAU), public key cryptographic acceleration unit (PKCAU) and quad-SPI interface (QSPI) are included.

The device operates from a 1.8 to 3.6 V power supply and available in –40 to +85 °C temperature range for grade 6 devices, -40 to +105 °C temperature range for grade 7 devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32VW553xx devices suitable for a wide range of applications, especially in areas such as industrial control, smart home control system, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, IoT and so on.

2. Device overview

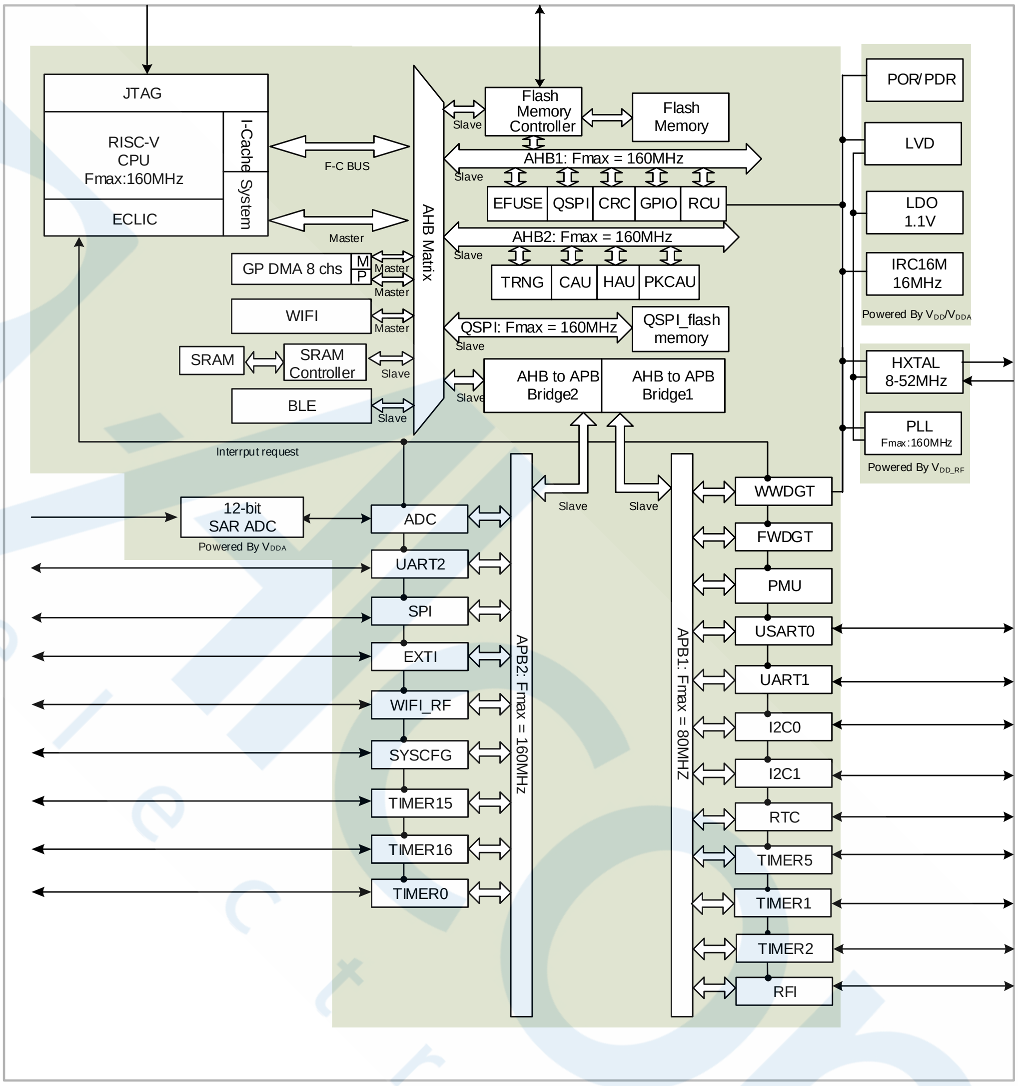
2.1. Device information

Table 2-1. GD32VW553xx devices features and peripheral list

Part Number		GD32VW553xx							
		KIQ6	KIQ7	KMQ6	KMQ7	HIQ6	HIQ7	HMQ6	HMQ7
FLASH (KB)		2048	2048	4096	4096	2048	2048	4096	4096
SRAM (KB)		320	320	320	320	320	320	320	320
Timers	General timer(16-bit)	2 (15-16)	2 (15-16)	2 (15-16)	2 (15-16)	2 (15-16)	2 (15-16)	2 (15-16)	2 (15-16)
	General timer(32-bit)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Basic timer(16-bit)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)
	SysTick(64-bit)	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	UART	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)
	I2C	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1
	QSPI	1	1	1	1	1	1	1	1
	Wi-Fi	1	1	1	1	1	1	1	1
	BLE5.2	1	1	1	1	1	1	1	1
TRNG		1	1	1	1	1	1	1	1
CAU		1	1	1	1	1	1	1	1
HAU		1	1	1	1	1	1	1	1
PKCAU		1	1	1	1	1	1	1	1
GPIO		21	21	21	21	28	28	28	28
ADC	Units	1	1	1	1	1	1	1	1
	Channels	9	9	9	9	9	9	9	9
Package		QFN32				QFN40			

2.2. Block diagram

Figure 2-1. GD32VW553xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32VW553Hx QFN40 pinouts

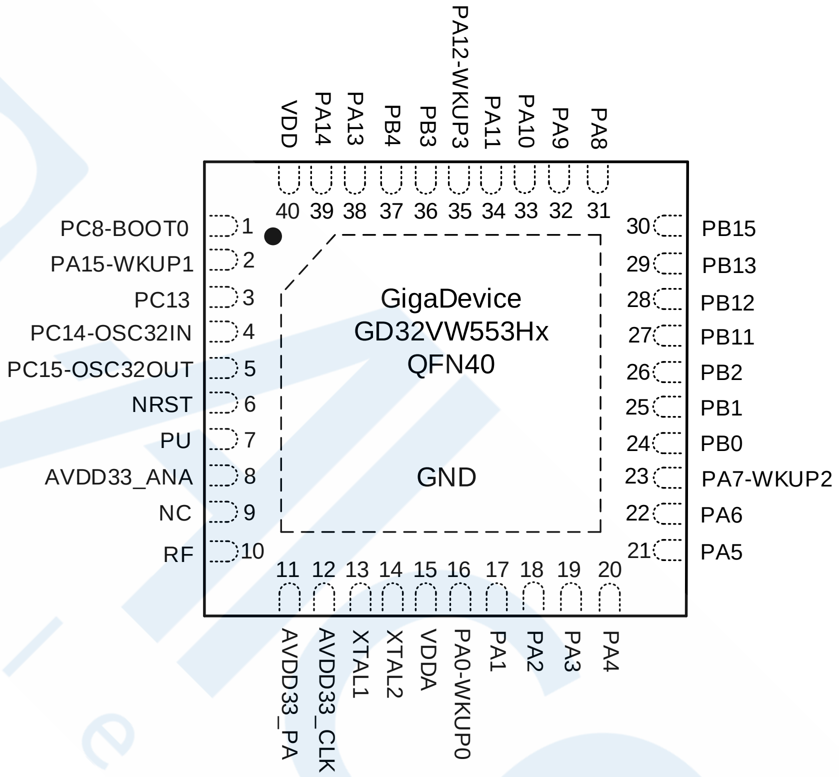
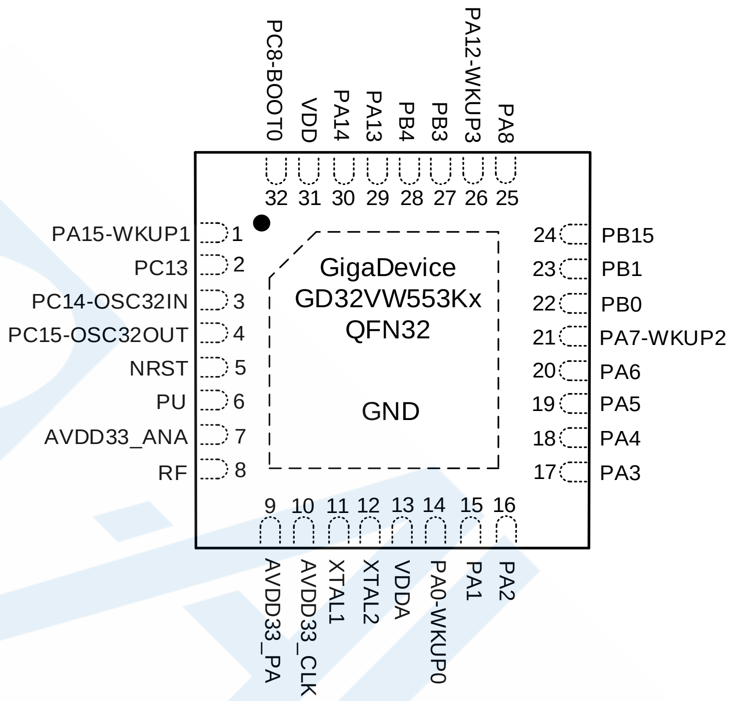


Figure 2-3. GD32VW553Kx QFN32 pinouts



2.4. Memory map

Table 2-2. GD32VW553xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xD100 0000 – 0xD200 10000	RISC-V internal peripherals
External device	QSPI	0x9800 0000 – 0xD0FF FFFF	Reserved
		0x9000 0000 - 0x97FF FFFF	QSPI_FLASH (MEM)
		0x7000 0000 - 0x8FFF FFFF	Reserved
		0x6000 0000 - 0x67FF FFFF	Reserved
Peripheral	AHB2	0x4C06 3000 - 0x4FFF FFFF	Reserved
		0x4C06 1000 - 0x4C06 2FFF	PKCAU
		0x4C06 0C00 - 0x4C06 0FFF	Reserved
		0x4C06 0800 - 0x4C06 0BFF	TRNG
		0x4C06 0400 - 0x4C06 07FF	HAU
		0x4C06 0000 - 0x4C06 03FF	CAU
		0x4C05 0400 - 0x4C05 FFFF	Reserved
		0x4C05 0000 - 0x4C05 03FF	Reserved
		0x4C04 0000 - 0x4C04 FFFF	Reserved
		0x4C00 0000 - 0x4C03 FFFF	Reserved
	AHB1	0x4904 0000 - 0x4BFF FFFF	Reserved
		0x4900 0000 - 0x4903 FFFF	Reserved
		0x400B 1000 - 0x48FF FFFF	Reserved
		0x400B 0800 - 0x400B 0FFF	Reserved
		0x400B 0400 - 0x400B 07FF	Reserved
		0x400B 0000 - 0x400B 03FF	Reserved
		0x400A 1000 - 0x400A FFFF	Reserved
		0x400A 0C00 - 0x400A 0FFF	Reserved
		0x400A 0800 - 0x400A 0BFF	Reserved
		0x400A 0400 - 0x400A 07FF	Reserved
		0x400A 0000 - 0x400A 03FF	Reserved
		0x4008 0400 - 0x4009 FFFF	Reserved
		0x4008 0000 - 0x4008 03FF	Reserved
		0x4003 0000 - 0x4007 FFFF	WIFI
		0x4002 BC00 - 0x4002 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	DMA
		0x4002 5C00 - 0x4002 5FFF	Reserved

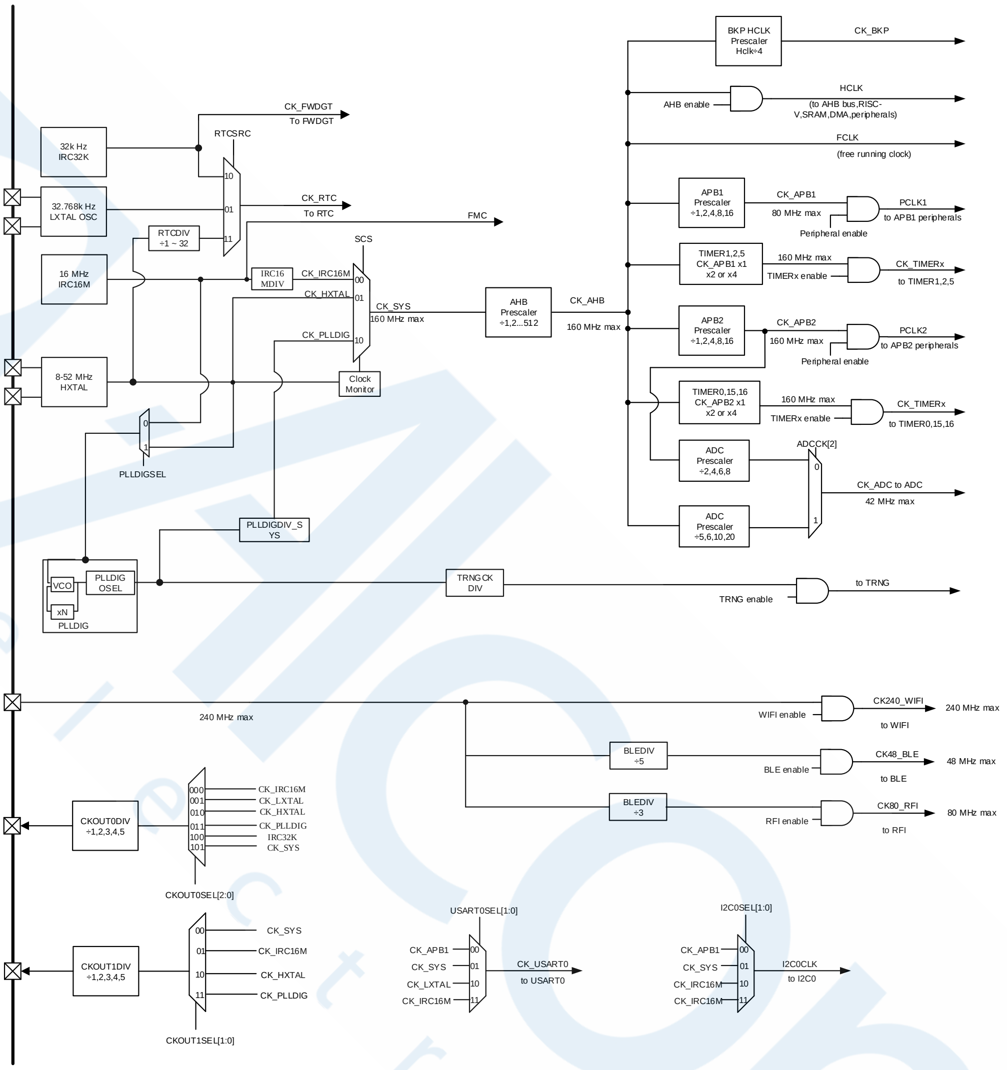
Pre-defined Regions	Bus	Address	Peripherals
		0x4002 5800 - 0x4002 5BFF	QSPI_FLASH(REG)
		0x4002 5400 - 0x4002 57FF	Reserved
		0x4002 5000 - 0x4002 53FF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	RCU
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	EFUSE
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	Reserved
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	GPIOC
		0x4002 0400 - 0x4002 07FF	GPIOB
		0x4002 0000 - 0x4002 03FF	GPIOA
	APB2	0x4001 8800 - 0x4001 FFFF	Reserved
		0x4001 8400 - 0x4001 87FF	TIMER16
		0x4001 8000 - 0x4001 83FF	TIMER15
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	WIFI_RF
		0x4001 6800 - 0x4001 77FF	Reserved
		0x4001 6000 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5FFF	Reserved
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 4C00 - 0x4001 53FF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	EXTI
		0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI
		0x4001 2C00 - 0x4001 2FFF	Reserved
		0x4001 2400 - 0x4001 2BFF	Reserved
		0x4001 2000 - 0x4001 23FF	ADC
		0x4001 1400 - 0x4001 1FFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4001 1000 - 0x4001 13FF	UART2
		0x4001 0800 - 0x4001 0FFF	Reserved
		0x4001 0400 - 0x4001 07FF	Reserved
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 D000 - 0x4000 FFFF	Reserved
		0x4000 CC00 - 0x4000 CFFF	RFI
		0x4000 7400 - 0x4000 CBFF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 5C00 - 0x4000 6BFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4C00 - 0x4000 53FF	Reserved
		0x4000 4800 - 0x4000 4BFF	USART0
		0x4000 4400 - 0x4000 47FF	UART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	Reserved
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	Reserved
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	Reserved
		0x4000 0800 - 0x4000 0BFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2101 0000 - 0x3FFF FFFF	Reserved
		0x2100 0000 - 0x2100 FFFF	BLE
		0x2005 0000 - 0x20FF FFFF	Reserved
		0x2003 0000 - 0x2004 FFFF	SRAM3 (96KB + shared 32KB)
		0x2002 0000 - 0x2002 FFFF	SRAM2 (64KB)
		0x2001 0000 - 0x2001 FFFF	SRAM1 (64KB)
		0x2000 0000 - 0x2000 FFFF	SRAM0 (64KB)
Code	AHB	0x1000 0000 - 0x1FFF FFFF	External memories remap
		0x0FFC 0100 - 0x0FFF FFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x0FFC 0000 - 0x0FFC 00FF	EFUSE (256 bytes)
		0x0BF8 0000 –0x0FFB FFFF	Reserved
		0x0BF4 0000 - 0x0BF7 FFFF	ROM(256KB)
		0x0A07 0000 - 0x0BF3 FFFF	Reserved
		0x0A04 0000 - 0x0A06 FFFF	Reserved
		0x0A02 0000 - 0x0A03 FFFF	Reserved
		0x0A01 0000 - 0x0A01 FFFF	Reserved
		0x0A00 0000 - 0x0A00 FFFF	Reserved
		0x0840 0000 - 0x09FF FFFF	Reserved
		0x0800 0000 - 0x083F FFFF	Flash memory
		0x0000 0000 - 0x07FF FFFF	External memories remap

2.5. Clock tree

Figure 2-4. GD32VW553xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillator

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32VW553Hx QFN40 pin definitions

Table 2-3. GD32VW553Hx QFN40 pin definitions

GD32VW553Hx QFN40				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC8-BOOT0	1	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, I2C0_SDA, I2C1_SDA, USART0_TX, UART1_TX, EVENTOUT Additional: BOOT0
PA15-WKUP1	2	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, I2C0_SCL, I2C1_SCL, USART0_RX, UART1_RX, EVENTOUT Additional: WKUP1
PC13	3	I/O	5VT	Default: PC13 Alternate: USART0_CK, EVENTOUT Additional: RTC_TAMP_0, RTC_OUT, RTC_TS
PC14-OSC32IN	4	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	5	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: OSC32OUT
NRST	6	I/O	-	Default: NRST
PU	7	-	-	Default: PU
AVDD33_ANA	8	P	-	Default: AVDD33_ANA
NC	9	-	-	-
RF	10	AI/AO		Default: RF
AVDD33_PA	11	P		Default: AVDD33_PA
AVDD33_CLK	12	P	-	Default: AVDD33_CLK
XTAL1	13	AI	-	Default: XTAL1
XTAL2	14	AO	-	Default: XTAL2
VDDA	15	P	-	Default: VDDA
PA0-WKUP0	16	I/O	5VT	Default: PA0 Alternate: USART0_TX, TIMER1_CH0, TIMER1_ETI, SPI_MOSI, UART1_CTS, TIMER0_ETI, EVENTOUT Additional: ADC_IN0, WAKEUP0, RTC_TAMP1
PA1	17	I/O	5VT	Default: PA1 Alternate: USART0_RX, TIMER1_CH1, SPI_MISO, UART1_RTS, EVENTOUT

GD32VW553Hx QFN40				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: ADC_IN1
PA2	18	I/O	5VT	Default: PA2 Alternate: USART0_CTS, TIMER1_CH2, I2C0_SCL, SPI_SCK, TIMER0_CH0, UART1_TX, EVENTOUT Additional: ADC_IN2
PA3	19	I/O	5VT	Default: PA3 Alternate: USART0_RTS, TIMER1_CH3, I2C0_SDA, SPI_NSS, TIMER0_CH0_ON, UART1_RX, RTC_OUT, EVENTOUT Additional: ADC_IN3
PA4	20	I/O	5VT	Default: PA4 Alternate: UART1_TX, SPI_MOSI, QSPI_SCK, SPI_NSS, TIMER0_CH1, EVENTOUT Additional: ADC_IN4
PA5	21	I/O	5VT	Default: PA5 Alternate: UART1_RX, TIMER2_ETI, QSPI_CSN, SPI_MISO, SPI_SCK, TIMER0_CH1_ON , EVENTOUT Additional: ADC_IN5
PA6	22	I/O	5VT	Default: PA6 Alternate: TIMER2_CH0, QSPI_IO0, I2C1_SCL, SPI_MISO, SPI_SCK, TIMER0_CH1, TIMER1_CH1, UART2_TX, EVENTOUT Additional: ADC_IN6
PA7-WKUP2	23	I/O	5VT	Default: PA7 Alternate: I2C1_SDA, TIMER0_CH0_ON, TIMER2_CH1, QSPI_IO1, SPI_NSS, SPI_MOSI, TIMER0_CH1_ON, UART2_RX, TIMER1_CH2, EVENTOUT Additional: ADC_IN7, WAKEUP2
PB0	24	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER0_CH0, TIMER0_CH2, UART1_TX, I2C0_SCL, TIMER2_ETI, TIMER16_CH0, UART2_CTS, TIMER0_BRKIN, EVENTOUT Additional: ADC_IN8
PB1	25	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER0_CH0_ON, TIMER2_CH2, UART1_RX, I2C0_SDA, TIMER16_CH0_ON, UART2_RTS, EVENTOUT Additional: BOOT1
PB2	26	I/O	5VT	Default: PB2 Alternate: TIMER1_CH3, TIMER2_CH3, UART1_CTS, TIMER0_ETI, TIMER16_BRKIN, EVENTOUT

GD32VW553Hx QFN40				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
PB11	27	I/O	5VT	Default: PB11 Alternate: CK_OUT1, TIMER1_CH2, TIMER0_CH1_ON, UART1_RTS, TIMER15_BRKIN, EVENTOUT
PB12	28	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN, TIMER0_CH3, TIMER1_CH2, I2C1_SCL, EVENTOUT
PB13	29	I/O	5VT	Default: PB13 Alternate: TIMER0_CH0_ON, TIMER1_CH3, I2C1_SDA, TIMER15_CH0, EVENTOUT
PB15	30	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER2_CH0, I2C0_SCL, I2C1_SCL, UART1_TX, USART0_TX, IFRP_OUT , EVENTOUT
PA8	31	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, USART0_RX, UART1_RX, I2C0_SDA, I2C1_SDA, USART0_CK, TIMER15_CH0, RTC_OUT, TIMER0_CH2_ON, EVENTOUT
PA9	32	I/O	5VT	Default: PA9 Alternate: SPI_MOSI, TIMER0_CH1, QSPI_SCK, USART0_TX, TIMER15_CH0_ON, EVENTOUT
PA10	33	I/O	5VT	Default: PA10 Alternate: SPI_MISO, TIMER0_CH2, QSPI_CSN, TIMER16_CH0, USART0_RX, EVENTOUT
PA11	34	I/O	5VT	Default: PA11 Alternate: SPI_SCK, TIMER0_CH3, QSPI_IO0, TIMER16_BRKIN, TIMER1_CH3, EVENTOUT
PA12-WKUP3	35	I/O	5VT	Default: PA12 Alternate: TIMER0_ETI, TIMER0_CH3, QSPI_IO1, SPI_NSS, USART0_CK, TIMER1_CH2, TIMER16_CH0_ON, EVENTOUT Additional: WKUP3
PB3	36	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, QSPI_IO2, USART0_RX, UART1_RX, TIMER15_BRKIN, EVENTOUT
PB4	37	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER1_CH0, TIMER1_ETI, QSPI_IO3, USART0_TX, UART1_TX, EVENTOUT
PA13	38	I/O	5VT	Default: JTMS, PA13 Alternate: I2C0_SMBA, I2C1_SCL, USART0_CTS, UART1_CTS, EVENTOUT
PA14	39	I/O	5VT	Default: JTCK, PA14 Alternate: I2C1_SMBA, I2C1_SDA, USART0_RTS, UART1_RTS, EVENTOUT

GD32VW553Hx QFN40				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
VDD	40	P	-	Default: VDD

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32VW553Kx QFN32 pin definitions

Table 2-4. GD32VW553Kx QFN32 pin definitions

GD32VW553Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA15-WKUP1	1	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, I2C0_SCL, I2C1_SCL, USART0_RX, UART1_RX, EVENTOUT Additional: WKUP1
PC13	2	I/O	5VT	Default: PC13 Alternate: USART0_CK, EVENTOUT Additional: RTC_TAMP_0, RTC_OUT, RTC_TS
PC14-OSC32IN	3	I/O	5VT	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: OSC32OUT
NRST	5	I/O		Default: NRST
PU	6	-		Default: PU
AVDD33_ANA	7	P		Default: AVDD33_ANA
RF	8	AI/AO		Default: RF
AVDD33_PA	9	P		Default: AVDD33_PA
AVDD33_CLK	10	P		Default: AVDD33_CLK
XTAL1	11	AI		Default: XTAL1
XTAL2	12	AO		Default: XTAL2
VDDA	13	P		Default: VDDA
PA0-WKUP0	14	I/O	5VT	Default: PA0 Alternate: USART0_TX, TIMER1_CH0, TIMER1_ETI, SPI_MOSI, UART1_CTS, TIMER0_ETI, EVENTOUT Additional: ADC_IN0, WAKEUP0, RTC_TAMP1
PA1	15	I/O	5VT	Default: PA1 Alternate: USART0_RX, TIMER1_CH1, SPI_MISO, UART1_RTS, EVENTOUT Additional: ADC_IN1
PA2	16	I/O	5VT	Default: PA2 Alternate: USART0_CTS, TIMER1_CH2, I2C0_SCL, SPI_SCK, TIMER0_CH0, UART1_TX, EVENTOUT Additional: ADC_IN2
PA3	17	I/O	5VT	Default: PA3 Alternate: USART0_RTS, TIMER1_CH3,

GD32VW553Kx QFN32				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				I2C0_SDA, SPI_NSS, TIMER0_CH0_ON, UART1_RX, RTC_OUT, EVENTOUT Additional: ADC_IN3
PA4	18	I/O	5VT	Default: PA4 Alternate: UART1_TX, SPI_MOSI, QSPI_SCK, SPI_NSS, TIMER0_CH1, EVENTOUT Additional: ADC_IN4
PA5	19	I/O	5VT	Default: PA5 Alternate: UART1_RX, TIMER2_ETI, QSPI_CSN, SPI_MISO, SPI_SCK, TIMER0_CH1_ON , EVENTOUT Additional: ADC_IN5
PA6	20	I/O	5VT	Default: PA6 Alternate: TIMER2_CH0, QSPI_IO0, I2C1_SCL, SPI_MISO, SPI_SCK, TIMER0_CH1, TIMER1_CH1, UART2_TX, EVENTOUT Additional: ADC_IN6
PA7-WKUP2	21	I/O	5VT	Default: PA7 Alternate: I2C1_SDA, TIMER0_CH0_ON, TIMER2_CH1, QSPI_IO1, SPI_NSS, SPI_MOSI, TIMER0_CH1_ON, UART2_RX, TIMER1_CH2, EVENTOUT Additional: ADC_IN7, WAKUP2
PB0	22	I/O	5VT	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER0_CH0, TIMER0_CH2, UART1_TX, I2C0_SCL, TIMER2_ETI, TIMER16_CH0, UART2_CTS, TIMER0_BRKIN, EVENTOUT Additional: ADC_IN8
PB1	23	I/O	5VT	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER0_CH0_ON, TIMER2_CH2, UART1_RX, I2C0_SDA, TIMER16_CH0_ON, UART2_RTS, EVENTOUT Additional: BOOT1
PB15	24	I/O	5VT	Default: PB15 Alternate: RTC_REFIN, TIMER0_CH2_ON, TIMER2_CH0, I2C0_SCL, I2C1_SCL, UART1_TX, USART0_TX, IFRP_OUT , EVENTOUT
PA8	25	I/O	5VT	Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, USART0_RX, UART1_RX, I2C0_SDA, I2C1_SDA, USART0_CK, TIMER15_CH0, RTC_OUT, TIMER0_CH2_ON , EVENTOUT
PA12-WKUP3	26	I/O	5VT	Default: PA12

GD32VW553Kx QFN32				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER0_ETI, TIMER0_CH3, QSPI_IO1, SPI_NSS, USART0_CK, TIMER1_CH2, TIMER16_CH0_ON, EVENTOUT Additional: WKUP3
PB3	27	I/O	5VT	Default: JTDO, PB3 Alternate: TIMER1_CH1, QSPI_IO2, USART0_RX, UART1_RX, TIMER15_BRKIN, EVENTOUT
PB4	28	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER1_CH0, TIMER1_ETI, QSPI_IO3, USART0_TX, UART1_TX, EVENTOUT
PA13	29	I/O	5VT	Default: JTMS, PA13 Alternate: I2C0_SMBA, I2C1_SCL, USART0_CTS, UART1_CTS, EVENTOUT
PA14	30	I/O	5VT	Default: JTCK, PA14 Alternate: I2C1_SMBA, I2C1_SDA, USART0_RTS, UART1_RTS, EVENTOUT
VDD	31	P		Default: VDD
PC8-BOOT0	32	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, I2C0_SDA, I2C1_SDA, USART0_TX, UART1_TX, EVENTOUT Additional: BOOT0

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.3. GD32VW553xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	USART0_TX	TIMER1_CH0/TIMER1_ETI				SPI_MOSI		UART1_CTS		TIMER0_ETI						EVENTOUT
PA1	USART0_RX	TIMER1_CH1				SPI_MISO		UART1_RTS								EVENTOUT
PA2	USART0_CTS	TIMER1_CH2			I2C0_SCL	SPI_SCK	TIMER0_CH0	UART1_TX								EVENTOUT
PA3	USART0_RTS	TIMER1_CH3			I2C0_SDA	SPI_NSS	TIMER0_CH0_ON	UART1_RX		RTC_OUT						EVENTOUT
PA4	UART1_TX		SPI_MOSI	QSPI_SCK		SPI_NSS			TIMER0_CH1							EVENTOUT
PA5	UART1_RX		TIMER2_ETI	QSPI_CSN	SPI_MISO	SPI_SCK			TIMER0_CH1_ON							EVENTOUT
PA6			TIMER2_CH0	QSPI_IO0	I2C1_SCL	SPI_MISO		SPI_SCK	TIMER0_CH1	TIMER1_CH1	UART2_TX					EVENTOUT
PA7	I2C1_SDA	TIMER0_CH0_ON	TIMER2_CH1	QSPI_IO1	SPI_NSS	SPI_MOSI	TIMER0_CH1_ON		UART2_RX	TIMER1_CH2						EVENTOUT
PA8	CK_OUT0	TIMER0_CH0	USART0_RX	UART1_RX		I2C0_SDA	I2C1_SDA	USART0_CK	TIMER15_CH0	RTC_OUT	TIMER0_CH2_ON					EVENTOUT
PA9	SPI_MOSI	TIMER0_CH1			QSPI_SCK			USART0_TX	TIMER15_CH0_ON							EVENTOUT
PA10	SPI_MISO	TIMER0_CH2			QSPI_CSN			TIMER16_CH0	USART0_RX							EVENTOUT
PA11	SPI_SCK	TIMER0_CH3			QSPI_IO0			TIMER16_BRKIN		TIMER1_CH3						EVENTOUT
PA12		TIMER0_ETI	TIMER0_CH3		QSPI_IO1		SPI_NSS	USART0_CK		TIMER1_CH2	TIMER16_CH0_ON					EVENTOUT
PA13	JTMS				I2C0_SMBA		I2C1_SCL	USART0_CTS	UART1_CTS							EVENTOUT
PA14	JTCK				I2C1_SMBA		I2C1_SDA	USART0_RTS	UART1_RTS							EVENTOUT
PA15	JTDI	TIMER1_CH0/TIMER1_ETI			I2C0_SCL		I2C1_SCL	USART0_RX	UART1_RX							EVENTOUT

Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON	TIMER0_CH0	TIMER0_CH2	UART1_TX		I2C0_SCL		TIMER2_ETI	TIMER16_CH0	UART2_CTS	TIMER0_BRKIN				EVENTOUT(1)
PB1		TIMER0_CH2_ON	TIMER0_CH0_ON	TIMER2_CH2	UART1_RX		I2C0_SDA			TIMER16_CH0_ON	UART2_RTS					EVENTOUT(1)
PB2		TIMER1_CH3		TIMER2_CH3	UART1_CTS				TIMER0_ETI	TIMER16_BRKIN						EVENTOUT(1)
PB3	JTDO	TIMER1_CH1		QSPI_IO2				USART0_RX	UART1_TX			TIMER15_BRKIN				EVENTOUT
PB4	NJTRST	TIMER1_CH0/TIMER1_ETI		QSPI_IO3				USART0_TX	UART1_RX							EVENTOUT
PB11	CK_OUT1	TIMER1_CH2	TIMER0_CH1_ON						UART1_RTS			TIMER15_BRKIN				EVENTOUT
PB12		TIMER0_BRKIN	TIMER0_CH3	TIMER1_CH2			I2C1_SCL									EVENTOUT
PB13		TIMER0_CH0_ON		TIMER1_CH3			I2C1_SDA		TIMER15_CH0							EVENTOUT
PB15	RTC_REFIN	TIMER0_CH2_ON	TIMER2_CH0		I2C0_SCL		I2C1_SCL	UART1_TX	USART0_TX	IFRP_OUT						EVENTOUT

Table 2-7. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC8			TIMER2_CH2		I2C0_SDA		I2C1_SDA	USART0_TX	UART1_TX							EVENTOUT
PC13	USART0_CK															EVENTOUT
PC14																EVENTOUT
PC15	IFRP_OUT															EVENTOUT

3. Functional description

3.1. RISC-V core

The devices of GD32VW553xx series devices are 32-bit general-purpose microcontrollers based on the Nuclei N307 processor. The N307 processor is based on the RISC-V architecture instruction set. The RISC-V processor includes two AHB buses known as I-Cache bus and System bus. All memory accesses of the RISC-V processor are executed on the two buses according to the different purposes and the target memory spaces. The memory organization uses a Harvard architecture, pre-defined memory map and up to 4 GB of memory space, making the system flexible and extendable. It supports 64 general purpose registers (GPRs):

- 3-pipeline stages, using state-of-the-art processor micro-architecture to deliver the best-of-class performance efficiency and lowest cost.
- Machine (M) and User (U) Privilege levels support.
- Non-maskable interrupt (NMI) support.
- Support dynamic branch predictor.
- Configurable instruction prefetch logic, which can prefetch subsequent two instructions to hide the instruction memory access latency.
- Support WFI (Wait for Interrupt) and WFE (Wait for Event) scheme to enter sleep mode.
- Interrupt priority levels configurable and programmable.
- Enhancement of vectored interrupt handling for real-time performance.
- Support interrupt preemption with priority.
- Support interrupt tail chaining.
- Standard 4-wire JTAG debug port and 2-wire cJTAG debug port.
- Support interactive debug functionalities.
- Support 8 triggers for hardware breakpoint.
- RV32I / M / A / F / D / C / P / B instruction extensions support.
- Support two-level sleep modes: shallow sleep mode, and deep sleep mode.
- Support 64-bits widereal-time counter (can be used as System Tick).
- Support Physical Memory Protection (PMP) to protect the memory, 8 entries.
- Support Instruction Cache (I-Cache), 2-way associative, cache line size 32 bytes, total 32KB.
- Support single / double precision FPU.
- Support 2 cycle floating point MAC.
- Support packed-SIMD DSP.

3.2. On-chip memory

- Up to 4096 Kbytes of Flash memory.

- Up to 288 Kbytes + 32 Kbyte (shared SRAM) SRAM memory.

4096 Kbytes Flash memory, and 320 Kbytes (288 Kbytes + 32 Kbyte Shared) SRAM at most is available for storing programs and data. ***Table 2-2. GD32VW553xx memory map*** shows the memory map of the GD32VW553xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 8 to 52 MHz crystal oscillator.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.8 to 3.6 V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 160 MHz/160 MHz/80MHz. See ***Figure 2-4. GD32VW553xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.55 V and down to 1.51V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.8 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} is 0 V.
- V_{DDA} range: 1.8 to 3.6 V, external analog power supply for ADC, reset blocks, RCs and PLL.

3.4. Boot modes

At startup, BOOT0 value and BOOT1 value are used to select the boot address. BOOT0 value and BOOT1 value are determined by configurations shown in ***Table 3-1. BOOT0 modes*** and ***Table 3-2. BOOT1 modes*** respectively.

- The BOOT0 value may come from the BOOT0 pin or from the value of SWBOOT0 bit in the EFUSE_CTL0 register to free the GPIO pad if needed.

- The BOOT1 value may come from the PB1 pin or from the value of SWBOOT1 bit in the EFUSE_CTL0 register to free the GPIO pad if needed.

Table 3-1. BOOT0 modes

SWBOOT0	EFBOOT0	BOOT0 PC8 pin	BOOT0
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Table 3-2. BOOT1 modes

SWBOOT1	EFBOOT1	BOOT1 PB1 pin	BOOT1
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Refer to ***Table 3-3. Boot address modes*** for boot address.

When BOOT0 value is 0:

- The boot address is selected according to EFSB bit value in EFUSE_CTL0 register.

When BOOT0 value is 1:

- When the EFBOOTLK bit in the EFUSE_CTL0 register is 0, the boot address is selected according to BOOT0 value and BOOT1 value.
- When the EFBOOTLK bit in the EFUSE_CTL0 register is 1, the boot address is selected according to BOOT0 value.

Table 3-3. Boot address modes

EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
-	0	-	0	0x08000000	SIP Flash
-	0	-	1	0x0BF46000	secure boot
0	1	0	-	0x0BF40000	Bootloader / ROM
0	1	1	-	0x0A000000	SRAM0
1	1	-	-	0x0BF40000	Bootloader / ROM

The BOOTx (x=0/1) value (either coming from the pin or the EFBOOTx bit) is latched upon reset release. It is up to the user to set BOOTx values to select the required boot mode. The BOOTx pin or EFBOOTx bit (depending on the EFBOOTLK and SWBOOTx bit value in the EFUSE_CTL0 register) is also re-sampled when exiting from Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode. After startup delay, the selection of the boot area is done before releasing the processor reset.

The embedded bootloader is located in the System memory, which is used to reprogram the Flash memory. The bootloader can be activated through one of the following serial interfaces: USART0 (PB15 and PA8), UART1 (PA4 and PA5), UART2 (PA6 and PA7).

3.5. Power saving modes

The MCU supports six kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, Standby, SRAM_sleep, WIFI_sleep and BLE_sleep mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode

  The sleep mode is corresponding to the SLEEPING mode of the RISC-V. In sleep mode, only clock of RISC-V is off. To enter the sleep mode, it is only necessary to clear the CSR_SLEEPVALUE bit in the RISC-V System Control Register, and execute a WFI or WFE instruction. If the sleep mode is entered by executing a WFI instruction, any interrupt can wake up the system. If it is entered by executing a WFE instruction, any wakeup event can wake up the system. The mode offers the lowest wakeup time as no time is wasted in interrupt entry or exit.

- **Deep-sleep** mode

  The deep-sleep mode is based on the SLEEPDEEP mode of the RISC-V. In deep-sleep mode, all clocks in the 1.1V domain are off, and all of IRC16M, HXTAL and PLLs are disabled. The contents of SRAM0/1/2/3 and registers are preserved. The LDO can operate normally or in low power mode depending on the LDOLP bit in the PMU_CTL0 register. Before entering the Deep-sleep mode, it is necessary to set the CSR_SLEEPVALUE bit in the RISC-V System Control Register, and clear the STBMOD bit in the PMU_CTL0 register. Then, the device enters the deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system. When exiting the Deep-sleep mode, the IRC16M is selected as the system clock. Notice that an additional wakeup delay will be incurred if the LDO operates in low power mode.

  The low-driver mode in deep-sleep mode can be entered by configuring the LDEN[1:0], LDNP, LDLP, LDOLP bits in the PMU_CTL0 register. The low-driver mode provides lower drive capability, and the low-power mode take lower power.

  Normal-driver & Normal-power: The Deep-sleep mode is not in low-driver mode by configure LDEN[1:0] to 00 in the PMU_CTL0 register, and not in low-power mode depending on the LDOLP bit reset in the PMU_CTL0 register.

  Normal-driver & Low-power: The Deep-sleep mode is not in low-driver mode by configure LDEN[1:0] to 00 in the PMU_CTL0 register. The low-power mode enters depending on the LDOLP bit set in the PMU_CTL0 register.

  Low-driver & Normal-power: The low-driver mode in Deep-sleep mode when the LDO in normal-power mode depending on the LDOLP bit reset in the PMU_CTL0 register enters by configure LDEN[1:0] to 0b11 and LDNP to 1 in the PMU_CTL0 register.

Low-driver & Low-power: The low-driver mode in Deep-sleep mode when the LDO in low-power mode depending on the LDOLP bit set in the PMU_CTL0 register enters by configure LDEN[1:0] to 0b11 and LDLP to 1 in the PMU_CTL0 register.

No Low-driver: The Deep-sleep mode is not in low-driver mode by configure LDEN[1:0] to 00 in the PMU_CTL0 register.

Note: In order to enter deep-sleep mode smoothly, all EXTI line pending status (in the EXTI_PD register) and RTC alarm / timestamp / tamper / auto wakeup flag must be reset. If not, the program will skip the entry process of deep-sleep mode to continue to execute the following procedure.

- **Standby** mode

  The standby mode is based on the SLEEPDEEP mode of the RISC-V, too. In standby mode, the whole 1.1V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLLs are disabled. Before entering the standby mode, it is necessary to set the CSR_SLEEPVALUE bit in the RISC-V System Control Register, and set the STBMOD bit in the PMU_CTL0 register, and clear WUF bit in the PMU_CS0 register. Then, the device enters the standby mode after a WFI or WFE instruction is executed, and the STBF status flag in the PMU_CS0 register indicates that the MCU has been in standby mode. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm / time stamp / tamper / auto wakeup events, the FWDGT reset, and the rising edge on WKUP pins. The standby mode achieves the lowest power consumption, but spends longest time to wake up. Besides, the contents of SRAM0 / SRAM1 / SRAM2 / SRAM3 and registers in 1.1V power domain are lost in standby mode. When exiting from the standby mode, a power-on reset occurs and the RISC-V will execute instruction code from the 0x00000000 address.

- **SRAM_sleep** mode

  When at least one of SRAM0 / SRAM1 / SRAM2 / SRAM3 is powered off, set the SRAMxPSLEEP (x = 0/1/2/3) bit in PMU_CTL1 register, then corresponding SRAMx (x = 0/1/2/3) will enter power off state (wait for several PCLK clocks, SRAM can completely power off and enter the SRAM sleep mode).

  When the SRAMxPWAKE (x = 0/1/2/3) bit in PMU_CTL1 register is set, the SRAMx (x = 0/1/2/3) will be powered on.

  SRAM0 / SRAM1 / SRAM2 / SRAM3 can be configured power on or power off when in run / sleep / deep_sleep mode.

  SRAM0 / SRAM1 / SRAM2 / SRAM3 are power off when in standby mode.

- **WIFI_sleep** mode

  The Wi-Fi_sleep mode can enter by software (set WPEN bit to 1 and set WPSLEEP bit to 1), or by hardware (driven by Wi-Fi hardware signal sleep_wl when WPEN is 1). This mode can exit by clearing WPEN bit to 0, or by setting WPEN bit to 1 then setting WPSLEEP bit to 1, or by hardware (driven by Wi-Fi hardware signal wake_wl when WPEN is 1).

  When Wi-Fi enter Wi-Fi_sleep mode, Wi-Fi_OFF domain power off.

- **BLE_sleep mode**

When BLE enter BLE_sleep mode, BLE_OFF domain power off.

When exit from BLE_sleep mode, BLE is active mode, all BLE power domain power on.

3.6. Electronic fuse (EFUSE)

- One-time programmable nonvolatile EFUSE storage cells organized as 128*8 bit.
- All bits in the efuse cannot be rollback from 1 to 0.
- Can only be accessed through corresponding registers.

The Efuse controller has Efuse macro that store system paramters. As a non-volatile unit of storage, the bit of Efuse macro cannot be restored to 0 once it is programmed to 1. According to the software opration, the Efuse controller can program all bits in the system parameters.

3.7. General-purpose inputs / outputs (GPIOs)

- Up to 29 fast GPIOs, all mappable on 16 external interrupt lines.
- Analog input/output configurable.
- Alternate function input/output configurable.

There are up to 29 general purpose I/O pins (GPIO) in GD32VW553xx, named PA0 ~ PA15, PB0 ~ PB4, PB11 ~ PB13, PB15, PC8 and PC13 ~ PC15 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.8. CRC calculation unit (CRC)

- 32-bit data input and 32-bit data output. Calculation period is 4 AHB clock cycles for 32-bit input data size from data entered to the calculation result available.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- Fixed polynomial: 0x4C11DB7
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 32 bit CRC code with fixed polynomial.

3.9. True Random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers.
- Disable TRNG module will significantly reduce the chip power consumption.
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.10. Direct memory access controller (DMA)

- 8 channels for DMA controller, up to 8 peripherals per channel with fixed hardware peripheral requests.
- Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer.
- Peripherals supported: Timers, ADC, SPI, QSPI, I2Cs, USARTs, CAU and HAU.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the MCU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data.

Two AHB master interfaces and eight four-word depth 32-bit width FIFOs are presented in DMA controller, which achieves a high DMA transmission performance. There are 8 independent channels in the DMA controller. Each channel is assigned a specific or multiple target peripheral devices for memory access request management. Two arbiters respectively for memory and peripheral are implemented inside to handle the priority among DMA requests.

Both the DMA controller and the RISC-V core implement data access through the system bus. An arbitration mechanism is implemented to solve the competition between these two masters. When the same peripheral is targeted, the MCU access will be suspended for some specific bus cycles. A round-robin scheduling algorithm is utilized in the bus matrix to guaranty at least half the bandwidth to the MCU.

3.11. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 3 MSPS.
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-

bit.

- Input voltage range: 0 ≤ V_{IN} ≤ V_{DDA}.
- Temperature sensor.

A 12-bit 3 MSPS multi-channel ADC is integrated in the device. It has a total of 11 multiplexed channels: up to 9 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between 0 and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the TIMERx (x= 0,1,2,5,15,16) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN9 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}, and V_{SSA} should be connected to V_{SS} through the specific circuit independently.

3.12. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer / counter with twenty 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function.

The RTC provides a time which includes hour / minute / second / sub-second and a calendar includes year / month / day / week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time. Working in power saving mode and smart wakeup is software configurable. Support improving the calendar accuracy using extern accurate low frequency clock.

3.13. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), two 32-bit general timer (TIMER1, TIMER2), two 16-bit general timers (TIMER15, TIMER16), and one 16-bit basic timer (TIMER5).

- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Encoder interface controller with two inputs using quadrature decoder.
- 64-bit SysTick timer up counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 and TIMER2 are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER15 and TIMER16 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. Only TIMER1 and TIMER2 supports an encoder interface with two inputs using quadrature decoder.

The basic timer TIMER5, is mainly used as a simple 16-bit time base.

The GD32VW553xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 64-bit up counter.
- Maskable system interrupt generation when the counter and comparison values are equal.
- Programmable clock source.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Maximum speed up to 20 MBits/s.
- Supports both asynchronous and clock synchronous serial communication modes.
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.
- Dual clock domain.
- Wake up from Deep-sleep mode.

The USART (USART0, UART1, UART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from Deep-sleep mode on I2C0 address match.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.16. Serial peripheral interface (SPI)

- SPI interfaces with a frequency of up to 40 MHz.
- Support both master and slave mode.
- Hardware CRC calculation and transmit automatic CRC error checking.
- SPI quad mode configuration available in master mode.

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). SPI can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.17. Quad-SPI interface (QSPI)

- Support normal mode, read polling mode and memory map mode.
- Fully programmable command format for both normal mode and memory map mode.
- Integrated FIFO for transmission/reception.
- 8, 16, or 32-bit data accesses.
- DMA channel for normal mode.

The QSPI is a specialized interface that communicate with Flash memories. This interface support single, dual or quad SPI FLASH.

3.18. Cryptographic acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode.
- AES supports 128bits-key, 192bits-key or 256 bits-key.
- AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), cipher message authentication code mode (CMAC), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported.

The Cryptographic Acceleration Unit supports acceleration of DES, TDES or AES (128, 192, or 256) algorithms. The DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode. The AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).

3.19. Hash acceleration unit (HAU)

- Supports SHA-1, SHA-224 and SHA-256 algorithms, compliant with FIPS PUB 180-2 (Federal Information Processing Standards Publication 180-2).
- Supports MD5 compliant with IETF RFC 1321 (Internet Engineering Task Force Request For Comments number 1321).

- Supports HMAC (keyed-hash message authentication code) algorithm.
- Automatic swapping to comply with the big-endian or little-endian for MD5, SHA-1, SHA-224 and SHA-256 algorithms.
- Automatic padding to fit module 512.
- Support DMA mode for input data flow.

The HAU supports acceleration of SHA-1, SHA-224, SHA-256, MD5 algorithm and the HMAC (keyed-hash message authentication code) algorithm, which calling the SHA-1, SHA-224, SHA-256 or MD5 hash function to calculate key, message, digest three times.

3.20. Public Key Cryptographic Acceleration Unit (PKCAU)

- Support RSA/DH algorithms with up to 3136 bits of operands.
- Support ECC algorithm with up to 640 bits of operands.
- Embedded RAM of 3584 bytes.
- Conversion between the Montgomery domain and the natural domain.
- only 32-bit access is supported.

Public key encryption is also called asymmetric encryption, asymmetric encryption algorithms use different keys for encryption and decryption. The Public Key Cryptographic Acceleration Unit (PKCAU) can accelerate RSA (Rivest, Shamir and Adleman), Diffie-Hellmann (DH key exchange) and ECC (elliptic curve cryptography) in GF(p) (Galois domain). These operations are performed in the Montgomery domain to improve computational efficiency.

3.21. Infrared ray port (IFRP)

- The IFRP output signal is decided by TIMER15_CH0 and TIMER16_CH0.
- To get correct infrared ray signal, TIMER15 should generate low frequency modulation envelope signal, and TIMER16 should generate high frequency carrier signal.

Infrared ray port (IFRP) is used to control infrared light LED, and send out infrared data to implement infrared ray remote control.

There is no register in this module, which is controlled by TIMER15 and TIMER16. The IFRP_OUT pin can be configured by GPIO alternate function selected register.

3.22. Wireless

3.22.1. Wi-Fi

Standards Supported

- 802.11b / g / n /ax compatible.
- 802.11e QoS Enhancement (WMM).
- 802.11i (WPA, WPA2, WPA3). Open, shared key, and pair-wise key authentication services.
- WiFi WPS.
- WiFi Direct.
- Integrated TCP / IP protocol.

Wi-Fi MAC

- Target Wake up Time (TWT) operation.
- Two NAV.
- Multiple BSSID operation.
- OFDMA-based random access.
- Spatial reuse.
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput.
- Support for immediate ACK and Block-ACK policies.
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP), and multiphase PSMP operation.
- Interframe space timing support, including RIFS.
- Support for RTS / CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware engine for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, and support for key management.
- Programmable independent basic service set (IBSS) or infrastructure basic service set or Access Point functionality.

Wi-Fi PHY

- Single antenna 1x1 stream in 20MHz channels.
- 20M bandwidth.
- MU-OFDMA in UL and DL as a non-AP STA.
- DL MU-MIMO as a non-AP STA.
- Beamforming as a beamformee.

- Rx STBC scheme (1 spatial stream and 2 space-time streams).
- Mid-amble.
- DCM.
- All guard interval (0.8 / 1.6 / 3.2us).
- Support of 802.11ax MCS up to MCS9 with Max phy rate as 114.7Mbps.
- Per packet TX power control.
- Advanced channel estimation / equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection.
- Digital calibration algorithms to handle CMOS RF chip process, voltage, and temperature (PVT) variations.
- Per-packet channel quality and signal-strength measurements.
- Compliance with FCC and other worldwide regulatory requirements.

3.22.2. BLE (Bluetooth Low Energy)

Standards Supported

- BLE5.2.

BLE Linker Layer

- Support multiple simulateneous hardware connection.
- Advertising Extension.
- High duty cycle non-connectable advertising.
- Channel selection algorithm #2.
- Support multiple simultaneous BLE connections.

BLE Modem

- High speed 2M PHY.
- Long range coded PHY.
- Data rate: 250, 500, 1000 and 2000kbps.

3.22.3. Radio

Radio is shared between Wi-Fi and BLE.

- Fractional-N for multiple reference clock support.
- Integrated PA with power control.
- Optimized Tx gain distribution for linearity and noise performance.
- Direct conversion architecture.
- On-chip gain selectable LNA with optimized noise figure.
- High dynamic range AGC.

3.23. Debug mode

- RISC-V External Debug Support Version 0.13.

The GD32VW553xx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the RISC-V module together with a daisy chained standard TAP controller. Debug functions are integrated into the RISC-V. The debug system supports standard JTAG debug.

3.24. Package and operation temperature

- QFN40 (GD32VW553Hx) and QFN32 (GD32VW553Kx).
- Operation temperature range: -40°C to +105°C (GD32VW553HxQ7), -40°C to +85°C (GD32VW553HxQ6).

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings (1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	- 0.3	3.6	V
V_{DDA}	External analog supply voltage	- 0.3	3.6	V
AVDD33_ANA	RF Analog voltage	- 0.3	3.6	V
AVDD33_PA	RF PA voltage	- 0.3	3.6	V
AVDD33_CLK	RF Clock voltage	- 0.3	3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	- 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	- 0.3	3.6	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	—	50	mV
I_{IO}	Maximum current for GPIO pin	—	±25	mA
T_A	Operating temperature range	-40	+105	°C
P_D(5)	Power dissipation at T_A = 105°C of QFN40	—	418	mW
	Power dissipation at T_A = 105°C of QFN32	—	389	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V_{IN} maximum value cannot exceed 5.5 V.
(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.
(5) When RF power off.

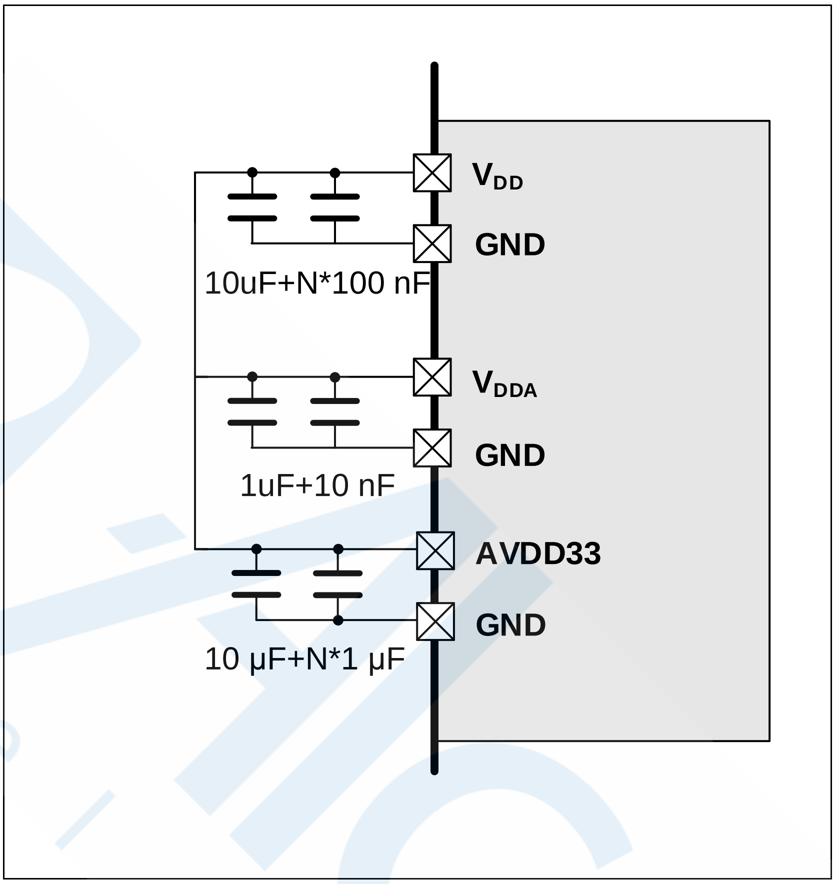
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.8	3.3	3.6	V
V_{DDA}	Analog supply voltage	—	1.8	3.3	3.6	V
AVDD33_ANA	RF Analog voltage	—	2.5(2)	3.3	3.6	V
AVDD33_PA	RF PA voltage	—	2.5(2)	3.3	3.6	V
AVDD33_CLK	RF Clock voltage	—	2.5(2)	3.3	3.6	V

(1) Based on characterization, not tested in production.
(2) RF performance may degrade below 3V.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)(3)



(1) When using precision internal reference voltage, and a bypass capacitor about 0.1 μF (or 1 μF connected in parallel, which is recommended) to ground is required.
(2) AVDD33 include AVDD33_PA, AVDD33_ANA, AVDD33_CLK.
(3) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	160	MHz
f_{APB1}	APB1 clock frequency	—	—	160	MHz
f_{APB2}	APB2 clock frequency	—	—	80	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	—	∞	μs /V
	V_{DD} fall time rate		TBD	—	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	181	ms
		Clock source from IRC16M	1.03	

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O

instruction.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	15.2	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	67	
	Wakeup from Deep-sleep mode (LDO in low power mode)	66.8	
	Wakeup from Deep-sleep mode (LDO On and Low driver mode)	66.6	
	Wakeup from Deep-sleep mode (LDO in low power and Low driver mode)	66.6	
$t_{Standby}$	Wakeup from Standby mode	1030	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16 MHz.

4.3. Power consumption

GD32VW553xx is designed with advanced power management technologies and suitable for Internet of Things applications.

Table 4-7. Wi-Fi Power consumption characteristics

Power Mode	MCU State	Wi-Fi State
Active	Active	Active
Wi-Fi Sleep	Active	Power save mode: Wi-Fi wake up periodically to listen beacon frame to stay connected to the AP.
Mild Sleep	Power on, PLL off, Clock gated	Power save mode: Wi-Fi wake up periodically to listen beacon frame to stay connected to the AP.
Hibernation	Mostly power off, only the wake up source is power on	Power off
Shutdown	—	Power off

Table 4-8. Wi-Fi Power consumption characteristics (1)(2)(3)

Power Mode	Description	Consumption	unit
Active	Wi-Fi Tx 802.11b, CCK 1Mbps, Pout = +18dBm(4)	331	mA
	Wi-Fi Tx 802.11b, CCK 11Mbps, Pout = +17dBm(4)	315	mA
	Wi-Fi Tx 802.11g, OFDM 6Mbps, Pout = +18dBm(4)	317	mA
	Wi-Fi Tx 802.11g, OFDM 54Mbps, Pout = +15dBm(4)	283	mA
	Wi-Fi Tx 802.11n, HT 20M MCS0, Pout = +18dBm(4)	316	mA
	Wi-Fi Tx 802.11n, HT 20M MCS7, Pout = +14dBm(4)	275	mA

Power Mode	Description	Consumption	unit
	Wi-Fi Tx 802.11ax, HE 20M MCS0, Pout = +18dBm(4)	316	mA
	Wi-Fi Tx 802.11ax, HE 20M MCS9, Pout = +12dBm(4)	265	mA
	Wi-Fi Rx 802.11b, CCK 1Mbps, -90dBm(5)	99	mA
	Wi-Fi Rx 802.11b, CCK 11Mbps, -80Bm(5)	100	mA
	Wi-Fi Rx 802.11g, OFDM 6Mbps, -80dBm(5)	101	mA
	Wi-Fi Rx 802.11g, OFDM 54Mbps, -70dBm(5)	102	mA
	Wi-Fi Rx 802.11n, HT 20M MCS0, -75dBm(5)	100	mA
	Wi-Fi Rx 802.11n, HT 20M MCS7, -65dBm(5)	103	mA
	Wi-Fi Rx 802.11ax, HE 20M MCS0, -75dBm(5)	101	mA
	Wi-Fi Rx 802.11ax, HE 20M MCS9, -60dBm(5)	107	mA
Wi-Fi Sleep	MCU in Run mode(6)	37.6	mA
Mild Sleep(7)	DTIM=1	1.4	mA
	DTIM=3	0.55	mA
	DTIM=10	0.31	mA
Hibernation	MCU in Standby mode(8)	TBD	μA
Shutdown	—	—	mA

(1) Below data are measured at antenna port of GD Wi-Fi Demo board.
(2) Unless otherwise specified, all values given for TA condition and test result is mean value.
(3) DC Power = 3.3 V, HXTAL = 40 MHz, System clock = 160 MHz.
(4) Continuous Tx, Duty cycle = 100%.
(5) Rx Packet Length = 1024 Bytes.
(6) V_{DD} = V_{DDA} = 3.3 V, HXTAL = 40 MHz, System clock = 160 MHz, all peripherals enabled, except Wi-Fi.
(7) The DTIM power consumption is equal to the average power consumption of multiple beacon intervals.
(8) V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on.

Table 4-9. Power consumption characteristics (2)(3)(4)(5)(6)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$I_{DD}+I_{DDA}$		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals enabled	—	35.52	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals disabled	—	18.72	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	—	28.26	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	15.49	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	25.74	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	14.24	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled	—	23.93	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled	—	13.55	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled	—	19.22	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled	—	12.74	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled	—	15.21	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled	—	10.61	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled	—	12.43	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals disabled	—	7.55	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, PLL off, All peripherals enabled	—	7.72	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, PLL off, All peripherals disabled	—	5.03	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 16 MHz, PLL off, All peripherals enabled	—	5.18	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 16 MHz, PLL off, All peripherals disabled	—	3.37	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 8 MHz, PLL off, All peripherals enabled	—	3.41	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System	—	2.51	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		clock = 8 MHz, PLL off, All peripherals disabled				
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 4 MHz, PLL off, All peripherals enabled	—	2.53	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 4 MHz, PLL off, All peripherals disabled	—	2.08	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 2 MHz, PLL off, All peripherals enabled	—	2.09	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 2 MHz, PLL off, All peripherals disabled	—	1.86	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals enabled	—	30.88	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals disabled	—	14.09	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled	—	24.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled	—	12.01	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled	—	22.62	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled	—	11.11	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled	—	21.14	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled	—	10.77	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled	—	17.14	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All	—	9.25	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		peripherals disabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled	—	13.82	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled	—	8.28	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled	—	11.40	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled	—	7.27	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 25 MHz, PLL off, CPU clock off, All peripherals enabled	—	7.02	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 25 MHz, PLL off, CPU clock off, All peripherals disabled	—	4.33	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 16 MHz, PLL off, CPU clock off, All peripherals enabled	—	4.39	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 16 MHz, PLL off, CPU clock off, All peripherals disabled	—	2.60	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 8 MHz, PLL off, CPU clock off, All peripherals enabled	—	3.02	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 8 MHz, PLL off, CPU clock off, All peripherals disabled	—	2.12	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 4 MHz, PLL off, CPU clock off, All peripherals enabled	—	2.32	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 4 MHz, PLL off, CPU clock off, All peripherals disabled	—	1.88	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 2 MHz, PLL off, CPU clock off, All peripherals enabled	—	1.98	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 2 MHz, PLL off, CPU clock off, All peripherals disabled	—	1.75	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode	—	188.93	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode	—	170.50	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	—	150.00	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode	—	130.77	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode, Wi-Fi、SRAM1、SRAM2、SRAM3 sleep	—	99.07	—	μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on	—	3.30	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC off	—	3.05	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off	—	2.73	—	μA

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all values given for T_A condition and test result is mean value.
(3) When System Clock is greater than 16 MHz, a crystal 25 MHz is used, and the HXTAL bypass function is closed, using PLL.
(4) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.
(5) With large margin, it will be adjusted according to the mass production data.
(6) When Wi-Fi power off.

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-10. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-10. EMS characteristics (1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = V_{DDA} = AVDD33 = 3.3 V, T_A = 25 °C, Wi-Fi on, QFN40, f_{HCLK} = 160 MHz	TBD

Symbol	Parameter	Conditions	Level/Class
		conforms to IEC 61000-4-2	
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and GND	$V_{DD} = V_{DDA}$ = AVDD33 = 3.3 V, T_A = 25 °C, Wi-Fi on, QFN40, f_{HCLK} = 160 MHz conforms to IEC 61000-4-4	TBD

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.19	—	V
		LVDT[2:0] = 000, falling edge	—	2.08	—	V
		LVDT[2:0] = 001, rising edge	—	2.33	—	V
		LVDT[2:0] = 001, falling edge	—	2.22	—	V
		LVDT[2:0] = 010, rising edge	—	2.47	—	V
		LVDT[2:0] = 010, falling edge	—	2.36	—	V
		LVDT[2:0] = 011, rising edge	—	2.61	—	V
		LVDT[2:0] = 011, falling edge	—	2.50	—	V
		LVDT[2:0] = 100, rising edge	—	2.75	—	V
		LVDT[2:0] = 100, falling edge	—	2.64	—	V
		LVDT[2:0] = 101, rising edge	—	2.90	—	V
		LVDT[2:0] = 101, falling edge	—	2.79	—	V
		LVDT[2:0] = 110, rising edge	—	3.04	—	V
		LVDT[2:0] = 110, falling edge	—	2.92	—	V
		LVDT[2:0] = 111, rising edge	—	3.17	—	V
		LVDT[2:0] = 111, falling edge	—	3.06	—	V
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.55	—	V
V_{PDR}(1)	Power down reset threshold		—	1.51	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	40	—	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	Reset temporization		—	2.6	—	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-12. ESD characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; ESDA/JEDEC JS-001-2017	—	—	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; ESDA/JEDEC JS-002-2018	—	—	TBD	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

Table 4-13. Static latch-up characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78E	—	—	TBD	mA
	V_{supply} over voltage		—	—	TBD	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

4.7. External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal / ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Frequency Range	—	19.2	40	52	MHz
C_{HXTAL}	Crystal load Capacitance	—	9	10	12	pF
ESR	Equivalent Series Resistance	—	—	—	70	Ω
f_tol	Frequency tolerance	Initial and over temperature	-20	—	20	ppm
$t_{SUHXTAL}$[1]	Crystal startup time	V_{DD} = 3.3 V, T_A = 25 °C, f_{HXTAL} = 40 MHz	—	0.75	—	ms

(1) Based on characterization, not tested in production.

Table 4-15. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	Frequency Range	—	—	40	—	MHz
V_{HXTAL}	OSCIN Input Voltage	—	0.7	—	2.5	V
$Ducy_{(HXTAL)}$	Duty cycle	—	45	50	55	%
PN	Phase Noise	@1kHz, f_{HXTAL} = 40 MHz	—	—	-125	dBc/Hz
		@10kHz f_{HXTAL} = 40 MHz	—	—	-138	dBc/Hz
		@100kHz f_{HXTAL} = 40 MHz	—	—	-143	dBc/Hz
f_tol	Frequency tolerance	Initial and over temperature	-20	—	20	ppm

Table 4-16. Low speed external clock (LXTAL) generated from a crystal / ceramic characteristics

	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
g_m(2)	Oscillator transconductance	Lower driving capability	—	4.5	—	µA/V
		Medium low driving capability	—	6.5	—	
		Medium high driving capability	—	13	—	
		Higher driving capability	—	19	—	
$I_{DDLXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = V_{DDA} = 3.3 V, Lower driving capability	—	0.8	—	µA
		V_{DD} = V_{DDA} = 3.3 V, Medium low driving capability	—	0.94	—	
		V_{DD} = V_{DDA} = 3.3 V, Medium high driving capability	—	1.34	—	
		V_{DD} = V_{DDA} = 3.3 V, Higher driving capability	—	1.74	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	2	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass

mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}[1]	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}[2]	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7*V_{DD}	—	—	V
V_{LXTALL}[2]	OSC32IN input pin low level voltage		—	—	0.3*V_{DD}	
$t_{H/L(LXTAL)}$[2]	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$[2]	OSC32IN rise or fall time	—	—	—	50	
C_{IN}[2]	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$[2]	Duty cycle	—	30	—	70	%

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-18. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16 M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	16	—	MHz
ACC_{IRC16M}	IRC16 M oscillator Frequency accuracy, Factory-trimmed	2.7 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V, T_A = -40 °C ~ +105 °C[1]	-2.0	—	+2.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C	-1.0	—	+1.0	%
	IRC16 M oscillator Frequency accuracy, User trimming step[1]	—	—	0.5	—	%
$Ducy_{IRC16M}$[2]	IRC16 M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC16M}$[1]	IRC16 M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	70	—	μA
$t_{SUIRC16M}$[1]	IRC16 M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.51	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-19. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}[1]	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	—	32	—	kHz
$I_{DDAIRC32K}$[2]	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	0.31	—	μA
$t_{SUIRC32K}$[2]	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	26.9	—	μs

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-20. PLLDIG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}[2]	PLL input clock frequency	—	19.2	40	52	MHz
f_{PLLOUT}[2]	PLL output clock frequency	—	—	—	480	MHz
f_{VCO}[2]	PLL VCO output clock frequency	—	—	960	—	MHz
t_{LOCK}[1]	PLL lock time	—	—	—	50	μs
I_{DDA}[1]	Current consumption	—	—	1.8	—	mA
$Jitter_{PLL}$[1]	Absolute RMS Jitter	XTAL freq = 40 MHz	—	8	—	ps

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.10. Memory characteristics

Table 4-21. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}[1]	Number of guaranteed program /erase cycles before failure(Endurance)	T_A = -40 °C ~ +105 °C	100	—	—	kcycles
t_{RET}[1]	Data retention time	—	—	20	—	years
t_{PROG}[2]	word programming time	T_A = -40 °C ~ +105 °C	—	1000	—	μs
t_{ERASE}[2]	Page[3] erase time	T_A = -40 °C ~ +105 °C	—	100	—	ms
t_{MERASE}[2]	Mass erase time	T_A = -40 °C ~ +105 °C	—	12	—	s

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) 4KB.

4.11. NRST pin characteristics

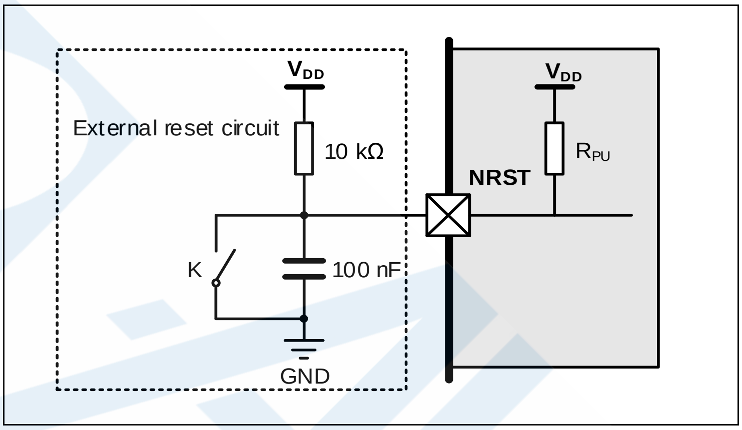
Table 4-22. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.8 V	0.3VDD	—	TBD	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		TBD	—	0.7VDD	
V_{hyst}[1]	Schmidt trigger Voltage hysteresis		—	370	—	mV
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	0.3VDD	—	TBD	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		TBD	—	0.7VDD	
V_{hyst}[1]	Schmidt trigger Voltage hysteresis		—	420	—	mV
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	0.3VDD	—	TBD	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		TBD	—	0.7VDD	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	440	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Figure 4-2. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-23. I/O port DC characteristics (1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO Low level input voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO Low level input voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL} (IO_speed = MAX)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	0.14	—	V
		V_{DD} = 2.7V	—	0.11	—	
		V_{DD} = 3.3V	—	0.10	—	V
		V_{DD} = 3.6V	—	0.10	—	
V_{OL} (IO_speed = MAX)	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.8V	—	0.41	—	V
		V_{DD} = 2.7V	—	0.27	—	
		V_{DD} = 3.3V	—	0.25	—	V
		V_{DD} = 3.6V	—	0.25	—	
V_{OH} (IO_speed = MAX)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	1.59	—	V
		V_{DD} = 2.7V	—	2.56	—	
		V_{DD} = 3.3V	—	3.17	—	V
		V_{DD} = 3.6V	—	3.47	—	
V_{OH}	High level output	V_{DD} = 1.8V	—	1.17	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(IO_speed = MAX)	voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7V	—	2.32	—	V
		V_{DD} = 3.3V	—	2.96	—	
		V_{DD} = 3.6V	—	3.28	—	
V_{OL} (IO_speed = 25 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	0.20	—	V
		V_{DD} = 2.7V	—	0.14	—	V
		V_{DD} = 3.3V	—	0.13	—	
		V_{DD} = 3.6V	—	0.13	—	
V_{OL} (IO_speed = 25 MHz)	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.8V	—	0.70	—	V
		V_{DD} = 2.7V	—	0.37	—	V
		V_{DD} = 3.3V	—	0.33	—	
		V_{DD} = 3.6V	—	0.32	—	
V_{OH} (IO_speed = 25 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	1.50	—	V
		V_{DD} = 2.7V	—	2.51	—	V
		V_{DD} = 3.3V	—	3.12	—	
		V_{DD} = 3.6V	—	3.43	—	
V_{OH} (IO_speed = 25 MHz)	High level output voltage for an IO Pin (I_{IO} = +17 mA)	V_{DD} = 1.8V	—	0.94	—	V
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.7V	—	2.16	—	V
		V_{DD} = 3.3V	—	2.83	—	
		V_{DD} = 3.6V	—	3.16	—	
V_{OL} (IO_speed = 10 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	0.40	—	V
		V_{DD} = 2.7V	—	0.25	—	V
		V_{DD} = 3.3V	—	0.23	—	
		V_{DD} = 3.6V	—	0.22	—	
V_{OL} (IO_speed = 10 MHz)	Low level output voltage for an IO Pin (I_{IO} = +12 mA)	V_{DD} = 1.8V	—	0.9	—	V
	Low level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 2.7V	—	0.54	—	V
		V_{DD} = 3.3V	—	0.47	—	
		V_{DD} = 3.6V	—	0.46	—	
V_{OH} (IO_speed = 10 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.8V	—	1.21	—	V
		V_{DD} = 2.7V	—	2.36	—	V
		V_{DD} = 3.3V	—	3.00	—	
		V_{DD} = 3.6V	—	3.32	—	
V_{OH} (IO_speed = 10 MHz)	High level output voltage for an IO Pin (I_{IO} = +10 mA)	V_{DD} = 1.8V	—	0.88	—	V
	High level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 2.7V	—	1.92	—	V
		V_{DD} = 3.3V	—	2.66	—	
		V_{DD} = 3.6V	—	3.00	—	
V_{OL}	Low level output	V_{DD} = 1.8V	—	0.22	—	V

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
(IO_speed = 2 MHz)	voltage for an IO Pin (I_{IO} = +1 mA)		V_{DD} = 2.7V	—	0.15	—	V
			V_{DD} = 3.3V	—	0.14	—	
			V_{DD} = 3.6V	—	0.13	—	
V_{OL} (IO_speed = 2 MHz)	Low level output voltage for an IO Pin (I_{IO} = +2 mA)		V_{DD} = 1.8V	—	0.56	—	V
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7V	—	0.70	—	V
			V_{DD} = 3.3V	—	0.59	—	
			V_{DD} = 3.6V	—	0.57	—	
V_{OH} (IO_speed = 2 MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)		V_{DD} = 1.8V	—	1.49	—	V
			V_{DD} = 2.7V	—	2.51	—	V
			V_{DD} = 3.3V	—	3.13	—	
			V_{DD} = 3.6V	—	3.44	—	
V_{OH} (IO_speed = 2 MHz)	High level output voltage for an IO Pin (I_{IO} = +2 mA)		V_{DD} = 1.8V	—	0.99	—	V
	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7V	—	1.73	—	V
			V_{DD} = 3.3V	—	2.55	—	
			V_{DD} = 3.6V	—	2.90	—	
R_{PU}(2)	Internal pull-up resistor	All pins	—	—	40	—	kΩ
		PU	—	—	10	—	
R_{PD}(2)	Internal pull-down resistor	All pins	—	—	40	—	kΩ
		PU	—	—	10	—	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

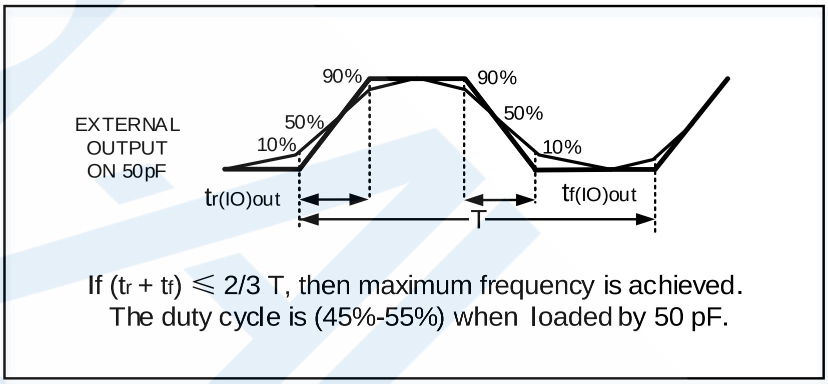
Table 4-24. I/O port AC characteristics (1)(2)

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_CTL->MDy[1:0]=10 (IO_Speed = 2 MHz)	Maximum frequency(4)	1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 10pF	3.47	MHz
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 30pF	3.15	
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 50pF	2.77	
GPIOx_CTL->MDy[1:0] = 01 (IO_Speed = 10 MHz)	Maximum frequency(4)	1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 10pF	24.33	MHz
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 30pF	20.41	
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 50pF	15.63	
GPIOx_CTL->MDy[1:0]=11 (IO_Speed = 25 MHz)	Maximum frequency(4)	1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 10pF	142.45	MHz
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 30pF	100.55	
		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 50pF	48.38	

GPIOx_MDy[1:0] bit value[3]	Parameter	Conditions	Max	Unit
GPIOx_CTL->MDy[1:0]=11(IO_Speed = MAX)	Maximum frequency[4]	1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 10pF	246.91	MHz
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 30pF	159.87	
		1.8 V ≤ V_{DD} ≤ 3.6 V , CL = 50pF	117.79	

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for T_A = 25 ℃.
(3) The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32VW553xx user manual which is selected to set the GPIO port output speed.
(4) The maximum frequency is defined in Figure 4-3, and maximum frequency cannot exceed 100 MHz.

Figure 4-3. I/O port AC characteristics definition



4.13. ADC characteristics

Table 4-25. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}[2]	Operating voltage	—	1.62	3.3	3.6	V
V_{IN}[2]	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}[2]	ADC clock[3]	2.4 V ≤ V_{DDA} ≤ 3.6 V	—	—	42	MHz
		1.62 V ≤ V_{DDA} ≤ 2.4 V	—	—	14	
f_S[2]	Sampling rate	12-bit	0.007	—	3	MSPS
V_{AIN}[2]	Analog input voltage	9 external; 2 internal	0	—	V_{DDA}	V
R_{AIN}[2]	External input impedance	See *Equation 1*	—	—	178.8	kΩ
R_{ADC}[2]	Input sampling switch resistance	—	—	—	0.2	kΩ
C_{ADC}[2]	Input sampling capacitance	No pin / pad capacitance included	—	—	6.57	pF
t_s[2]	Sampling time	f_{ADC}[3] = 42 MHz	0.036	—	11.42	μs
t_{CONV}[2]	Total conversion time(including sampling time)	12-bit	14	—	492	1 / f_{ADC}
t_{SU}[2]	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) When the supply voltage of V_{DDA} is 2.4V to 3.6V, the maximum frequency of f_{ADC} is 42 MHz, and when the supply voltage of V_{DDA} is 1.62V to 2.4V, the maximum frequency of f_{ADC} is 14 MHz.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-26. ADC R_{AIN} max for f_{ADC} = 42 MHz (1)

T_s(cycles)	t_s(μs)	R_{AINmax}(kΩ)
1.5	0.036	0.36
2.5	0.06	0.73
14.5	0.345	5.21
27.5	0.655	10.07
55.5	1.32	20.52
83.5	1.99	30.9
111.5	2.655	41.44
143.5	3.416	53.39
479.5	11.42	178.8

(1) Based on characterization, not tested in production.

Table 4-27. ADC dynamic accuracy at f_{ADC} = 42 MHz (1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 42 MHz, V_{DDA} = 3.3 V, Input Frequency = 20 kHz, Temperature = 25℃	—	11	—	bits
SNDR	Signal-to-noise and distortion ratio		—	68.21	—	dB
SNR	Signal-to-noise ratio		—	68.39	—	
THD	Total harmonic distortion		—	-81.5	—	

(1) Based on characterization, not tested in production.

Table 4-28. ADC static accuracy at f_{ADC} = 42 MHz

Symbol	Parameter	Test conditions	Typ(1)	Max	Unit
Offset	Offset error	f_{ADC} = 42 MHz, V_{DDA} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±0.9	—	
INL	Integral linearity error		±1.1	—	

(1) Based on characterization, not tested in production.

4.14. Temperature sensor characteristics

Table 4-29. Temperature sensor characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1	—	℃
Avg_Slope	Average slope	—	4.3	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.42	—	V
t_{START}	Startup time	—	8	—	μs
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	13.7	—	μs

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. I2C characteristics

Table 4-30. I2C characteristics (1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	3(4)(5)	300	3(4)(6)	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{s(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{s(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{buff}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

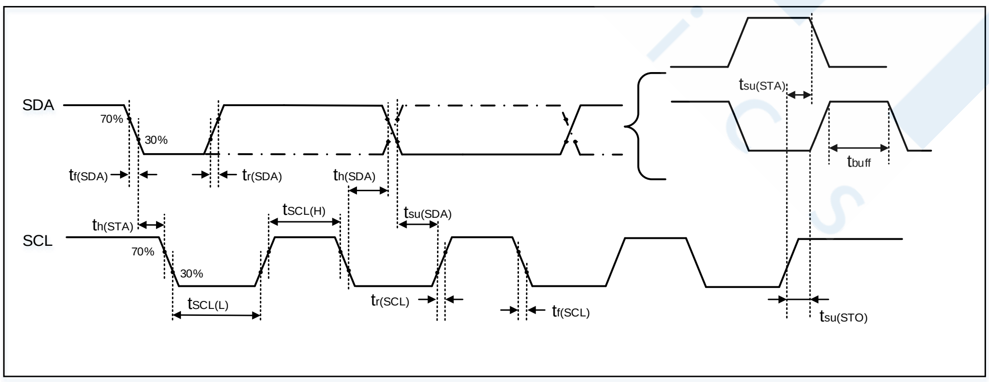
(3) The external device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

(4) Based on characterization, not tested in production.

(5) In the condition of I2C frequency = 400 kHz, IO_Speed = 50 MHz and Pull-up resistor = 1 kΩ.

(6) In the condition of I2C frequency = 1 MHz, IO_Speed = 50 MHz and Pull-up resistor = 1 kΩ.

Figure 4-4. I2C bus timing diagram



4.16. SPI characteristics

Table 4-31. Standard SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	40	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 160 MHz, presc = 4	10.5	12.5	14.5	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 160 MHz, presc = 4	10.5	12.5	14.5	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	TBD	ns
$t_{SU(MI)}$	Data input setup time	—	4.4	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	2.3	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	TBD	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	TBD	—	ns
$t_{V(SO)}$	Data output valid time	—	—	TBD	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1.6	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-5. SPI timing diagram - master mode

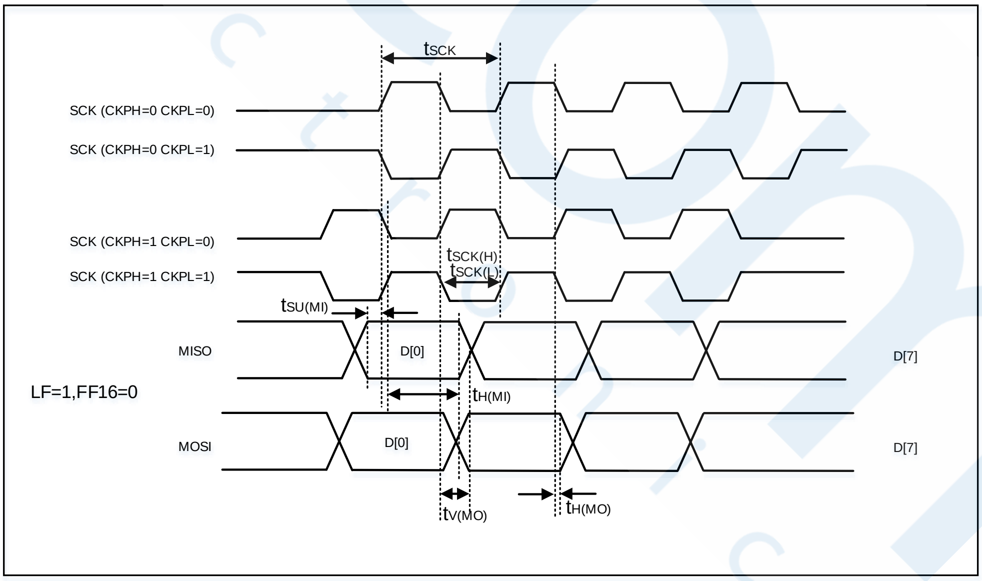
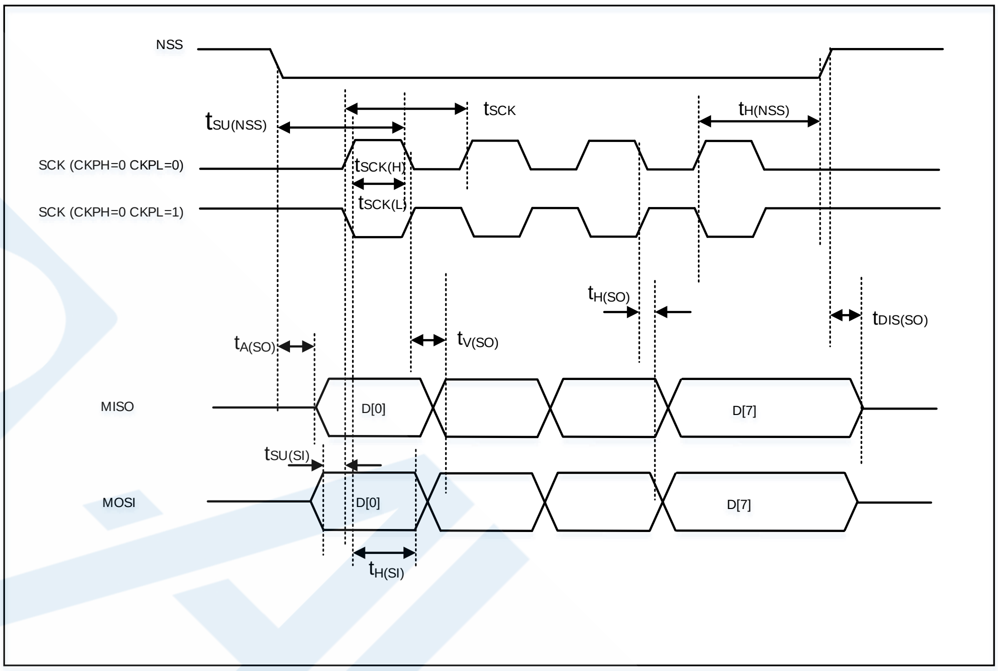


Figure 4-6. SPI timing diagram - slave mode



4.17. USART characteristics

Table 4-32. USART characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 80MHz	—	—	40	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 80 MHz	12.50	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} =80 MHz	12.50	—	—	ns

(1) Guaranteed by design, not tested in production.

4.18. TIMER characteristics

Table 4-33. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	t_{CK_TIMERx}
		f_{CK_TIMERx} = 160 MHz	6.25	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		f_{CK_TIMERx} = 160 MHz	0	80	MHz
RES	Timer resolution	TIMERx except (TIMER1& TIMER2)	—	16	bit
		TIMER1& TIMER2	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 160 MHz	0.00625	409.6	μs

Symbol	Parameter	Conditions	Min	Max	Unit
	32-bit counter clock period when internal clock is selected	—	1	65536 × 65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 160 MHz	—	26.84	s
t_{MAX_COUNT}	Maximum possible count (32-bit)	—	—	65536 × 65536× 65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 160 MHz	—	488.6	s

(1) Guaranteed by design, not tested in production.

4.19. WDGT characteristics

Table 4-34. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] =0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Guaranteed by design, not tested in production.

Table 4-35. WWDGT min-max timeout value at 40 MHz (fPCLK1) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	102.4	μs	6.55	ms
1/2	01	204.8		13.10	
1/4	10	409.6		26.21	
1/8	11	819.2		52.42	

(1) Guaranteed by design, not tested in production.

4.20. Wi-Fi Radio characteristics

Below data are measured at GD32VW553xx RF pin.

Table 4-36. Transmitter power characteristics (1)(2)

Parameter	Rate	Typ	Unit
Tx Power	11b,1Mbps	22.3	dBm
	11b,11Mbps	22.3	
	11g,6Mbps	20.9	
	11g,54Mbps	18.7	
	11n,HT20,MCS0	20.3	

Parameter	Rate	Typ	Unit
	11n,HT20,MCS7	18	
	11ax,HE20,MCS0	20.8	
	11ax,HE20,MCS9	15.6	

(1) Tx Power level is Limited by 802.11 Mask & EVM spec.

(2) Based on characterization, not tested in production.

Table 4-37. Receiver sensitivity characteristics (1)

Parameter	Rate	Typ	Unit
Rx Sensitivity	11b,1Mbps	-100.3	dBm
	11b,2Mbps	-96.9	
	11b,5.5Mbps	-94.8	
	11b,11Mbps	-91.8	
	11g,6Mbps	-95.2	
	11g,9Mbps	-94.5	
	11g,12Mbps	-93.4	
	11g,18Mbps	-90.5	
	11g,24Mbps	-87.8	
	11g,36Mbps	-84.8	
	11g,48Mbps	-80	
	11g,54Mbps	-78.7	
	11n,HT20,MCS0	-95.1	
	11n,HT20,MCS1	-92.6	
	11n,HT20,MCS2	-90.3	
	11n,HT20,MCS3	-87.2	
	11n,HT20,MCS4	-83.9	
	11n,HT20,MCS5	-79.5	
	11n,HT20,MCS6	-77.9	
	11n,HT20,MCS7	-76.2	
	11ax,HE20,MCS0	-94.9	
	11ax,HE20,MCS1	-92.1	
	11ax,HE20,MCS2	-89.7	
	11ax,HE20,MCS3	-86.3	
	11ax,HE20,MCS4	-83.2	
	11ax,HE20,MCS5	-78.7	
	11ax,HE20,MCS6	-77.5	
	11ax,HE20,MCS7	-76.2	
	11ax,HE20,MCS8	-71.5	
	11ax,HE20,MCS9	-69.7	
	11ax,HE20,MCS0-DCM	-95.1	
	11ax,HE20,MCS1-DCM	-94.6	
	11ax,HE20,MCS3-DCM	-89.9	
	11ax,HE20,MCS4-DCM	-86.8	

Parameter	Rate	Typ	Unit
	11ax,HE20,MCS0-ER	-95.6	
	11ax,HE20,MCS0-ER-106	-96.5	
	11ax,HE20,MCS0-ER-DCM	-96.5	
	11ax,HE20,MCS0-ER-DCM-106	-96.7	
	11ax,HE20,MCS1-ER	-92.6	
	11ax,HE20,MCS1-ER-DCM	-95.2	
	11ax,HE20,MCS2-ER	-90.1	

(1) Based on characterization, not tested in production.

Table 4-38. Rx Maximum Input Level (1)

Parameter	Rate	Typ	Unit
Rx Maximum Level Input	11b,1Mbps	>8.5	dBm
	11b,11Mbps	>8.5	
	11g,6Mbps	>8.5	
	11g,54Mbps	TBD	
	11n,HT20,MCS0	>8.5	
	11n,HT20,MCS7	TBD	
	11ax,HE20,MCS0	>8.5	
	11ax,HE20,MCS9	TBD	

(1) Based on characterization, not tested in production.

Table 4-39. Adjacent Channel Rejection (1)(4)

Parameter	Rate	Typ		Unit
		Interference pattern by IQxel(2)	In-house interference pattern(3)	
Adjacent Channel Rejection	11b, 11Mbps	45	TBD	dB
	11g, 6Mbps	30	TBD	
	11g, 54Mbps	11.5	TBD	
	11n, HT20,MCS0	27	TBD	
	11n,HT20,MCS7	10	TBD	
	11ax,HE20,MCS0	25	TBD	
	11ax,HE20,MCS9	-0.5	TBD	

(1) ACR result depends on interference source.
(2) Waveform generated by LitePoint IQxel series instrument, gap = SIFS
(3) Waveform generated by GD32VW553xx baseband, gap = SIFS
(4) Based on characterization, not tested in production.

4.21. Bluetooth LE Radio characteristics

Table 4-40. Transmitter Characteristics - Bluetooth LE 1 Mbps

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	RF power control range	-30	5	15	dBm

	Gain control step	—	1	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0, 1, 2, ..k}$	—	0.89	—	kHz
	Max $\|f_0 - f_n\|$	—	1.53	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	0.74	—	kHz
	$\|f_1 - f_0\|$	—	0.85	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.61	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	216.5	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	0.88	—	—
In-band spurious emissions	±2 MHz offset	—	-47	—	dBm
	±3 MHz offset	—	-50	—	dBm
	>±3 MHz offset	—	-51	—	dBm

Table 4-41. Transmitter Characteristics - Bluetooth LE 2 Mbps

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	RF power control range	-30	5	15	dBm
	Gain control step	—	1	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0, 1, 2, ..k}$	—	1.06	—	kHz
	Max $\|f_0 - f_n\|$	—	1.58	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	0.78	—	kHz
	$\|f_1 - f_0\|$	—	0.72	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	499.8	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	436	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	0.89	—	—
In-band spurious emissions	±4 MHz offset	—	-48	—	dBm
	±5 MHz offset	—	-51	—	dBm
	>±5 MHz offset	—	-53	—	dBm

Table 4-42. Transmitter Characteristics - Bluetooth LE 125 Kbps

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	RF power control range	-30	5	15	dBm
	Gain control step	—	1	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0, 1, 2, ..k}$	—	0.47	—	kHz
	Max $\|f_0 - f_n\|$	—	1.55	—	kHz
	$\|f_n - f_{n-3}\|$	—	1.19	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	251.38	—	kHz
	Min $\Delta f1_{max}$ (for at least 99.9% of all $\Delta f1_{max}$)	—	248.18	—	kHz

Table 4-43. Receiver Characteristics - Bluetooth LE 1 Mbps

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8%	—	—	-100.5	—	dBm

Parameter	Conditions	Min	Typ	Max	Unit
PER					
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-2	—	dB
	F = F0 – 1 MHz	—	-4	—	dB
	F = F0 + 2 MHz	—	-31	—	dB
	F = F0 – 2 MHz	—	-36	—	dB
	F = F0 + 3 MHz	—	-37	—	dB
	F = F0 – 3 MHz	—	-44	—	dB
	F ⩾ F0 + 4 MHz	—	-37	—	dB
	F ⩽ F0 – 4 MHz	—	-56	—	dB
Image frequency	+ 4 MHz	—	-37	—	dB
Adjacent channel to image frequency	$F = F_{image} + 1$ MHz	—	-47	—	dB
	$F = F_{image} - 1$ MHz	—	-37	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	-5.5	—	dBm
	2003 MHz ~ 2399 MHz	—	-8.5	—	dBm
	2484 MHz ~ 2997 MHz	—	-7.5	—	dBm
	3000 MHz ~ 12.75 GHz	—	-5.5	—	dBm
Intermodulation	—	—	-27	—	dBm

Table 4-44. Receiver Characteristics - Bluetooth LE 2 Mbps

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	-97.5	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	-4	—	dB
	F = F0 – 2 MHz	—	-7	—	dB
	F = F0 + 4 MHz	—	-35	—	dB
	F = F0 – 4 MHz	—	-48	—	dB
	F = F0 + 6 MHz	—	-45	—	dB
	F = F0 – 6 MHz	—	-53	—	dB
	F ⩾ F0 + 8 MHz	—	-53	—	dB
	F ⩽ F0 – 8 MHz	—	-55	—	dB
Image frequency	+ 4 MHz	—	-35	—	dB
Adjacent channel to image frequency	$F = F_{image} + 2$ MHz	—	-45	—	dB
	$F = F_{image} - 2$ MHz	—	-4	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	-5.5	—	dBm
	2003 MHz ~ 2399 MHz	—	-18.5	—	dBm
	2484 MHz ~ 2997 MHz	—	-15.5	—	dBm

Parameter	Conditions	Min	Typ	Max	Unit
	3000 MHz ~ 12.75 GHz	—	-15.5	—	dBm
Intermodulation	—	—	-27	—	dBm

Table 4-45. Receiver Characteristics - Bluetooth LE 125 Kbps

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	-107.5	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	2	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-14	—	dB
	F = F0 – 1 MHz	—	-14	—	dB
	F = F0 + 2 MHz	—	-30	—	dB
	F = F0 – 2 MHz	—	-34	—	dB
	F = F0 + 3 MHz	—	-32	—	dB
	F = F0 – 3 MHz	—	-46	—	dB
	F ⩾ F0 + 4 MHz	—	-42	—	dB
	F ⩽ F0 – 4 MHz	—	-65	—	dB
Image frequency	+ 4 MHz	—	-42	—	dB
Adjacent channel to image frequency	$F = F_{image} + 1$ MHz	—	-53	—	dB
	$F = F_{image} - 1$ MHz	—	-32	—	dB

Table 4-46. Receiver Characteristics - Bluetooth LE 500 Kbps

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	-102	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	5	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-9	—	dB
	F = F0 – 1 MHz	—	-10	—	dB
	F = F0 + 2 MHz	—	-29	—	dB
	F = F0 – 2 MHz	—	-32	—	dB
	F = F0 + 3 MHz	—	-32	—	dB
	F = F0 – 3 MHz	—	-46	—	dB
	F ⩾ F0 + 4 MHz	—	-39	—	dB
	F ⩽ F0 – 4 MHz	—	-61	—	dB
Image frequency	+ 4 MHz	—	-39	—	dB
Adjacent channel to image frequency	$F = F_{image} + 1$ MHz	—	-52	—	dB
	$F = F_{image} - 1$ MHz	—	-32	—	dB

4.22. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = AVDD33_ANA = AVDD33_PA = AVDD33_CLK = 3.3 V, T_A = 25 ℃.

5. Package information

5.1. QFN40 package outline dimensions

Figure 5-1. QFN40 package outline

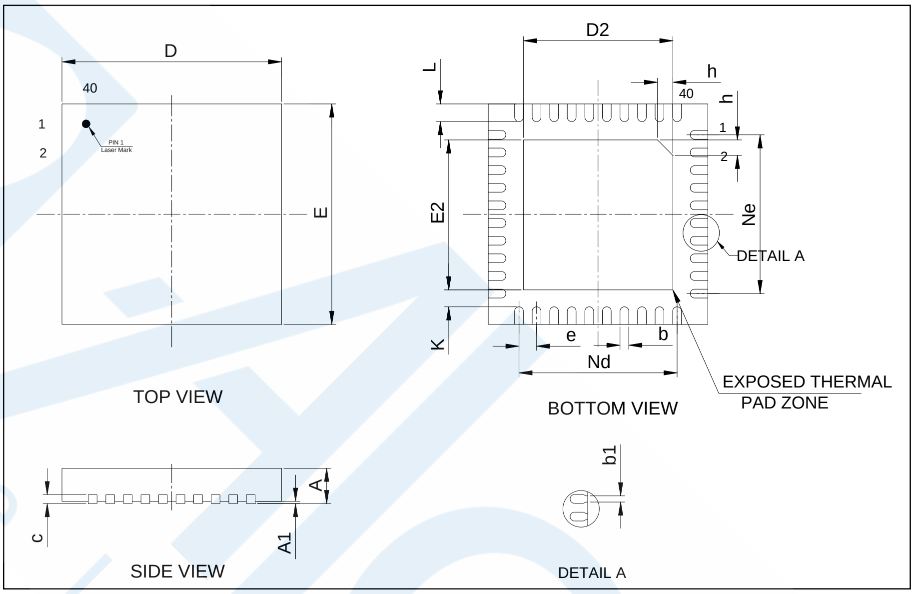
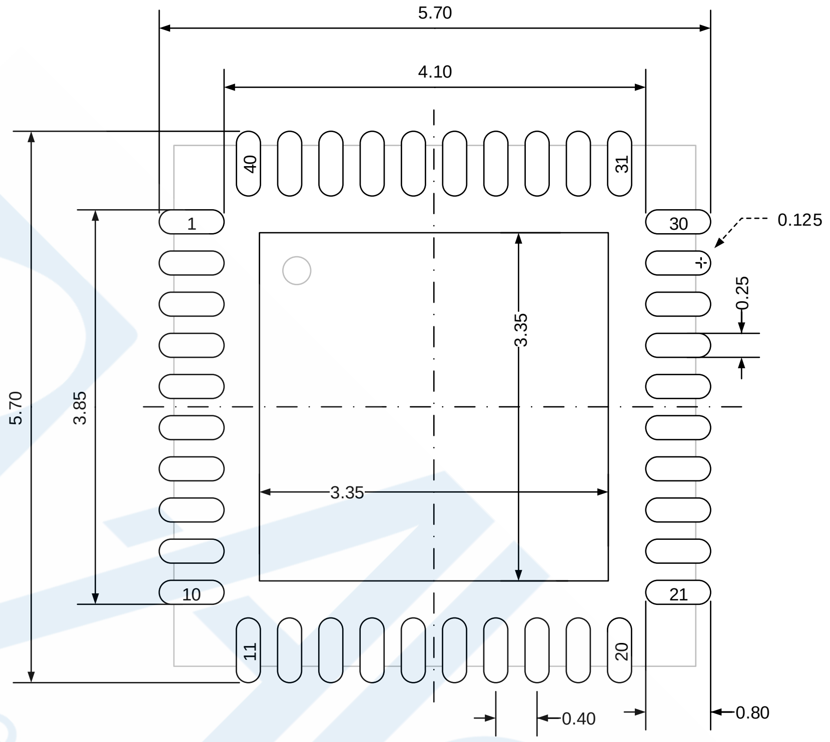


Table 5-1. QFN40 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
e	—	0.40	—
h	0.30	0.35	0.40
K	0.20	—	—
L	0.35	0.40	0.45
Nd	—	3.60	—
Ne	—	3.60	—

(Original dimensions are in millimeters)

Figure 5-2. QFN40 recommended footprint



(Original dimensions are in millimeters)

5.2. QFN32 package outline dimensions

Figure 5-3. QFN32 package outline

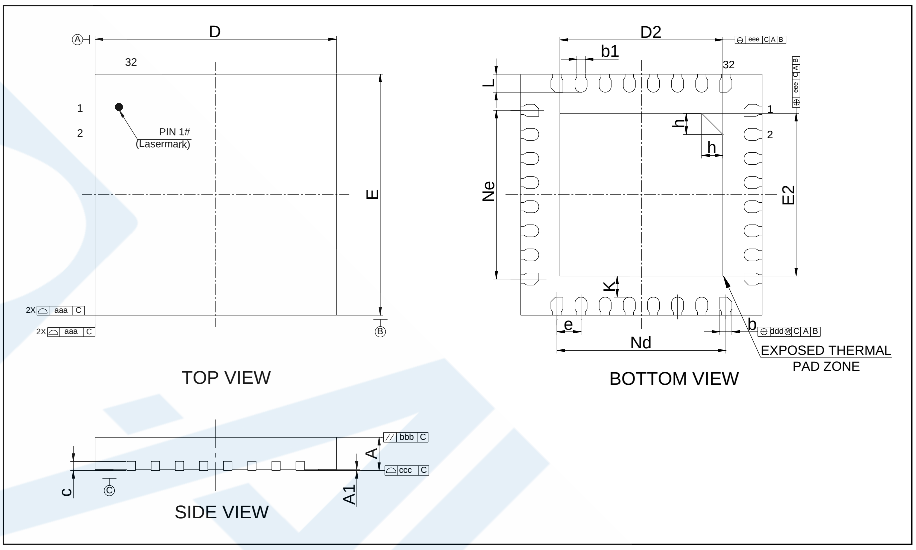
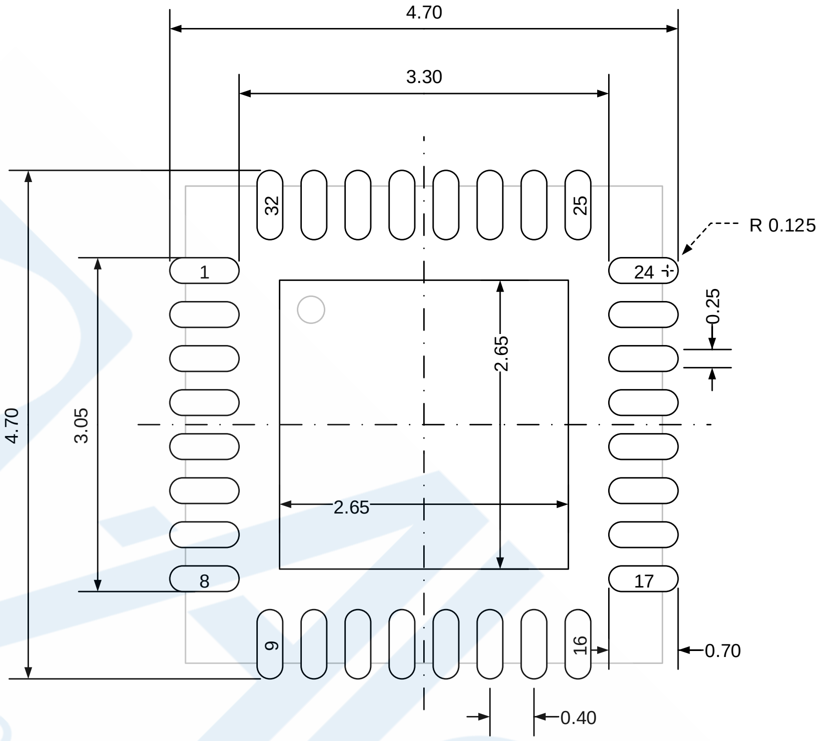


Table 5-2. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	—	0.152	—
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	—	0.40	—
h	0.30	0.35	0.40
K	—	0.35	—
L	0.25	0.30	0..35
Nd	—	2.80	—
Ne	—	2.80	—
aaa	—	0.10	—
bbb	—	0.10	—
ccc	—	0.08	—
ddd	—	0.10	—
eee	—	0.10	—

(Original dimensions are in millimeters)

Figure 5-4. QFN32 recommended footprint



(Original dimensions are in millimeters)

5.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$θ_{JA}$: Thermal resistance, junction-to-ambient.

$θ_{JB}$: Thermal resistance, junction-to-board.

$θ_{JC}$: Thermal resistance, junction-to-case.

$Ψ_{JB}$: Thermal characterization parameter, junction-to-board.

$Ψ_{JT}$: Thermal characterization parameter, junction-to-top center.

$$θ_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$θ_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$θ_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

$θ_{JA}$ represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower $θ_{JA}$ can be considerate as better overall thermal performance. $θ_{JA}$ is generally used to estimate junction temperature.

$θ_{JB}$ is used to measure the heat flow resistance between the chip surface and the PCB board.

$θ_{JC}$ represents the thermal resistance between the chip surface and the package top case. $θ_{JC}$ is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
$θ_{JA}$	Natural convection, 2S2P PCB	QFN40	47.85	°C/W
		QFN32	51.44	
$θ_{JB}$	Cold plate, 2S2P PCB	QFN40	17.97	°C/W
		QFN32	18.71	
$θ_{JC}$	Cold plate, 2S2P PCB	QFN40	16.85	°C/W

Symbol	Condition	Package	Value	Unit
		QFN32	21.85	
Ψ_{JB}	Natural convection, 2S2P PCB	QFN40	18.15	°C/W
		QFN32	17.69	
Ψ_{JT}	Natural convection, 2S2P PCB	QFN40	1.55	°C/W
		QFN32	0.99	

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32VW553xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32VW553HMQ7	4096	QFN40	Green	Industrial -40 °C to +105 °C
GD32VW553HMQ6	4096	QFN40	Green	Industrial -40 °C to +85 °C
GD32VW553HIQ7	2048	QFN40	Green	Industrial -40 °C to +105 °C
GD32VW553HIQ6	2048	QFN40	Green	Industrial -40 °C to +85 °C
GD32VW553KMQ7	4096	QFN32	Green	Industrial -40 °C to +105 °C
GD32VW553KMQ6	4096	QFN32	Green	Industrial -40 °C to +85 °C
GD32VW553KIQ7	2048	QFN32	Green	Industrial -40 °C to +105 °C
GD32VW553KIQ6	2048	QFN32	Green	Industrial -40 °C to +85 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct. 13, 2023
1.1	1. Update the flash size of GD32VW553HMQ6 in ***Table 2-1. GD32VW553xx devices features and peripheral list***.	Nov. 14, 2023

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.