



*Dimension 32x35x3.1mm (right picture)
and 44x46x5.3mm (incl. PCAP, left one)*

FEATURES

- 1.5" TFT FULL COLOR DISPLAY
- AACS TECHNOLOGY WITH IPS FOR UNLIMITED VIEWING ANGLE
- 240X240X3 DOTS, CONTROLLER LCD: ST7789V, CTP: ST1615
- 1100 OR 1000 CD/M² WITHOUT/WITH TOUCHPANEL
- 4 DIFFERENT INTERFACES AVAILABLE:
 - 18-BIT RGB INTERFACE
 - 8-BIT PARALLEL INTERFACE
 - 16-BIT PARALLEL INTERFACE
 - SPI INTERFACE
- WIDE TEMPERATURE RANGE (T_{OP} -20°C - +70°C)
- SUPPLY VOLTAGE 3.3V
- OPTIONALLY WITH OPTICAL BONDED PCAP AND CONTROLLER ST1615

ORDERING CODES

- 1.5" TFT, 240X240, IPS
- AS ABOVE, BUT WITH OPTICALLY BONDED PCAP

EA TFT015-22AINN
EA TFT015-22AITC

Accessories

- TEST BOARD WITH USB-INTERFACE
- BREAK-OUT BOARD 2.54 MM CONTACTS
- ZIF CONNECTOR 0.3MM, BOTTOM CONTACT

EA 9782-1USB
EA 9980-TFT
EA WF030-39S



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REVISION HISTORY

| Date | Rev. | Page(s) | Description |
|-------------------|-------------|----------------|--------------------|
| 2022-10-27 | 1.0 | All | First issue |

PRELIMINARY

GENERAL DESCRIPTION

With its new 1.5" TFT displays DISPLAY VISIONS launches the worldwide first small-sized quadratic displays with high-quality. With its IPS technology these displays provide full viewing angle with all-angle color stability management (AACs). This means that color stays same even when viewing angle is changing. So it can be used in directions without any disadvantage.

Display brightness is enormous with typ. over 1000cd/m² and paves the way for manifold applications in industrially and medically field, even for usage at direct sunlight.

The displays provide many interface modes like standard RGB interface which is suitable even for fast changing display content. The 4-wire SPI interface is perfect for pin saving applications and the 16-bit and 8-bit µC data bus interface enables parallel access to the display.

The version EA TFT015-22AITC comes with an optical bonded (OCA) PCAP touch panel. Interface is I²C which makes it easy to read out directly the coordinates.

The single connector for display interface, power supply for backlight and touch panel interface saves time in production. It also saves space on pcb because there's 1 single FPC connector necessary only. For SMD mount we do provide a connector EA WF030-39S as an accessory.

| Parameter | Specifications | Unit |
|----------------------|---|--------|
| Screen size | 1.54(Diagonal) | inch |
| Resolution | 240RGB(H)× 240(V) | Pixel |
| Active area | 27.72 x 27.72 | mm |
| Outline dimension | 32.0(W) x 35.0(H), (Exclude FPC) for details see dimension drawing | mm |
| Display Mode | Normally Black/Transmissive | |
| Driving method | TFT active matrix | |
| Pixel pitch | 0.1155(H)x0.1155(V) | mm |
| Input Signals | 4 line SPI / 4 line SPI +18 bit RGB / 8/16 bit MCU | |
| Surface treatment | - | |
| Color Depth | 262K | Color |
| View Angle direction | Free | |
| Temperature Range | Operation | -20~70 |
| | Storage | -30~80 |
| Input voltage | 3.3 | V |
| RoHS Compliance | RoHS | |

INTERFACE SIGNALS, PINOUT

| Pin No | Symbol | Function | Remark |
|--------|-----------|---|--------|
| 1 | LED- | Cathode of the backlight. | |
| 2 | LED+ | Anode of the backlight. | |
| 3 | VDD | Power supply for TFT and optional CTP | |
| 4 | GND | GND | |
| 5~22 | DB0~DB17 | Data bus | |
| 23 | DOTCLK | Dot clock signal for RGB interface operation. | |
| 24 | ENABLE | Data enable signal for RGB interface operation. Low: access enabled, High: access inhibited, | |
| 25 | HSYNC | Line synchronizing signal for RGB interface operation. | |
| 26 | VSYNC | Frame synchronizing signal for RGB interface operation. | |
| 27 | TE | Tearing effect signal is used to synchronize MCU to frame memory | |
| 28 | CSX | Chip selection pin; Low enable. High disable. | |
| 29 | SDA | The data is latched on the rising edge of the SCL signal. | |
| 30 | SDO | Serial data output | |
| 31 | DCX | Display data/command selection pin in parallel interface. This pin is used to be serial interface clock. DCX='1': display data or parameter. DCX='0': command data. If not used, please fix this pin at VDDI or DGND. | |
| 32 | WRX | Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface. Second Data lane in 2 data lane serial interface. If not used, please fix this pin at VDDI or DGND. | |
| 33 | RESET | This signal will reset the device and it must be applied to properly initialize the chip. Signal is active low. | |
| 34 | IM1+IM2 | Interface select | Note 1 |
| 35 | IM3 | Interface select | Note 1 |
| 36 | RDX | Read enable in 8080 MCU parallel interface. If not used, please fix this pin at VDDI or DGND. | |
| 37 | Touch CLK | I2C serial clock for CTP | Note 2 |
| 38 | Touch SDA | I2C serial data for CTP | Note 2 |
| 39 | Touch INT | Indicate coordinate data ready | Note 2 |

Note 1: Interface select table:

| IM3 | IM2 | IM1 | IM0 | MPU Interface Mode | Data pin |
|-----|-----|-----|-----|---------------------------|-----------------------|
| 0 | 0 | 0 | 0 | 80-8bit parallel I/F | DB[7:0] |
| 0 | 1 | 1 | 0 | 4-line 8bit serial I/F | SDA: in/out |
| 1 | 0 | 0 | 0 | 80-16bit parallel I/F II | DB[17:10], DB[8:1] |
| 1 | 1 | 1 | 0 | 4-line 8bit serial I/F II | SDA:in/ SDO: out |

Note 2: Pin 37-38 is NC for EA TFT015-22AINN, only necessary for version with CTP EA TFT015-22AITC

ELECTRICAL AND ENVIRONMENTAL SPECIFICATION

ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(GND=0V ,Ta=25°C)

| Item | Symbol | Min. | Max. | Unit | Note |
|------------------------------------|---------|------|------|------|------|
| Power Supply Voltage | VDD | -0.3 | +4.6 | V | |
| Logic Signal Input /Output Voltage | VDDI | -0.3 | +4.6 | V | |
| Driver Supply Voltage | VGH-VGL | -0.3 | +30 | V | |

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. VDD >GND must be maintained.
3. Please be sure users are grounded when handling LCD Module.

ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

| Item | Storage | | Operating | | Note |
|---------------------|---------|------|-----------|------|------|
| | MIN. | MAX. | MIN. | MAX. | |
| Ambient Temperature | -30°C | 80°C | -20°C | 70°C | 1,2 |

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature. The phenomenon is reversible.

ELECTRICAL SPECIFICATION TFT LCD PANEL

(GND=0V, Ta=25°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|------------------------------|--------|----------|---------|-----|---------|------|
| Power supply | VDD | 3.0 | 3.3 | 3.6 | V | |
| Input voltage | H | V_{IH} | 0.7*VDD | - | VDD | V |
| | L | V_{IL} | GND | - | 0.3*VDD | V |
| output voltage | H | V_{OH} | 0.8*VDD | - | VDD | V |
| | L | V_{OL} | GND | - | 0.2*VDD | V |
| TFT gate on voltage | VGH | - | 12 | - | V | |
| TFT gate off voltage | VGL | - | -7 | - | V | |
| TFT Common Electrode Voltage | VCOM | - | 0 | - | V | |

ELECTRICAL SPECIFICATION LED BACKLIGHT

(GND=0V, Ta=25°C)

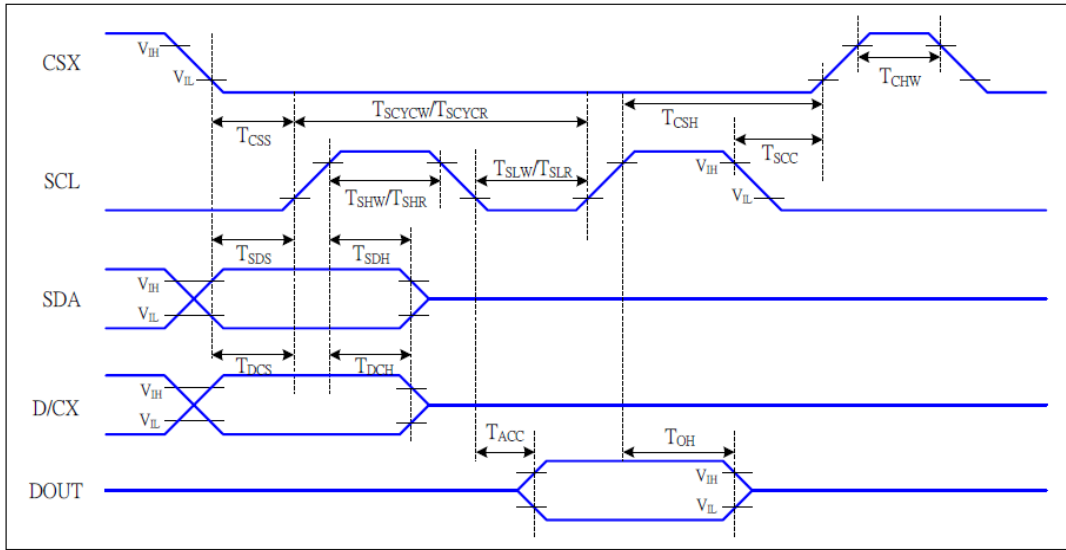
| Item | Symbol | Min | Typ | Max | Unit | Note |
|---------------------|--------|-------|-----|-----|------|------|
| Supply voltage | V_f | - | 3.1 | - | V | 1 |
| Supply current | I_f | - | 80 | - | mA | 2 |
| Life time | - | 30000 | - | - | Hr | 3 |
| Luminous Uniformity | Avg | 80 | - | - | % | |

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25°C and $I_f=80\text{mA}$.

Note 2: Constant current.

Note 3: The "life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and $I_L=80\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 80mA.

SERIAL INTERFACE CHARACTERISTICS (4-LINE SERIAL)

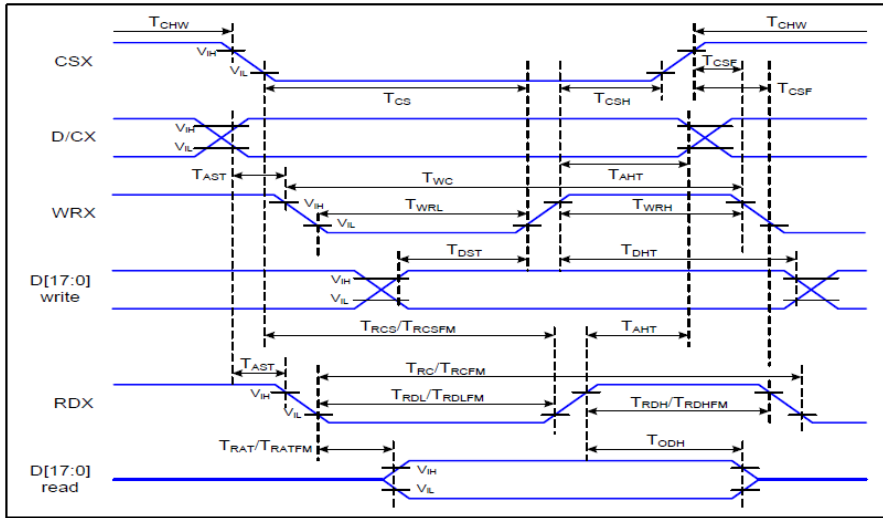


VDDI=1.65 to 3.6V, VDD=2.4 to 3.6V, AGND=DGND=0V, Ta=25 °C

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|-----------|-------------|--------------------------------|-----|-----|------|---------------------------|
| CSX | T_{CSS} | Chip select setup time (write) | 15 | | ns | |
| | T_{CSH} | Chip select hold time (write) | 15 | | ns | |
| | T_{CSS} | Chip select setup time (read) | 60 | | ns | |
| | T_{SCC} | Chip select hold time (read) | 65 | | ns | |
| | T_{CHW} | Chip select "H" pulse width | 40 | | ns | |
| SCL | T_{SCYCW} | Serial clock cycle (Write) | 16 | | ns | -write command & data ram |
| | T_{SHW} | SCL "H" pulse width (Write) | 7 | | ns | |
| | T_{SLW} | SCL "L" pulse width (Write) | 7 | | ns | |
| | T_{SCYCR} | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | T_{SHR} | SCL "H" pulse width (Read) | 60 | | ns | |
| | T_{SLR} | SCL "L" pulse width (Read) | 60 | | ns | |
| D/CX | T_{DCS} | D/CX setup time | 10 | | ns | |
| | T_{DCH} | D/CX hold time | 10 | | ns | |
| SDA (DIN) | T_{SDS} | Data setup time | 7 | | ns | |
| | T_{SDH} | Data hold time | 7 | | ns | |
| DOUT | T_{ACC} | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | T_{OH} | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8080 SERIES MCU PARALLEL INTERFACE CHARACTERISTICS



| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|----------|---------------------|------------------------------------|-----|-----|------|-----------------------------|
| D/CX | T _{AST} | Address setup time | 0 | | ns | - |
| | T _{AHT} | Address hold time (Write/Read) | 0 | | ns | |
| CSX | T _{CHW} | Chip select "H" pulse width | 0 | | ns | - |
| | T _{CS} | Chip select setup time (Write) | 15 | | ns | |
| | T _{RCS} | Chip select setup time (Read ID) | 45 | | ns | |
| | T _{RCSFM} | Chip select setup time (Read FM) | 355 | | ns | |
| | T _{CSF} | Chip select wait time (Write/Read) | 10 | | ns | |
| | T _{CSH} | Chip select hold time | 0 | | ns | |
| WRX | T _{WC} | Write cycle | 66 | | ns | - |
| | T _{WRH} | Control pulse "H" duration | 15 | | ns | |
| | T _{WRL} | Control pulse "L" duration | 15 | | ns | |
| RDX (ID) | T _{RC} | Read cycle (ID) | 160 | | ns | When read ID data |
| | T _{RDH} | Control pulse "H" duration (ID) | 90 | | ns | |
| | T _{RDL} | Control pulse "L" duration (ID) | 45 | | ns | |
| RDX (FM) | T _{RCFM} | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | T _{RDHFM} | Control pulse "H" duration (FM) | 90 | | ns | |
| | T _{RDLFM} | Control pulse "L" duration (FM) | 355 | | ns | |
| D[17:0] | T _{DST} | Data setup time | 10 | | ns | For CL=30pF |
| | T _{DHT} | Data hold time | 10 | | ns | |
| | T _{TRAT} | Read access time (ID) | | 40 | ns | |
| | T _{TRATFM} | Read access time (FM) | | 340 | ns | |
| | T _{ODH} | Output disable time | 20 | 80 | ns | |

Table 4 8080 Parallel Interface Characteristics

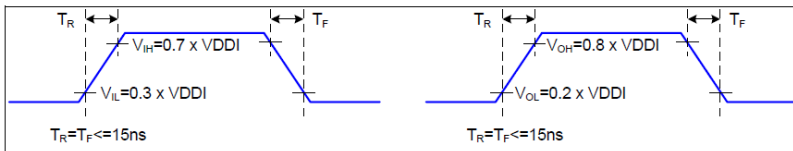


Figure 2 Rising and Falling Timing for I/O Signal

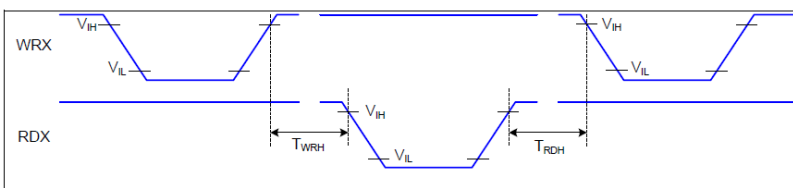
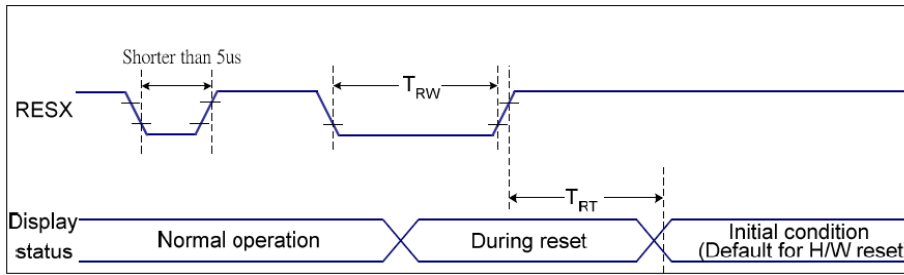


Figure 3 Write-to-Read and Read-to-Write Timing

RESET TIMING



VDDI=1.65 to 3.6V, VDD=2.4 to 3.6V, AGND=DGND=0V, Ta=25 °C

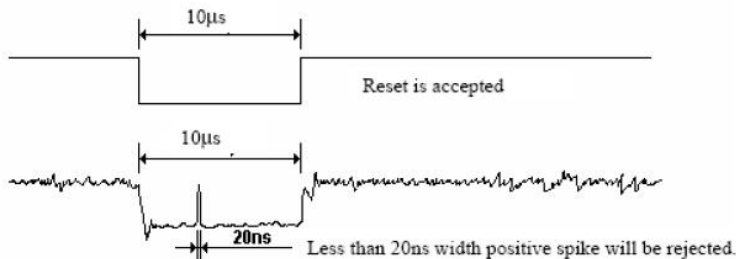
| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|--------------|--------|----------------------|--------------------|---------------|------|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| | | | 120 (Note 1, 6, 7) | ms | |

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

| RESX Pulse | Action |
|---------------------|----------------|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

RGB INTERFACE TIMING

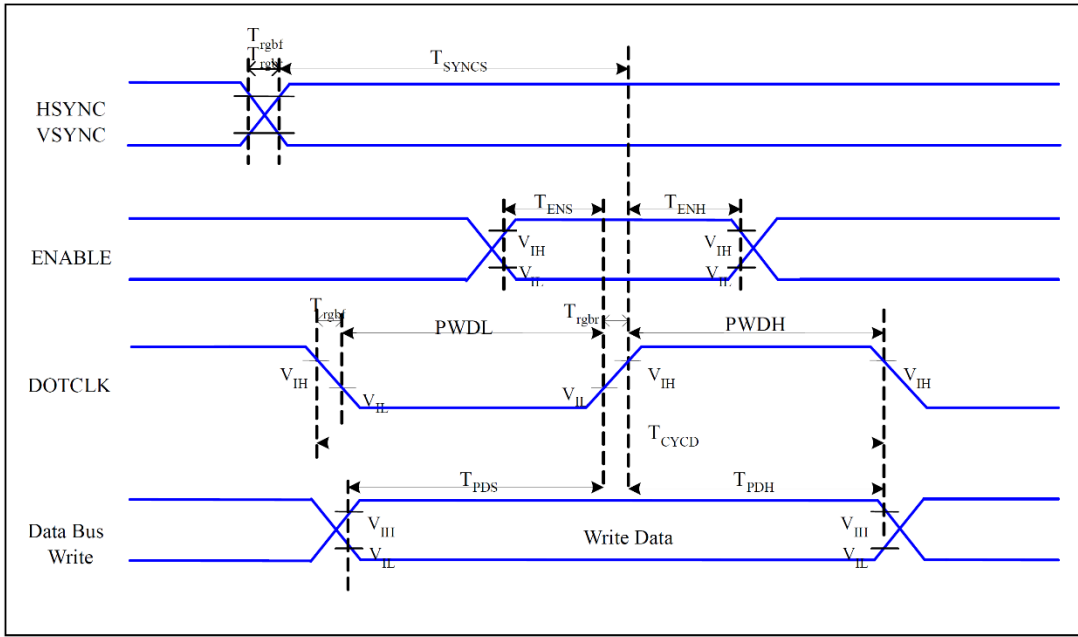


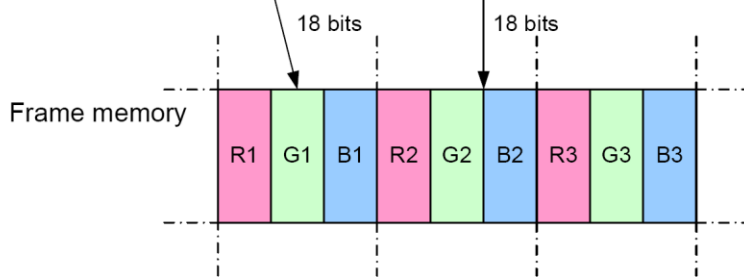
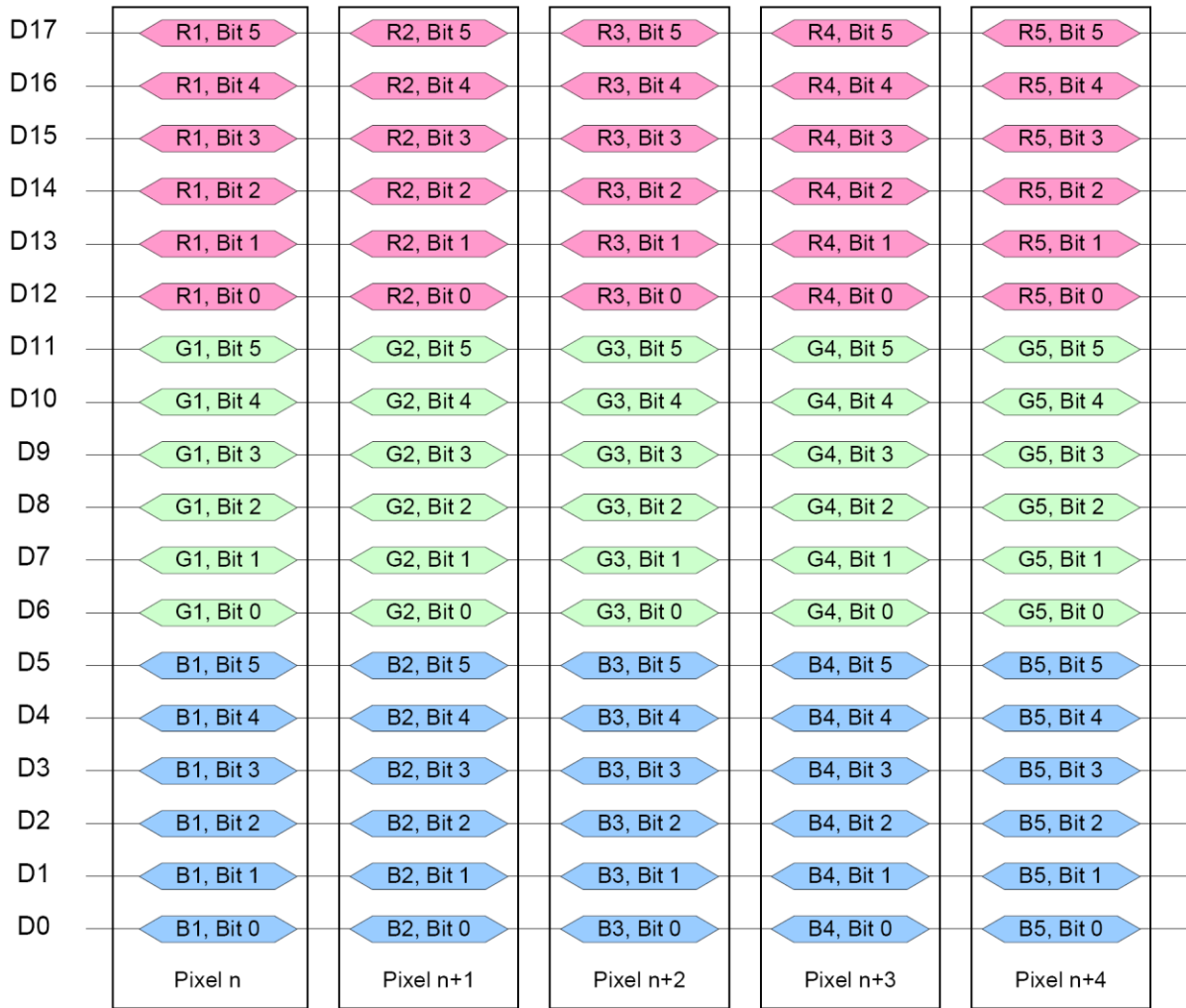
Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|--------------|-------------------|-------------------------------|-----|-----|------|-------------|
| HSYNC, VSYNC | T_{SYNC} | VSYNC, HSYNC Setup Time | 30 | - | ns | |
| ENABLE | T_{ENS} | Enable Setup Time | 25 | - | ns | |
| | T_{ENH} | Enable Hold Time | 25 | - | ns | |
| DOTCLK | PWDH | DOTCLK High-level Pulse Width | 60 | - | ns | |
| | PWDL | DOTCLK Low-level Pulse Width | 60 | - | ns | |
| | T_{CYCD} | DOTCLK Cycle Time | 120 | - | ns | |
| | Trghr, Trghf | DOTCLK Rise/Fall time | - | 20 | ns | |
| DB | T_{PDS} | PD Data Setup Time | 50 | - | ns | |
| | T_{PDH} | PD Data Hold Time | 50 | - | ns | |

RGB COLOR FORMAT

Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



RGB INTERFACE DEFINITION

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

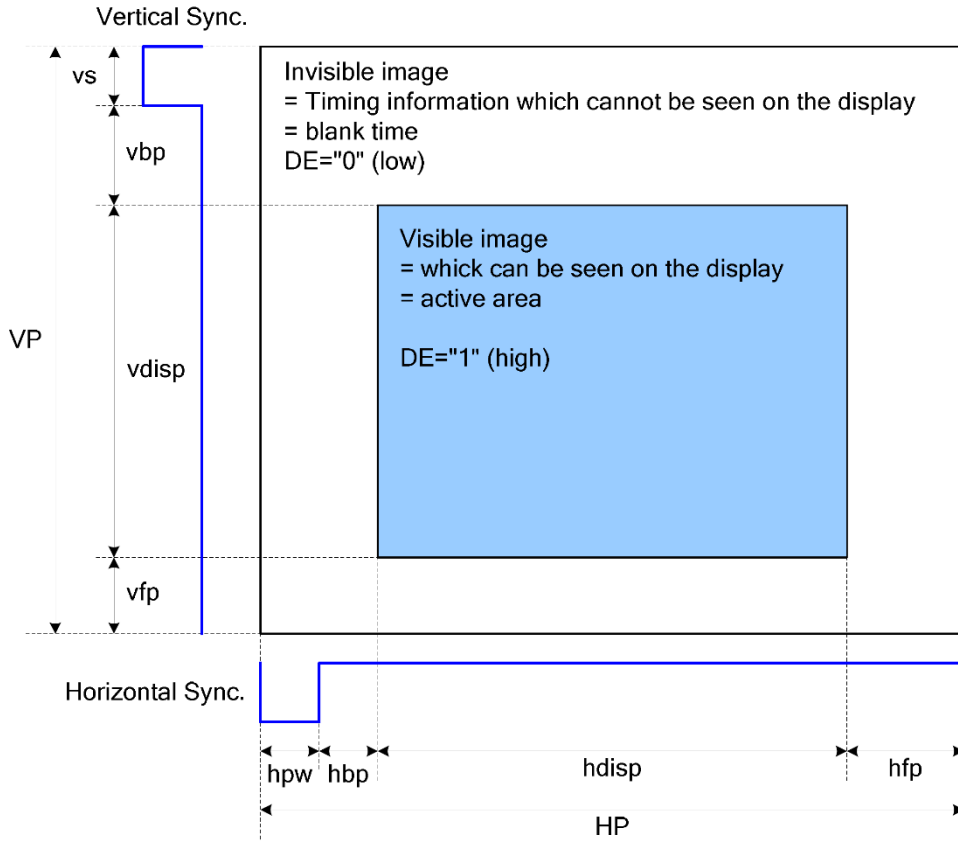


Figure 24 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|--------|------|------|------------|-------|
| Horizontal Sync. Width | hpw | 2 | 10 | hpw+hbp=31 | Clock |
| Horizontal Sync. Back Porch | hbp | 4 | 10 | | Clock |
| Horizontal Sync. Front Porch | hfp | 2 | 38 | - | Clock |
| Vertical Sync. Width | vs | 2 | 4 | vs+vbp=127 | Line |
| Vertical Sync. Back Porch | vbp | 2 | 4 | | Line |
| Vertical Sync. Front Porch | vfp | 2 | 8 | - | Line |

Note:

Typical value are related to the setting of dot clock is 7MHz and frame rate is 70Hz.

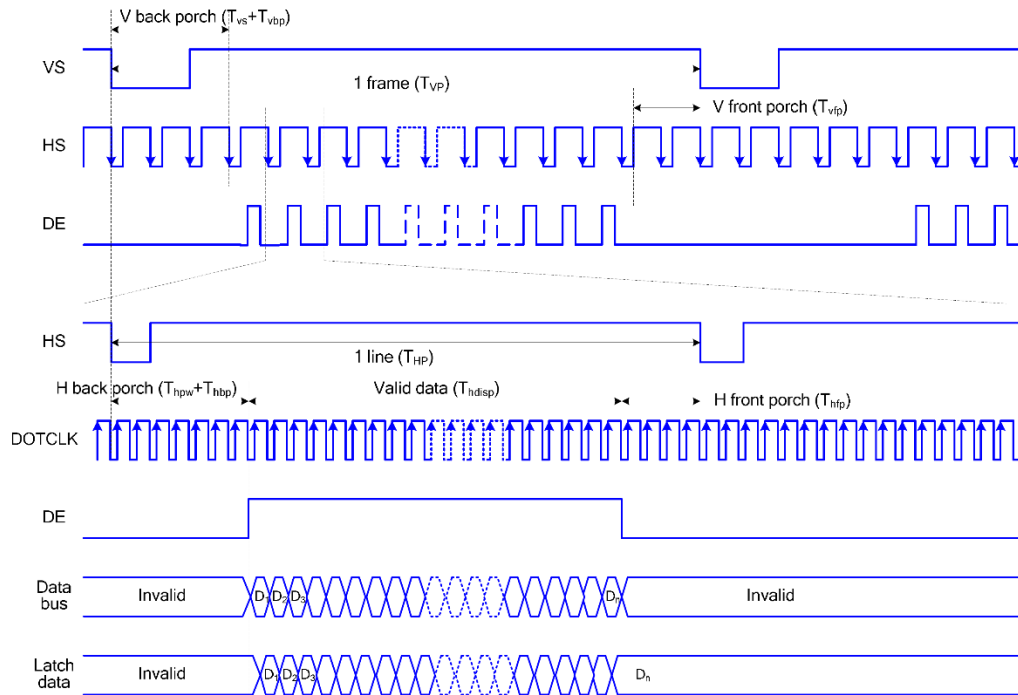
If the setting of hpw is 10 dot clocks and hbp is 10 dot clocks, the setting of HBP in command B1h is 20 dot clocks

In with ram mode, hpw+hbp+hfp ≥ 22

In without ram mode, hpw+hbp ≥ 20

RGB INTERFACE TIMING

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

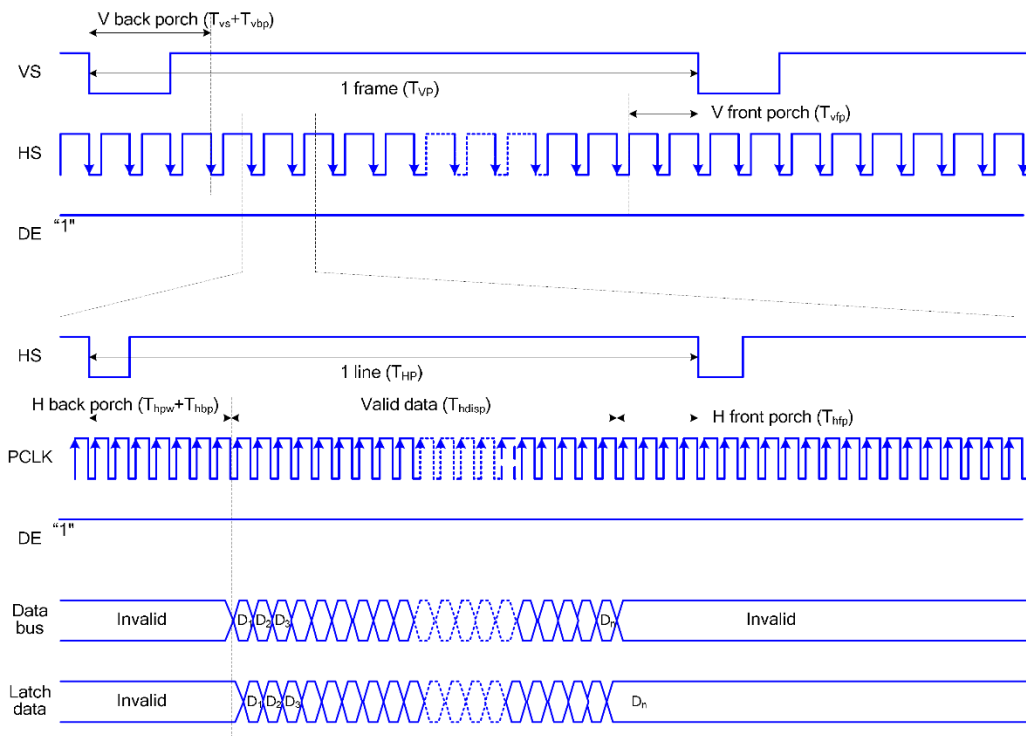


Figure 26 Timing chart of RGB interface HV mod

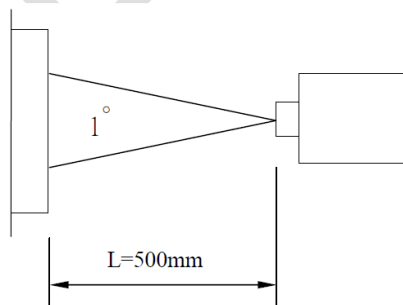
OPTICAL CHARACTERISTIC

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 °C. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

| Item | Condition. | Values | | | Unit | Note | |
|--------------------------|-----------------------------------|------------------|----------|------|-------------------|-------------|---------|
| | | Min. | Typ. | Max. | | | |
| 1) Contrast Ratio | Center | - | 900 | - | | Note(3) | |
| 2) Response time | T _{ON} +T _{OFF} | - | 30 | - | ms | Note (4) | |
| 3) Viewing Angle (CR≥10) | θ_L | $\Phi=180^\circ$ | - | 80 | - | Degree | Note(5) |
| | θ_R | $\Phi=0^\circ$ | - | 80 | - | | |
| | θ_T | $\Phi=90^\circ$ | - | 80 | - | | |
| | θ_B | $\Phi=270^\circ$ | - | 80 | - | | |
| 4) Chromaticity | Wx | Typ-0.05 | Typ+0.05 | TBD | | Note(2,6,7) | |
| | Wy | | | TBD | | | |
| | Rx | | | TBD | | | |
| | Ry | | | TBD | | | |
| | Gx | | | TBD | | | |
| | Gy | | | TBD | | | |
| | Bx | | | TBD | | | |
| | By | | | TBD | | | |
| 5) LCD Luminance | Surface L | 1100 | - | - | cd/m ² | Note(7) | |

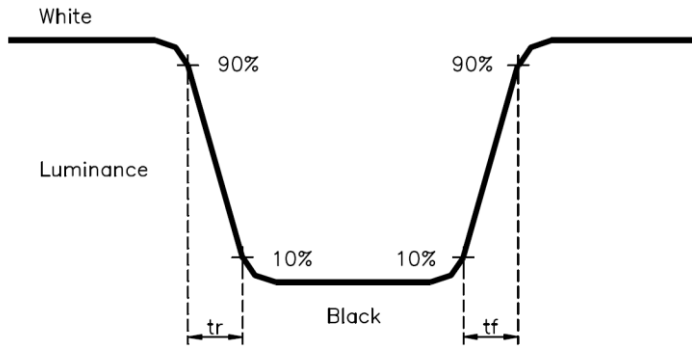
Note 1. Test Conditions: V_{DD}=3.3V, I_L=80mA (Backlight current).
Ambient condition: 25°C±2°C, 60±10%RH, under 10 Lux in the darkroom.

Note 2. Measure device: BM-5A (TOPCON), viewing cone=1°.

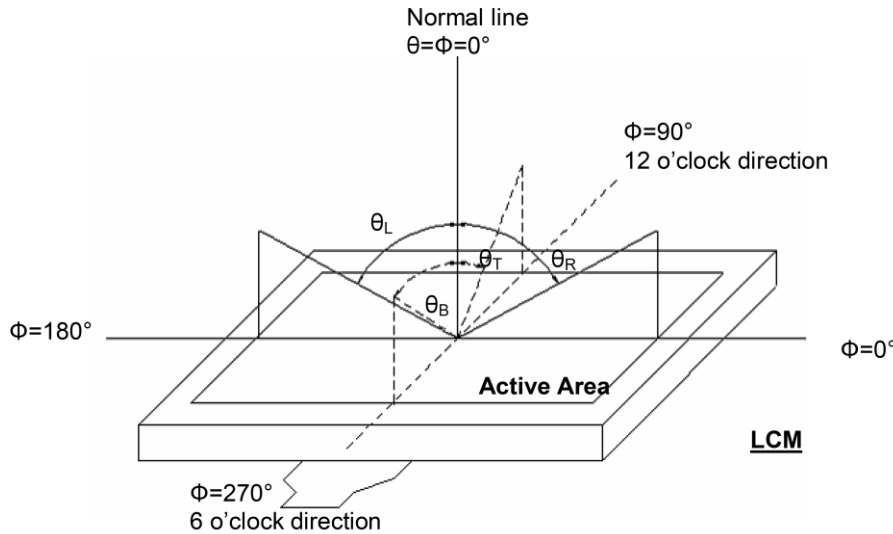


Note 3. Definition of Contrast Ratio:
CR = White Luminance (ON) / Black Luminance (OFF)

Note 4. Definition of response time: The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle (θ , Φ):



Note 6. Definition of color chromaticity (CIE1931), Color coordinates measured at center point of LCD.

Note 7. All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is $I_L = 60\text{mA}$.

Note 8. Light source: C light.

TOUCPANEL EA TFT015-22AITC ST771615

The display module EA TFT015-22AITC comes with optically bonded PCAP Touchpanel. The touch controller is included.

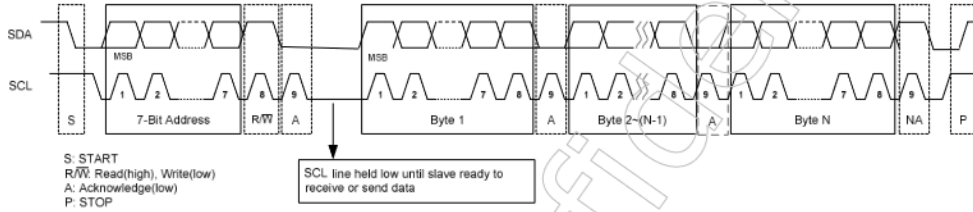
I²C HARDEWARE INTERFACE DESCRIPTION

The complete datasheet can be found under:

https://www.lcd-module.de/fileadmin/eng/pdf/zubehoer/ST1615_datasheet_v1.4.pdf

ST1615 is equipped with I²C interface, up tp 400 KHz.

Read



Write

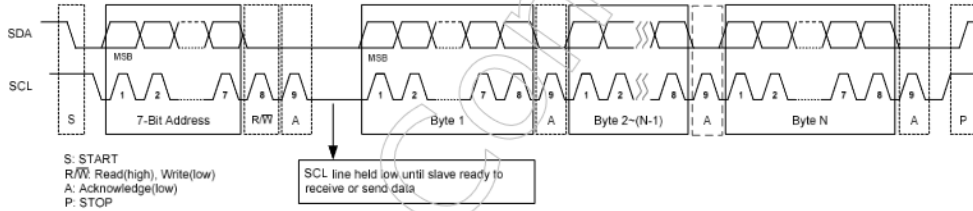


Figure 4-1 I2C Waveform

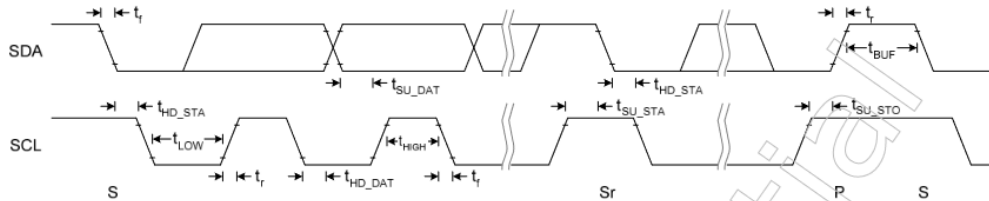


Figure 5-1 I2C Fast Mode Timing

Table 5-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

| Symbol | Parameter | Rating | | | Unit |
|---------------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| f _{SCL} | SCL clock frequency | 0 | - | 400 | kHz |
| t _{LOW} | Low period of the SCL clock | 1.3 | - | - | us |
| t _{HIGH} | High period of the SCL clock | 0.6 | - | - | us |
| t _f | Signal falling time | - | - | 300 | ns |
| t _r | Signal rising time | - | - | 300 | ns |
| t _{SU_STA} | Set up time for a repeated START condition | 0.6 | - | - | us |
| t _{HD_STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 0.6 | - | - | us |
| t _{SU_DAT} | Data set up time | 100 | - | - | ns |
| t _{HD_DAT} | Data hold time | 0 | - | 0.9 | us |
| t _{SU_STO} | Set up time for STOP condition | 0.6 | - | - | us |
| t _{BUF} | Bus free time between a STOP and START condition | 1.3 | - | - | us |
| C _b | Capacitive load for each bus line | - | - | 400 | pF |

I²C SOFTWARE PROTOCOL DESCRIPTION

The complete datasheet can be found under:

[https://www.lcd-module.de/fileadmin/eng/pdf/zubehoer/Sitronix Touch IC Protocol A V2.7.pdf](https://www.lcd-module.de/fileadmin/eng/pdf/zubehoer/Sitronix_Touch_IC_Protocol_A_V2.7.pdf)

| Host Interface Registers (Report Page) | | | | | | | | | |
|--|-----------------------------|-----------------------------|--------------------------|------------------------|-----------|--------------------|----------------------|-----------------|------------|
| Reg. Addr. | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x00 | Firmware Version | Version (RO) | | | | | | | |
| 0x01 | Status Reg. | Error Code (RO) | | | | Device Status (RO) | | | |
| 0x02 | Device Control Reg. | Reserv ed | Multi-Touch Disable (RW) | Proximi ty Enable (RW) | Reserv ed | Reserv ed | Deep Power Down (RW) | Power Down (RW) | Reset (RW) |
| 0x03 | Timeout to Idle Reg. | Timeout to Idle (sec.) (RW) | | | | | | | |
| 0x04 | XY Resolution (High Byte) | Reserv ed | X_Res_H (RO) | | | Reserv ed | Y_Res_H (RO) | | |
| 0x05 | X Resolution (Low Byte) | X_Res_L (RO) | | | | | | | |
| 0x06 | Y Resolution (Low Byte) | Y_Res_L (RO) | | | | | | | |
| 0x07 | Sensing Counter (High Byte) | Sensing_Counter_H (RO) | | | | | | | |
| 0x08 | Sensing Counter (Low Byte) | Sensing_Counter_L (RO) | | | | | | | |
| 0x09 ... 0x0B | ... | Reserved | | | | | | | |
| 0x0C | Firmware Revision 3 | FW_Rev_3 (RO) | | | | | | | |
| 0x0D | Firmware Revision 2 | FW_Rev_2 (RO) | | | | | | | |
| 0x0E | Firmware Revision 1 | FW_Rev_1 (RO) | | | | | | | |
| 0x0F | Firmware Revision 0 | FW_Rev_0 (RO) | | | | | | | |
| 0x10 | Advanced Touch Info. | Reserv ed | Proximi ty Flag (RO) | Water Flag (RO) | Reserv ed | Gesture Type(RO) | | | |
| 0x11 | Keys Reg. | Keys (RO) | | | | | | | |
| 0x12 | XY0 Coord. (High Byte) | Valid 0 (RO) | X0_H (RO) | | | Reserv ed | Y0_H (RO) | | |

IPRY

| Host Interface Registers (Report Page) | | | | | | | | | |
|--|------------------|---------------------------|----------|-------|-------|-------|-------|-------|-------|
| Reg. Addr. | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0xF1 | Misc. Control | Enable Smart Wake Up (RW) | Reserved | | | | | | |
| 0xF2 | Smart Wake Up ID | Smart Wake Up ID (RW) | | | | | | | |
| 0xF3 ... 0xFE | ... | Reserved | | | | | | | |
| 0xFF | Page Reg. | Page Number (RW) | | | | | | | |

Figure 4 – Host Interface Registers

QUALITY ASSURANCE

| | Test Items | Test Condition | REMARK |
|---|---|--|---------------|
| 1 | High Temperature Storage Test | Ta=+80°C Dry 240h | |
| 2 | Low Temperature Storage Test | Ta=-30°C Dry 240h | |
| 3 | High Temperature Operation Test | Ta=70°C Dry 240h | |
| 4 | Low Temperature Operation Test | Ta=-20°C Dry 240h | |
| 5 | High Temperature and High Humidity Operation Test | Ta=60°C 90%RH 240h | |
| 6 | Electro Static Discharge Test | Panel surface / top case. Contact / Air : ±6KV / ±8KV, 150pF, 330Ω | Non-operating |
| 7 | Vibration Test (non-operating) | Frequency range: 10Hz ~ 500Hz Sweep: 5G, Vibration: Sinusoidal Wave, 30min for X,Y,Z direction. | |
| 8 | Thermal Shock Test | -30°C(0.5h) ~ 80°C(0.5h) / 100 cycles | |

* Ta= Ambient Temperature

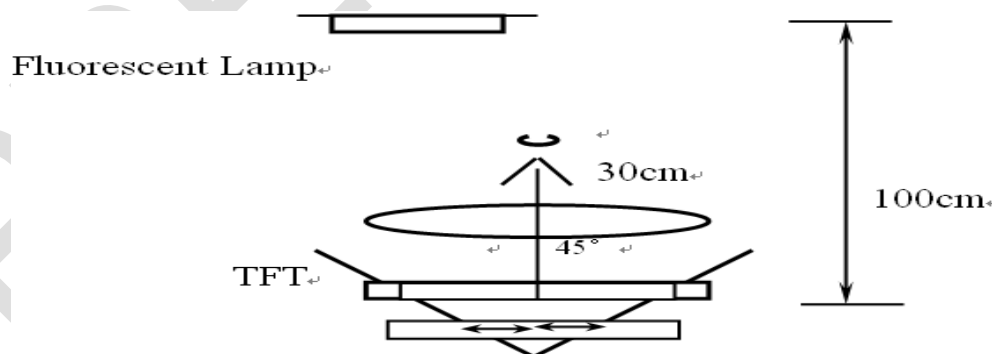
Note:

1. The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.
2. All the cosmetic specifications are judged before the reliability stress.

QUALITY UNITS

INSPECTION METHOD

An appearance inspection should be conducted at 30 cm or more distance/height from the inspector's eye sight to the LCD module surface under fluorescent light. The distance between LCD and fluorescent lamps should be 100 cm or more. Viewing angle for inspection is 45° from vertical against LCD.



QUALITY LEVEL

The AQL for major and minor defects is defined as follows:

DEFINITION

The environmental condition of inspection

1. Ambient temperature : 22°C±5°C, 65±20%RH
2. Function inspection : less than 300Lux
3. Visual inspection : 750±150Lux

DEFINITION OF DOT DEFECT

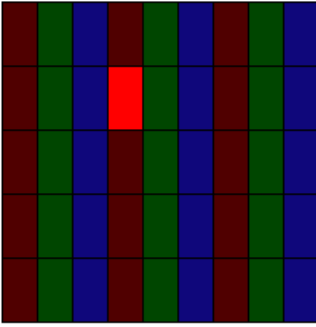
The size of a defective dot full of a whole dot and all bright dot or dark dot defect must be visible through ND 5% filter.

Bright dot

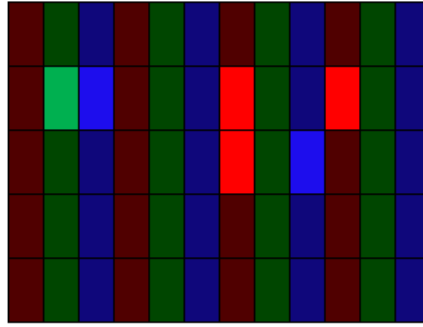
Dots appear bright and unchanged in size in which TFT is displaying.

| Partition | Definition | AQL |
|--------------|--|------|
| Major defect | Functional defective in product. | 0.25 |
| Minor defect | Meet all functions of product but have some cosmetic defective | 0.65 |

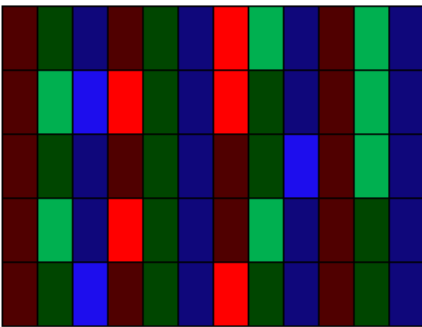
single dot



two adjacent dots



three adjacent dots



Dark dot

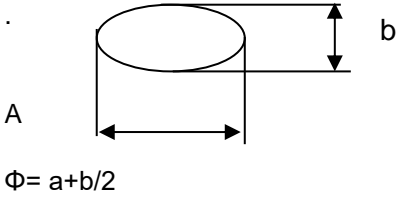
The same definition of bright dot, but always display dark

The usage of ND 5%

Use the ND 5% to cover bright dot within 2s, it should be judged OK if it's invisible.

VISUAL INSPECTION STANDARD

| Defect | Inspection | Criteria |
|-------------------------------|------------|--|
| 1 Corner Broken (Minor) | | 1. $A \leq 2.0 \text{ mm}$, $B \leq 2.0 \text{ mm}$, $C \leq T$ Ignore (No effect on function) 2. $A > 2.0 \text{ mm}$, or $B > 2.0 \text{ mm}$, Not allowed |
| 2 Corner Broken (Minor) | | 1. $A \leq 1.5 \text{ mm}$, $B \leq 1.5 \text{ mm}$, $C \leq T$ Ignore (No effect on function) 2. $A > 1.5 \text{ mm}$, or $B > 1.5 \text{ mm}$ Not allowed 3. To be applied to both CF and TFT glass |
| 3 Corner Broken (Minor) | | 1. $A \leq 1.5 \text{ mm}$, $B \leq 1.5 \text{ mm}$, $C \leq T$ Ignore (No effect on function) 2. $A > 1.5 \text{ mm}$, or $B > 1.5 \text{ mm}$ Not allowed 3. To be applied to both CF and TFT glass |
| 4 Pad Broken (Minor) | | 1. $A \leq 0.8 \text{ mm}$, $C \leq T$ Ignore B Length Ignore (No effect on function) 2. $A > 0.8 \text{ mm}$, Not allowed |
| 5 Side Broken (Minor) | | 1. $A \leq 0.8 \text{ mm}$, $C \leq T$ Ignore B Length Ignore (No effect on function) 2. $A > 0.8 \text{ mm}$, Not allowed |
| 6 Glass crack (Major) | | Not allowed |
| 7 | | |

| <p>Spot defect: (Minor)</p> | <p>Foreign/Black/White/Bright Spot/POL dent or bubble</p>  <p>$\Phi = a+b/2$</p> | <table border="1" data-bbox="922 246 1501 465"> <thead> <tr> <th>Dimensions</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1\text{mm}$</td> <td>Ignore</td> </tr> <tr> <td>$0.1\text{mm} < \Phi \leq 0.20\text{mm}$</td> <td>2</td> </tr> <tr> <td>$0.2\text{mm} < \Phi \leq 0.30\text{mm}$</td> <td>1</td> </tr> <tr> <td>$\Phi > 0.30\text{mm}$</td> <td>0</td> </tr> </tbody> </table> <p>Note: *1: defect that beyond AA area Ignored</p> | Dimensions | Acceptable Numbers | $\Phi \leq 0.1\text{mm}$ | Ignore | $0.1\text{mm} < \Phi \leq 0.20\text{mm}$ | 2 | $0.2\text{mm} < \Phi \leq 0.30\text{mm}$ | 1 | $\Phi > 0.30\text{mm}$ | 0 | | | | | | | | |
|--|--|---|------------|--------------------|--------------------------|--------|--|---|---|---|---------------------------|---|------|--------------------|------------------------|--------|---|---|---------------------------|--|
| Dimensions | Acceptable Numbers | | | | | | | | | | | | | | | | | | | |
| $\Phi \leq 0.1\text{mm}$ | Ignore | | | | | | | | | | | | | | | | | | | |
| $0.1\text{mm} < \Phi \leq 0.20\text{mm}$ | 2 | | | | | | | | | | | | | | | | | | | |
| $0.2\text{mm} < \Phi \leq 0.30\text{mm}$ | 1 | | | | | | | | | | | | | | | | | | | |
| $\Phi > 0.30\text{mm}$ | 0 | | | | | | | | | | | | | | | | | | | |
| <p>8 Line defect (Minor)</p> | <p>Scratch ; Fiber</p> | <p>Scratch :</p> <table border="1" data-bbox="922 680 1501 958"> <thead> <tr> <th>Dimensions</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03\text{mm}$</td> <td>Ignore</td> </tr> <tr> <td>$L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$</td> <td>2</td> </tr> <tr> <td>$L \leq 5\text{ mm}$ $0.05\text{mm} < W \leq 0.1\text{mm}$</td> <td>1</td> </tr> <tr> <td>Beyond Above, Not Allowed</td> <td></td> </tr> </tbody> </table> <p>Fiber:</p> <table border="1" data-bbox="922 1025 1501 1200"> <thead> <tr> <th>Size</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03\text{mm}$</td> <td>Ignore</td> </tr> <tr> <td>$L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$</td> <td>2</td> </tr> <tr> <td>Beyond Above, Not Allowed</td> <td></td> </tr> </tbody> </table> <p>Note: *1 : defect that beyond AA area Ignored</p> | Dimensions | Acceptable Numbers | $W \leq 0.03\text{mm}$ | Ignore | $L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$ | 2 | $L \leq 5\text{ mm}$ $0.05\text{mm} < W \leq 0.1\text{mm}$ | 1 | Beyond Above, Not Allowed | | Size | Acceptable Numbers | $W \leq 0.03\text{mm}$ | Ignore | $L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$ | 2 | Beyond Above, Not Allowed | |
| Dimensions | Acceptable Numbers | | | | | | | | | | | | | | | | | | | |
| $W \leq 0.03\text{mm}$ | Ignore | | | | | | | | | | | | | | | | | | | |
| $L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$ | 2 | | | | | | | | | | | | | | | | | | | |
| $L \leq 5\text{ mm}$ $0.05\text{mm} < W \leq 0.1\text{mm}$ | 1 | | | | | | | | | | | | | | | | | | | |
| Beyond Above, Not Allowed | | | | | | | | | | | | | | | | | | | | |
| Size | Acceptable Numbers | | | | | | | | | | | | | | | | | | | |
| $W \leq 0.03\text{mm}$ | Ignore | | | | | | | | | | | | | | | | | | | |
| $L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$ | 2 | | | | | | | | | | | | | | | | | | | |
| Beyond Above, Not Allowed | | | | | | | | | | | | | | | | | | | | |
| <p>9 (Minor)</p> | <p>glue on glass</p> | <p>1. Silicon area not match with document request reject 2. Silicon not cover with all effective ITO reject 4. Glue wet to the LCD upper POL or the bottom POL. And the connector over the LCD PIN. (Include FFC、FPC...etc reject</p> | | | | | | | | | | | | | | | | | | |
| <p>10 (Major)</p> | <p>IC/FPC</p> | <p>1. the line broken off reject 2. oxidation/broken/fold-injury in acute angle / distortion on golden fingers reject 3. FPC protection cover fix no good or deflection over the drawing request reject 4. Scratch/Surface Dirty or mark that doesn't affect display Ignored</p> | | | | | | | | | | | | | | | | | | |
| <p>11 (Minor)</p> | <p>Backlight</p> | <p>1. The size don't match with the drawing . reject 2. Surface Dirty or mark that can not wipe out Ignored 3. Scald reject 4. Uneven or Scratch on surface that doesn't affect display Ignored</p> | | | | | | | | | | | | | | | | | | |
| <p>12</p> | <p>Weld</p> | <p>1. tack weld reject</p> | | | | | | | | | | | | | | | | | | |

| | | |
|---------------|--------------|---|
| (Major) | | 2.welding short out reject 3.very little or too much tin reject 4.FPC cock reject |
| 13 (Minor) | protect film | Neglect any defect on protect film, such as: scratches/bubbles/particles |

PRELIMINARY

ELECTRONIC INSPECTION STANDARD:

| Defect | Inspection | Criteria | | | | | | | | | | | | | | |
|--|---|---|------------------------|-----------------------|---|------------|--|--------|---|--------|------------------------|----------|------------------------|----------|--------------------------|--------|
| 1 Spot defect (Minor) | Foreign particle/Black/Whit e spot/Bubble .etc. | <table border="1"> <thead> <tr> <th>Dimensions</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1\text{mm}$</td> <td>Ignore</td> </tr> <tr> <td>$0.1\text{mm} < \Phi \leq 0.20\text{mm}$</td> <td>2</td> </tr> <tr> <td>$0.2\text{mm} < \Phi \leq 0.30\text{mm}$</td> <td>1</td> </tr> <tr> <td>$\Phi > 0.30\text{mm}$</td> <td>0</td> </tr> </tbody> </table> | Dimensions | Acceptable Numbers | $\Phi \leq 0.1\text{mm}$ | Ignore | $0.1\text{mm} < \Phi \leq 0.20\text{mm}$ | 2 | $0.2\text{mm} < \Phi \leq 0.30\text{mm}$ | 1 | $\Phi > 0.30\text{mm}$ | 0 | | | | |
| | | Dimensions | Acceptable Numbers | | | | | | | | | | | | | |
| | | $\Phi \leq 0.1\text{mm}$ | Ignore | | | | | | | | | | | | | |
| | | $0.1\text{mm} < \Phi \leq 0.20\text{mm}$ | 2 | | | | | | | | | | | | | |
| | | $0.2\text{mm} < \Phi \leq 0.30\text{mm}$ | 1 | | | | | | | | | | | | | |
| $\Phi > 0.30\text{mm}$ | 0 | | | | | | | | | | | | | | | |
| Note: *1: defect that beyond AA area Ignored | | | | | | | | | | | | | | | | |
| 2 Line defect (Minor) | Scatched ; Fiber | Scratch: | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>Dimensions</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03\text{mm}$</td> <td>Ignore</td> </tr> <tr> <td>$L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$</td> <td>2, *1</td> </tr> <tr> <td>$L \geq 5\text{ mm}$ or $W \geq 0.05\text{ mm}$</td> <td>0</td> </tr> </tbody> </table> | Dimensions | Acceptable Numbers | $W \leq 0.03\text{mm}$ | Ignore | $L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$ | 2, *1 | $L \geq 5\text{ mm}$ or $W \geq 0.05\text{ mm}$ | 0 | | | | | | |
| | | Dimensions | Acceptable Numbers | | | | | | | | | | | | | |
| | | $W \leq 0.03\text{mm}$ | Ignore | | | | | | | | | | | | | |
| | | $L \leq 5\text{ mm}$ $0.03\text{mm} < W \leq 0.05\text{mm}$ | 2, *1 | | | | | | | | | | | | | |
| $L \geq 5\text{ mm}$ or $W \geq 0.05\text{ mm}$ | 0 | | | | | | | | | | | | | | | |
| Fiber: | | | | | | | | | | | | | | | | |
| <table border="1"> <thead> <tr> <th>Size</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03\text{mm}$</td> <td>Ignore , *1</td> </tr> <tr> <td>$L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$</td> <td>2; *2</td> </tr> <tr> <td colspan="2">Beyond Above, Not Allowed</td> </tr> </tbody> </table> | Size | Acceptable Numbers | $W \leq 0.03\text{mm}$ | Ignore , *1 | $L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$ | 2; *2 | Beyond Above, Not Allowed | | | | | | | | | |
| Size | Acceptable Numbers | | | | | | | | | | | | | | | |
| $W \leq 0.03\text{mm}$ | Ignore , *1 | | | | | | | | | | | | | | | |
| $L \leq 3\text{ mm}$ $0.03 < W \leq 0.05\text{mm}$ | 2; *2 | | | | | | | | | | | | | | | |
| Beyond Above, Not Allowed | | | | | | | | | | | | | | | | |
| Note: *1: defect that beyond AA area Ignored | | | | | | | | | | | | | | | | |
| 3 (Minor) | Bright/dark dot By sub-pixel | <table border="1"> <thead> <tr> <th>Dimensions</th> <th>Acceptable Numbers</th> </tr> </thead> <tbody> <tr> <td>Single bright dot</td> <td>$N \leq 1$</td> </tr> <tr> <td>Two adjacent bright dots</td> <td>reject</td> </tr> <tr> <td>Three adjacent bright dots</td> <td>reject</td> </tr> <tr> <td>Single dark dot</td> <td>≤ 2</td> </tr> <tr> <td>Two adjacent dark dots</td> <td>≤ 0</td> </tr> <tr> <td>Three adjacent dark dots</td> <td>reject</td> </tr> </tbody> </table> | Dimensions | Acceptable Numbers | Single bright dot | $N \leq 1$ | Two adjacent bright dots | reject | Three adjacent bright dots | reject | Single dark dot | ≤ 2 | Two adjacent dark dots | ≤ 0 | Three adjacent dark dots | reject |
| | | Dimensions | Acceptable Numbers | | | | | | | | | | | | | |
| | | Single bright dot | $N \leq 1$ | | | | | | | | | | | | | |
| | | Two adjacent bright dots | reject | | | | | | | | | | | | | |
| | | Three adjacent bright dots | reject | | | | | | | | | | | | | |
| | | Single dark dot | ≤ 2 | | | | | | | | | | | | | |
| | | Two adjacent dark dots | ≤ 0 | | | | | | | | | | | | | |
| Three adjacent dark dots | reject | | | | | | | | | | | | | | | |
| 1: The distance between dot defects should be more 5MM apart | | | | | | | | | | | | | | | | |
| 2: Total dot ≤ 2 | | | | | | | | | | | | | | | | |
| 4 (Minor) | Tiny Bright dot | Invisible by ND5% Filter, Ignore; | | | | | | | | | | | | | | |
| | | If visible, $\Phi \leq 0.1\text{mm}$, Ignore ; $0.1\text{mm} < \Phi \leq 0.30\text{mm}$, $N \leq 2$ | | | | | | | | | | | | | | |
| 5 (Major) | Display | 1. Missing segment, missing word reject | | | | | | | | | | | | | | |
| | | 2. no display. reject | | | | | | | | | | | | | | |
| | | 3. Viewing angle not right. reject | | | | | | | | | | | | | | |
| | | 4. Display abnormal reject | | | | | | | | | | | | | | |
| 6 (Major) | Mura/ hot spot/ Light leak (apply to all patterns) | judge by ND5% filter or limit sample | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | |
| 7 (Major) | flicker | judge by ND 5% filter in grey pattern or limit sample | | | | | | | | | | | | | | |

| | | |
|---------------|--------------------------------------|--|
| 8 (Major) | Electricity parameter (VoP/Current) | Over the production SPEC reject |
| 9 (Major) | Backlight | LED died off reject Display on uniformity Invisible by ND5% filter Brightness does not match the SPEC reject 4、 light leak Invisible by ND5% filter |
| 10 (Major) | Cross talk | Limit sample |

PRELIMINARY

INITIALISATION EXAMPLE

```

WriteComm(0x01);
Delay(200);

//-----
----//
WriteComm(0x11);
Delay(120); //Delay 120ms
//-----display and color format setting-----
//
WriteComm(0x36);
WriteData(0x00);
WriteComm(0x3a);
WriteData(0x05);
WriteComm(0x21);

//-----ST7789V Frame rate setting-----//
WriteComm(0xb2);
WriteData(0x05);
WriteData(0x05);
WriteData(0x00);
WriteData(0x33);
WriteData(0x33);
WriteComm(0xb7);
WriteData(0x35);
//-----ST7789V Power setting-----//
WriteComm(0xb8);
WriteData(0x2f);
WriteData(0x2b);
WriteData(0x2f);
WriteComm(0xbb);
WriteData(0x2B);
WriteComm(0xc0);
WriteData(0x2c);
WriteComm(0xc2);
WriteData(0x01);
WriteComm(0xc3);
WriteData(0x0b);
WriteComm(0xc4);
WriteData(0x20);
WriteComm(0xc6);
WriteData(0x11);
WriteComm(0xd0);
WriteData(0xa4);
WriteData(0xa1);
WriteComm(0xe8);
WriteData(0x03);
WriteComm(0xe9);
WriteData(0x0d);
WriteData(0x12);
WriteData(0x00);
//-----ST7789V gamma setting-----//
WriteComm(0xe0);
WriteData(0xd0);
WriteData(0x06);
WriteData(0x0b);
WriteData(0x0a);
WriteData(0x09);
WriteData(0x05);
WriteData(0x2e);
WriteData(0x43);
WriteData(0x44);

```

```

WriteData(0x09);
WriteData(0x16);
WriteData(0x15);
WriteData(0x23);
WriteData(0x27);

WriteComm(0xe1);
WriteData(0xd0);
WriteData(0x06);
WriteData(0x0b);
WriteData(0x09);
WriteData(0x08);
WriteData(0x06);
WriteData(0x2e);
WriteData(0x44);
WriteData(0x44);
WriteData(0x3a);
WriteData(0x15);
WriteData(0x15);
WriteData(0x23);
WriteData(0x26);

//-----Init RGB-Mode-----
WriteComm(0x3A); //Interface Pixel Format
WriteData(0x55); //RGB 65K Colors, Control interface 16bit/pixel

WriteComm(0xB0); //RAM access control
WriteData(0x11); //RGB interface access RAM, Display operation RGB interface
WriteData(0xE0); //16 Bit Farbformat R7 auf R0, MSB first, 18 bit bus width,

WriteComm(0xB1); //RGB interfacecontrol
WriteData(0xEF); //Direct RGB mode, RGB DE Mode, Control pins high active
WriteData(0x08); //VSYNC Back porch setting
WriteData(0x14); //HSYNC Back porch setting

//-----Display on-----
WriteComm(0x11);
Delay(120); //Delay 120ms

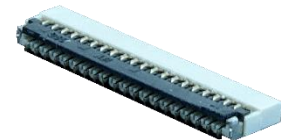
WriteComm(0x29);
Delay(100);

```

ACCESSORY EA WF030-39S

The 39-pin FFC cable is an all in one connection. It provides all signals for

- TFT interface
- LED backlight
- PCAP touchpanel



EA WF030-39S is a 39-pin ZIFF connector for bottom side contact.

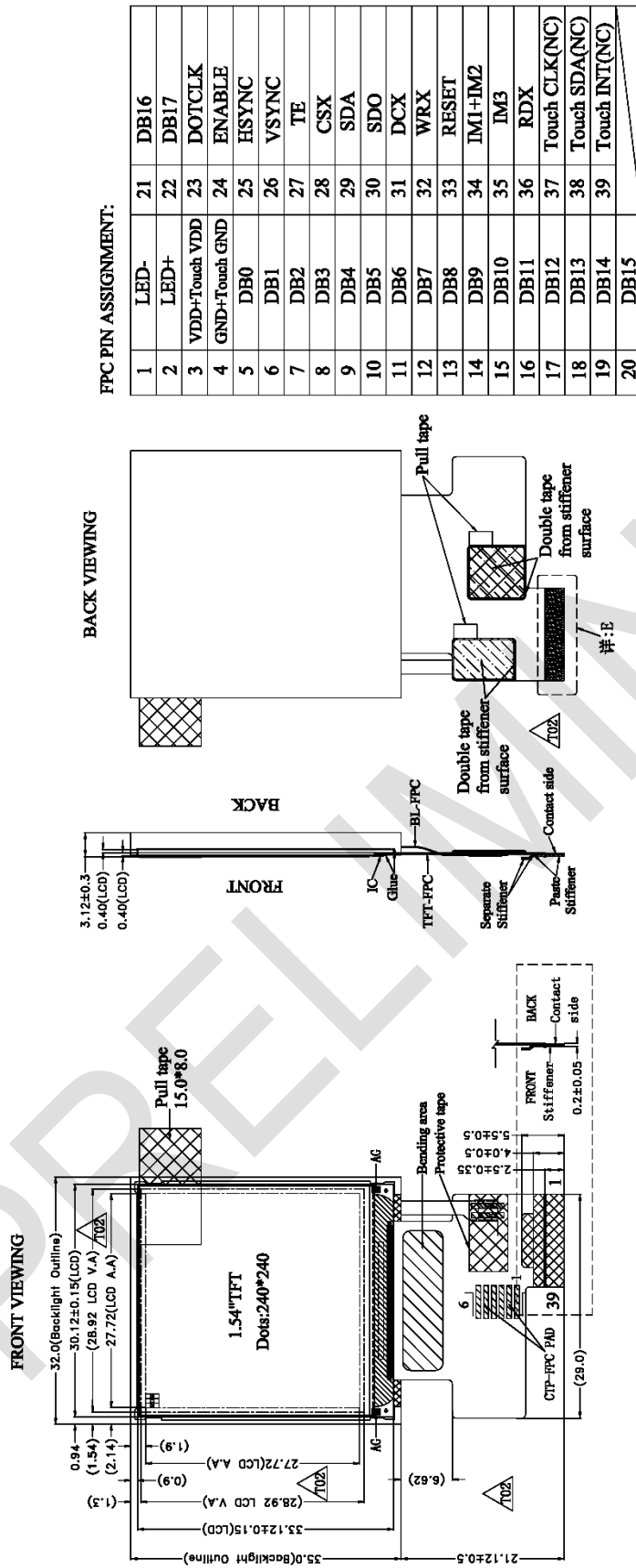
Datasheet: <https://www.lcd-module.de/eng/pdf/zubehoer/WF030-39S.pdf>

DIMENSION EA TFT015-22AINN

| ISSUB | MODIFY DESCRIPTION | DATE |
|-------|--------------------|------------|
| T01 | First Issue | 2022.01.05 |
| T02 | Modify FPC | 2022.10.27 |

Kind suggestion: VA of customer's application should be 0.5mm smaller than LCD VA in each side.

ROHS



| | |
|---|----------------------------|
| TITLE: Module Speciality | |
| PROJECT NO: EA TFT015-22AINN | DATE: 2022.10.27 |
| ▲: Special characteristic | ▽: Critical dimension |
| + : Safety characteristic | (...): Reference dimension |
| Tolerance unless: x.xx±0.3 Otherwise specified: x.xx±0.2 | |
| THIRD ANGLE PROJECTION | |
| DRAWN | SIGN |
| CHECKED | DATE |
| CHECKED | 2022.10.27 |
| APPROVED | |
| REV: T02 | UNIT: mm |
| SCALE: 1/1 | SHEET: 1 OF 2 |

Backlight circuit for reference:

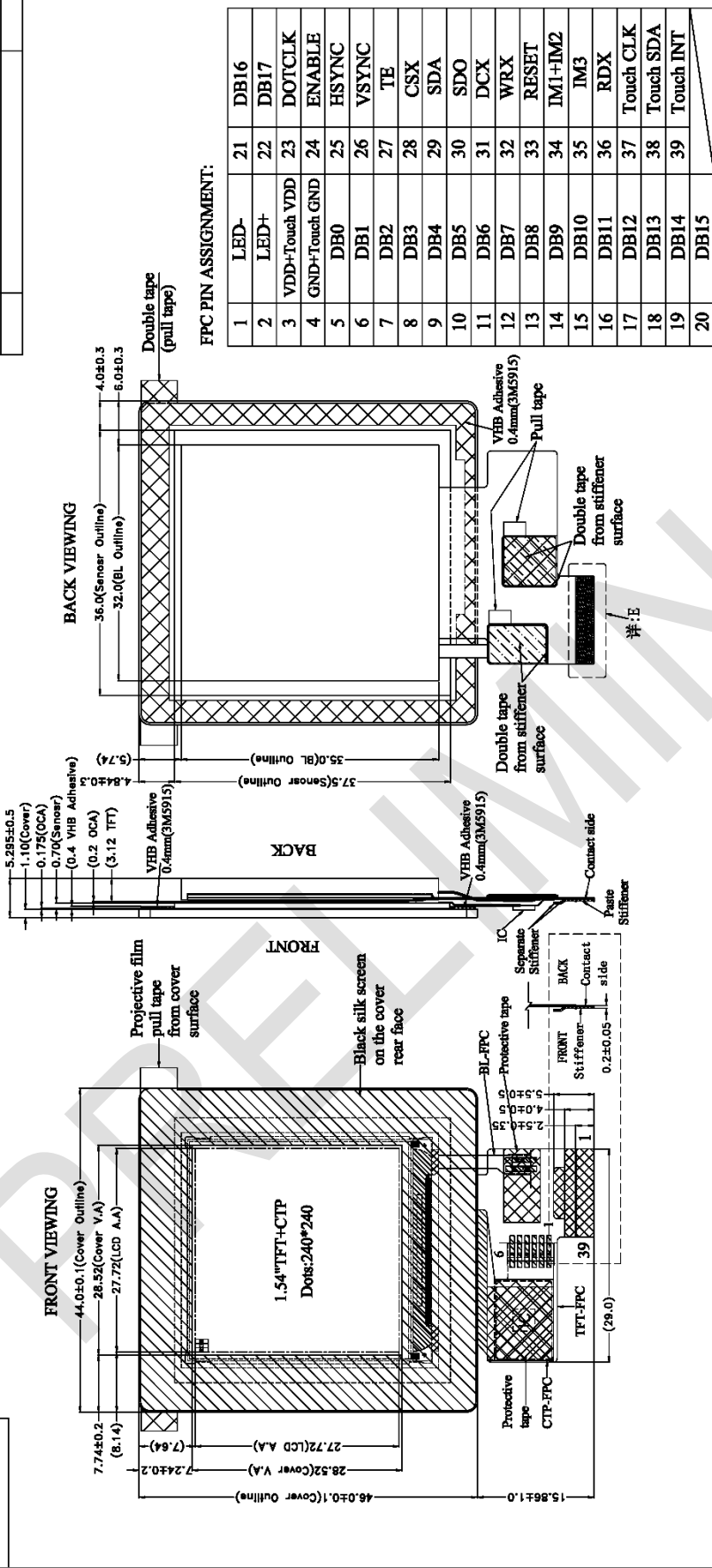
DISPLAY VISIONS
INDUSTRIAL SOLUTIONS

DIMENSION EA TFT015-22AITC

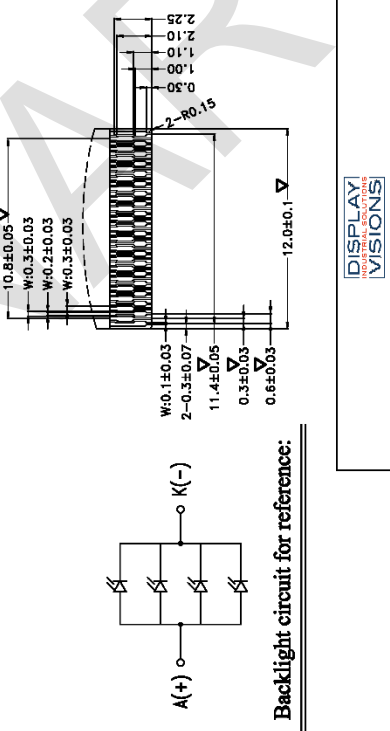
| ISSUE | MODIFY DESCRIPTION | DATE |
|-------|--------------------|------------|
| T01 | First Issue | 2022.01.05 |
| T02 | Modify FPC cable | 2022.10.26 |

Kind suggestion: VA of customer's application should be 0.5mm smaller than LCD VA in each side.

ROHS



| LED- | 21 | DB16 |
|---------------|----|-----------|
| LED+ | 22 | DB17 |
| VDD+Touch YDD | 23 | DOTCLK |
| GND+Touch GND | 24 | ENABLE |
| DB0 | 25 | HSYNC |
| DB1 | 26 | VSYNC |
| DB2 | 27 | TE |
| DB3 | 28 | CSX |
| DB4 | 29 | SDA |
| DB5 | 30 | SDO |
| DB6 | 31 | DCX |
| DB7 | 32 | WRX |
| DB8 | 33 | RESET |
| DB9 | 34 | IM1+IM2 |
| DB10 | 35 | IM3 |
| DB11 | 36 | RDX |
| DB12 | 37 | Touch CLK |
| DB13 | 38 | Touch SDA |
| DB14 | 39 | Touch INT |
| DB15 | | |



| | |
|---------------------------|---|
| Display Type | 1.54\"TFT-LCD / Normally black Transmissive + CTP |
| Display Resolution | DOTS:240*240 |
| Viewing Direction | ALL |
| Max.Ratio and Bias Level | ✓ |
| LCD&CTP Controller/Driver | LCD:ST7789VI (COG),CTP:ST1615(SMT) |
| Logic Voltage | 3.3V±0.3V(VDD) |
| LCD Driving Voltage | ✓ |
| Operation Temperature | -20°C TO 70°C |
| Storage Temperature | -30°C TO 80°C |
| Backlight Speciality | LED SIDE (WHITE),APCS VF=3.1V(TYP.),IF=80mA(Constant) Luminous of module is 1000cd/m2(MIN.) |
| Reliability Test | Normal |
| Remark | ✓ |

DISPLAY
INDUSTRIAL SOLUTIONS
VISIONS

| TITLE: | Module Speciality | | |
|---------------------------|------------------------------|------------|---------------|
| PROJECT NO: | EA TFT01522AITC | | |
| ▲: Special characteristic | ▽: Critical dimension | | |
| + : Safety characteristic | (...): Reference dimension | | |
| Tolerance unless x.x±0.3 | Otherwise specified x.xx±0.2 | | |
| THIRD ANGLE PROJECTION | | | |
| NAME | SIGN | DATE | |
| DRAWN | | 2022.10.26 | |
| CHECKED | | | |
| CHECKED | | | |
| APPROVED | | | |
| REV: T02 | UNIT: mm | SCALE: 1/1 | SHEET: 1 OF 2 |