TPA8023

2.25-V Input, Single-End Output Isolated Amplifier

Features

- Input Voltage Range: 2.25 V
- Single-End Input, Single-End Output
- Fixed Gain: 1
- Low Offset Error: 3 mV Maximum at 25°C
- Very Low Gain Error: 0.5% Maximum at 25°C
- Wide Temperature Range: −40°C to +125°C
- Basic Isolation: TPA8023-SO1R
- Reinforced Isolation: TPA8023-SOAR
- TPA8023-SO1R-S and TPA8023-SOAR-S are Qualified for Automotive Applications with the AEC-Q100 Reliability Test
- Safety-Related Certifications Finished:
  - 3750-V_{RMS} Isolation Rating per UL 1577 (SOP8)
  - 5000-V_{RMS} Isolation Rating per UL 1577 (WSOP8)
  - CQC, CSA Certifications

Applications

- Motor Control
- Power Supplies
- Automotive OBC

Description

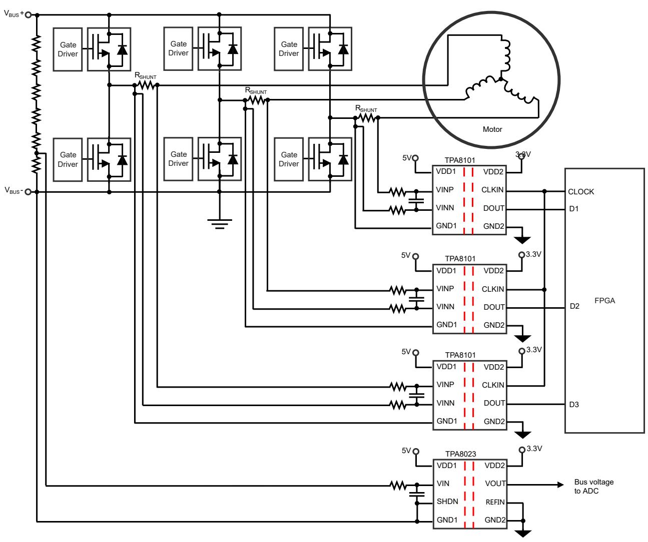
The TPA8023 is a precision, single-end input, single-end output isolated amplifier with an output separated from the input circuitry by a capacitive silicon dioxide insulation barrier. This barrier is certified to provide isolation of up to 3750-V_{RMS} according to UL1577 for the SOP8 version and 5000-V_{RMS} for the WSOP8 version.

The common mode transient immunity (CMTI) of the TPA8023 has been significantly enhanced through innovative circuit design and optimized structure.

The input of the device is high-impedance which can be connected to high-impedance resistive dividers or any other high-impedance voltage signal source. The device provides a single-end output which can be fed into single-end input of the next stage. The excellent performance of the device supports bus voltage in motor control or other applications.

The device is available in both SOP8 and WSOP8 packages, and is characterized from −40°C to +125°C.

Typical Application Circuit



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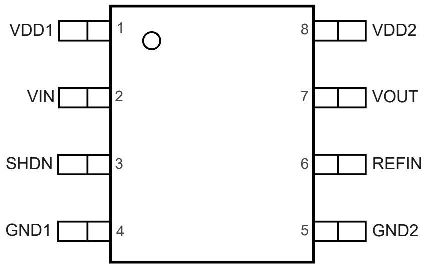
Revision History

Date	Revision	Notes
2024-03-20	Rev.A.0	Initial version
2024-09-12	Rev.A.1	The following updates are all about the new datasheet formats or typos, the actual product remains unchanged. • Updated the pin configuration of the SOP8 package top view. • Updated output noise specification. • Updated typos of insulation specifications, safety-related certifications, features specifications to align with the electrical characteristics table.
2025-02-19	Rev.A.2	• Added new part numbers TPA8023-SO1R-S and TPA8023-SOAR. • Modified Input Voltage Range from 2.2 V to 2.25 V. • Updated status of safety-related certificates. • Added detailed functional description of REFIN PIN. • Updated the POD format of the WSOP8.
2025-05-15	Rev.A.3	• Added a new part number: TPA8023-SOAR-S. • Updated safety-related certifications number and status, updated safety limiting values of WSOP and SOP packages.

Pin Configuration and Functions

TPA8023-SO1R
SOP8 Package
Top View



TPA8023-SOAR
WSOP8 Package
Top View

Table 1. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1		High-side power supply
2	VIN	Input	Analog input
3	SHDN	Input	Shutdown input, active high, with an internal pullup resistor. Connect to GND1 to enable the device.
4	GND1		High-side analog ground
5	GND2		Low-side analog ground
6	REFIN	Input	The voltage applied to this PIN is regarded as an offset to the output voltage of the device. Connect to GND2 if no need to offset the output voltage.
7	VOUT	Output	Analog output, refer to the voltage at the REFIN pin
8	VDD2		Low-side power supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VDD	Supply Voltage, VDD1 to GND1 or VDD2 to GND2	−0.3	7	V
V_{INPUT}	Analog Input Voltage at VIN	GND1 – 6	VDD1 + 0.5	V
	Analog Input Voltage at SHDN	GND1 – 0.5	VDD1 + 0.5	V
	Analog Output Voltage at VOUTP, VOUTN	GND2 – 0.5	VDD2 + 0.5	V
I_{IN}	Input Current to Any Pin except Supply Pins	−10	10	mA
T_J	Operating Virtual Junction Temperature		150	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection—TPA8023-SOAR and TPA8023-SO1R

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD, Electrostatic Discharge Protection—TPA8023-SO1R-S and TPA8023-SOAR-S

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC-Q100-002	2	kV
CDM	Charged Device Model ESD	AEC-Q100-011	1.5	kV

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VDD1	High-side Supply Voltage (VDD1 to GND1)	4.5	5.0	5.5	V
VDD2	Low-side Supply Voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T_A	Operating Ambient Temperature	−40	25	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	158	43	°C/W

Package Type	θ_{JA}	θ_{JC}	Unit
WSOP8	85	43	°C/W

Insulation Specifications

The value of UL and VDE is provided by lab tests.

Parameter		Conditions	Value	Value	Unit
			SOP8	WSOP8	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	4.0	8.0	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	4.0	8.0	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	22	22	μm
DTC	Distance through the Molding Compound	Minimum internal distance across the conductors inside the package	0.45	0.8	mm
CTI	Comparative Tracking Index		> 600	> 600	V
	Material Group	According to IEC 60664-1	I	I	
	Over-voltage Category	For Rated Mains Voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		For Rated Mains Voltage ≤ 300 V_{RMS}	I-III	I-IV	
		For Rated Mains Voltage ≤ 600 V_{RMS}	I-II	I-IV	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I	I-III	
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
DIN V VDE V 0884-17 (1)(2)					
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage	990	1700	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	700	1200	V_{RMS}
		DC voltage	990	1700	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5300	7000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage (3)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM} (qualification)	5980	6500	V_{PK}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type	≤ 5	≤ 5	

Parameter		Conditions	Value SOP8	Value WSOP8	Unit
		test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s			
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T A= 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T A≤ 125°C	> 10^{11}	> 10^{11}	Ω
		V_{IO} = 500 V at T S= 150°C	> 10^{9}	> 10^{9}	Ω
UL 1577					
V_{ISO}	Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s(qualification); V_{TEST}= 1.2 × V_{ISO}, t = 1 s (100% production)	3750	5000	V_{RMS}

(1) All pins on each side of the barrier are tied together creating a two-terminal device.
(2) This coupler is suitable for safe electrical insulation only within the safety operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing must be carried out in oil.

Safety-Related Certifications

UL and CSA	CQC
Certified according to UL 1577 and CSA Component Acceptance Notice 5A	Certified according to GB 4943.1
Report Reference E524241	Certificate No. CQC23001393276

Safety Limiting Values

Parameter	Conditions (1)	Min	Typ	Max	Unit
Safety Input, Output, or Supply Current	$R_{θJA}$ = 85°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C, WSOP8 Package			134	mA
	$R_{θJA}$ = 158°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C, SOP8 Package			72	mA
Safety Total Power	$R_{θJA}$ = 85°C/W, T_J = 150°C, T_A = 25°C, WSOP8 Package			735	mW
	$R_{θJA}$ = 158°C/W, T_J = 150°C, T_A = 25°C, SOP8 Package			396	mW
Maximum Safety Temperature				150	°C

(1) The assumed junction-to-air thermal resistance in the Thermal Information is that of a device installed on a high-K test board for leaded surface-mount packages.

Electrical Characteristics

Minimum and maximum specifications apply from T_A= –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VIN = 0.1 V to 2 V (unless otherwise noted); typical specifications are at T_A= 25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

Parameter		Conditions	Min	Typ	Max	Unit
Analog Input						
$V_{Clipping}$	Input Voltage before Clipping Output	IN to GND1		2.5		V
V_{FSR}	Specified Linear Full-scale Voltage (1)	IN to GND1	0.1		2.25	V
	Specified Linear Full-scale Voltage	IN to GND1	0.1		2	V
V_{OS}	Input Offset Voltage	VDD1 = 5V, VDD2 = 5V, In VFSR, T_A= 25°C	–3	0.5	3	mV
		In 0V to 0.1V, T_A= 25°C		10		mV
TCV_{OS}	Input Offset Drift (1)	In VFSR		10	30	μV/°C
C_{IND}	Differential Input Capacitance			7		pF
R_{IN}	Single-ended Input Resistance	VINN = GND1		1		GΩ
I_{IB}	Input bias Current	IN = GND1, T_A = 25℃	–15	3	15	nA
Analog Output						
	Nominal Gain	VIN at VFSR		1		
E_G	Gain Error	VDD1 = 5 V, VIN at VFSR, T_A= 25°C	–0.5	±0.05	0.5	%
TCE_G	Gain Error Drift (1)	VDD1 = 5 V, VIN at VFSR	–100	±30	100	ppm/°C
	Nonlinearity (1)		–0.02	±0.01	0.02	%
	Nonlinearity Drift			1		ppm/°C
THD	Total Harmonic Distortion	f_{IN}= 10 kHz		–80		dB
	Output Noise	VIN = GND1, BW = 100 kHz		300		μVRMS
SNR	Signal-to-noise Ratio	f_{IN}= 1 kHz, BW = 10 kHz		80		dB
		f_{IN}= 10 kHz, BW = 100 kHz		62		dB
PSRR	Power-supply Rejection Ratio	vs VDD1, at dc		–70		dB
		vs VDD1, 100-mV and 10-kHz ripple		–70		dB
		vs VDD2, at dc		–65		dB
		vs VDD2, 100-mV and 10-kHz ripple		–65		dB
CMTI	Common-mode Transient Immunity	|GND1 – GND2| = 1 kV		100		kV/μs
	Input Voltage Range of REFIN		0		VDD2 – 2.5	V
	Input Resistance of REFIN			145		kΩ

Parameter		Conditions	Min	Typ	Max	Unit
	Output Short-circuit Current			±15		mA
R_{OUT}	Output Resistance			< 0.2		Ω
BW	Output Bandwidth			300		kHz
Digital Input						
	Input Voltage	SHDN to GND1	0		VDD1	V
I_{IN}	Input Current	SHDN pin, GND1 ≤ SHDN ≤ VDD1	–70		1	μA
C_{IN}	Input Capacitance	SHDN pin		5		pF
V_{IH}	High-level Input Voltage	Shutdown	0.7 × VDD1			V
V_{IL}	Low-level Input Voltage	Enable			0.3 × VDD1	V
Power Supply						
	VDD1 Undervoltage Detection Threshold	VDD1 falling		2		V
	VDD2 Undervoltage Detection Threshold	VDD2 falling		2		V
IDD1	High-side Supply Current	VDD1 = 5.5 V		15	18	mA
IDD2	Low-side Supply Current	VDD2 = 3 V		8	10	mA
		VDD2 = 5.5 V		9	11	mA
Switching Characteristics						
t_r	Rise Time			1		μs
t_f	Fall Time			1		μs
	V_{IN} to V_{OUT} signal delay (50% – 10%) (1)			0.9	1.4	μs
	V_{IN} to V_{OUT} signal delay (50% – 50%) (1)			1.5	2.0	μs
	V_{IN} to V_{OUT} signal delay (50% – 90%) (1)			2.0	2.7	μs
	Analog Settling Time	VDD1 step to 5.0 V with VDD2 ≥ 3.0 V, to VOUTP, VOUTN valid, 0.1% settling		500		μs
	Enable Time	Set SHDN high to low		35		μs
	Shutdown Time	Set SHDN low to high		2		μs

(1) Provided by bench tests and design simulation.

Typical Performance Characteristics

All test conditions: VDD1 = 5 V, VDD2 = 3.3 V, SHDN = 0 V, unless otherwise noted.

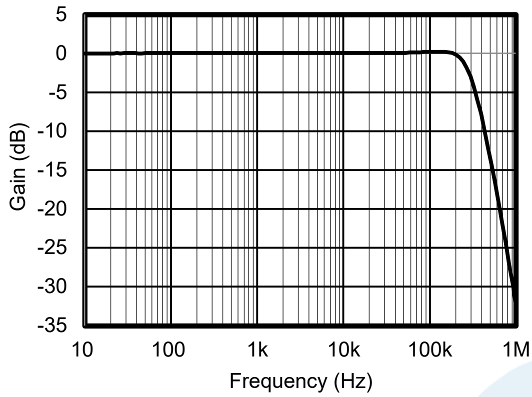


Figure 1. Normalized Gain vs. Input Frequency

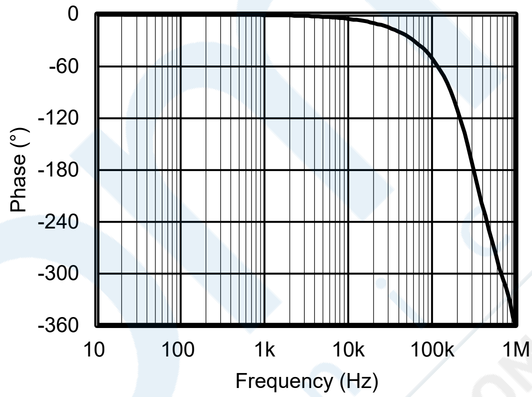


Figure 2. Phase vs. Input Frequency

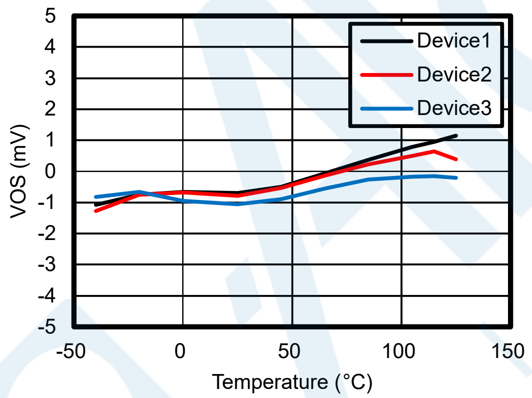


Figure 3. VOS vs. Temperature

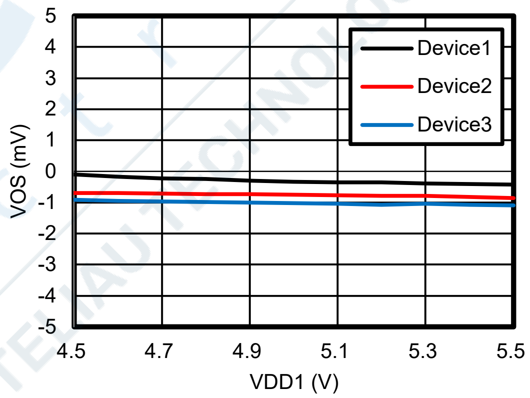


Figure 4. VOS vs. VDD1

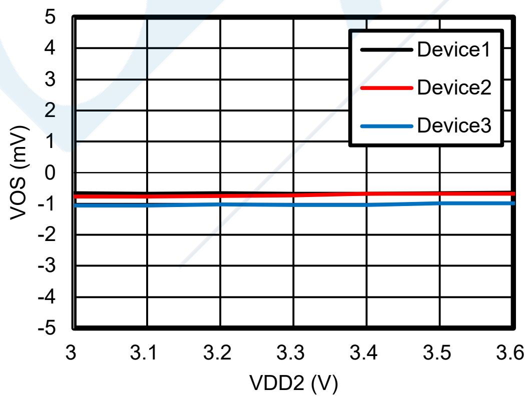


Figure 5. VOS vs. VDD2

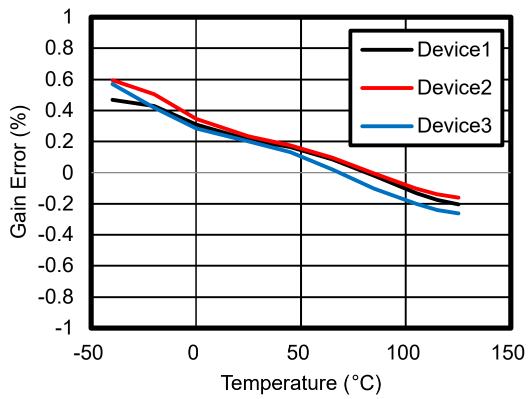


Figure 6. Gain Error vs. Temperature

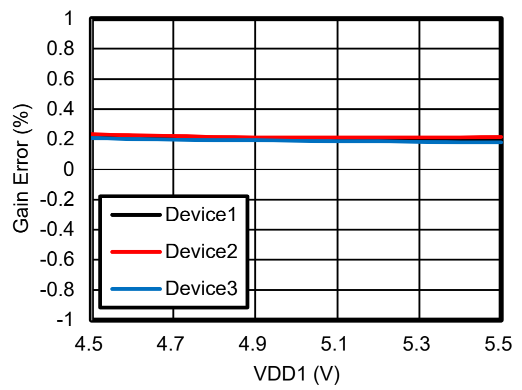


Figure 7. Gain Error vs. VDD1

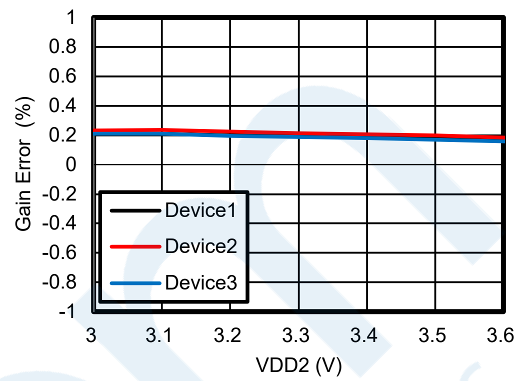


Figure 8. Gain Error vs. VDD2

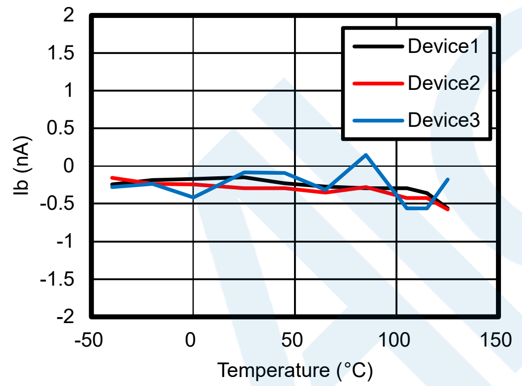


Figure 9. IB vs. Temperature

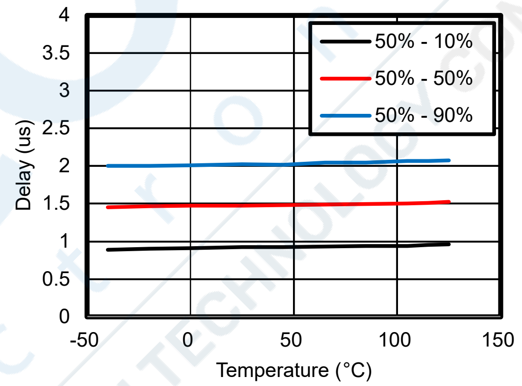


Figure 10. Signal Delay vs. Temperature

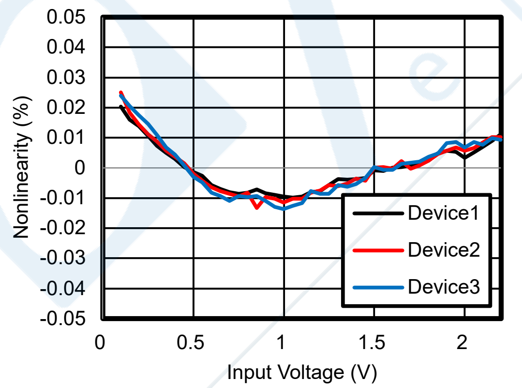


Figure 11. Nonlinearity vs. Input Voltage

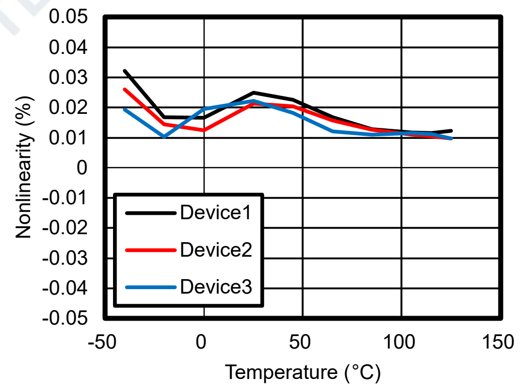


Figure 12. Nonlinearity vs. Temperature

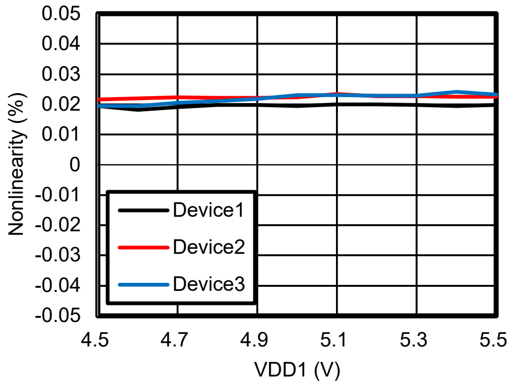


Figure 13. Nonlinearity vs. VDD1

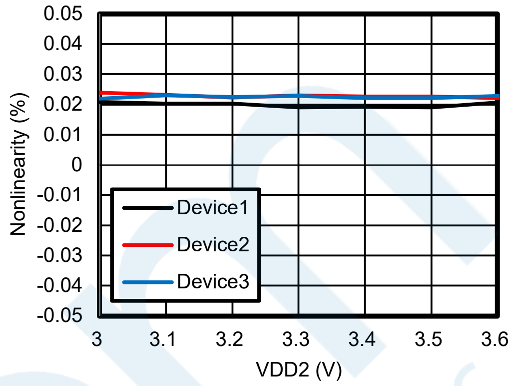


Figure 14. Nonlinearity vs. VDD2

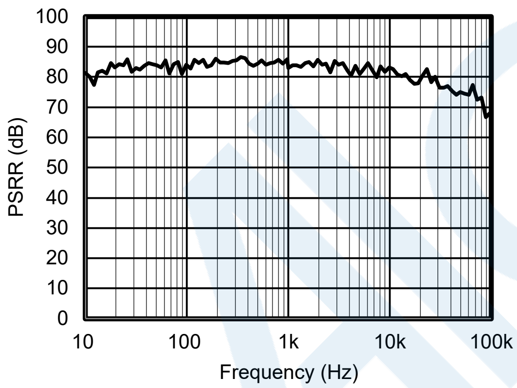


Figure 15. VDD1 PSRR vs. Frequency

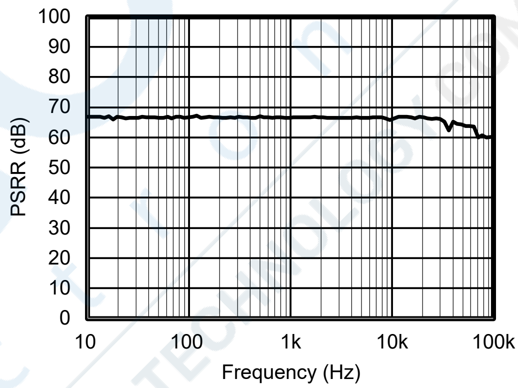


Figure 16. VDD2 PSRR vs. Frequency

Detailed Description

Overview

The device is a single-end input isolated amplifier with single-end output. The input stage of the device drives a delta-sigma (ΔΣ) modulator. The modulator utilizes an internal voltage reference source and clock generator to convert the analog input signal into a digital bit stream. A driver (referred to as TX in the functional block diagram) transmits the output of the modulator to the isolation barrier, which isolates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by an analog filter on the low side and presented as a single-end output of the device.

Based on the SiO_2-based, double-capacitive isolation barrier, the digital modulation and isolation barrier characteristics provide the device with high reliability and common-mode transient immunity.

Functional Block Diagram

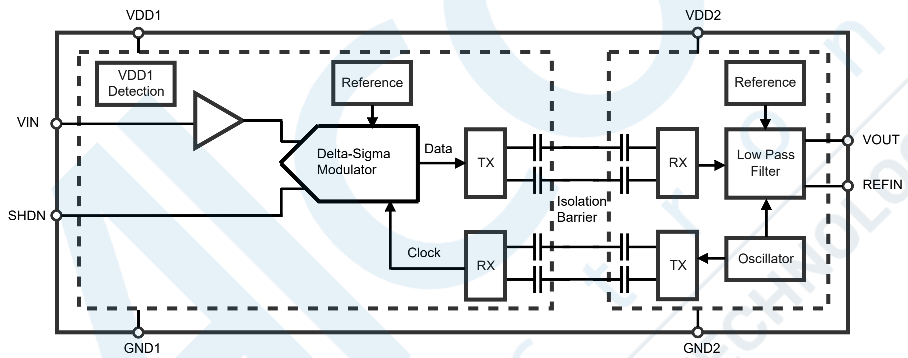


Figure 17. Functional Block Diagram

Feature Description

Single-End Output

The device provides a single-end output which can be fed into single-end input of the next stage.

Reference Input, REF

The output voltage of the device refers to the voltage at the REFIN pin. This function enables the shifting of common mode output voltage. Connecting the reference input (REF) to ground makes the output voltage equal to the input voltage. The output voltage of the device is equal to:

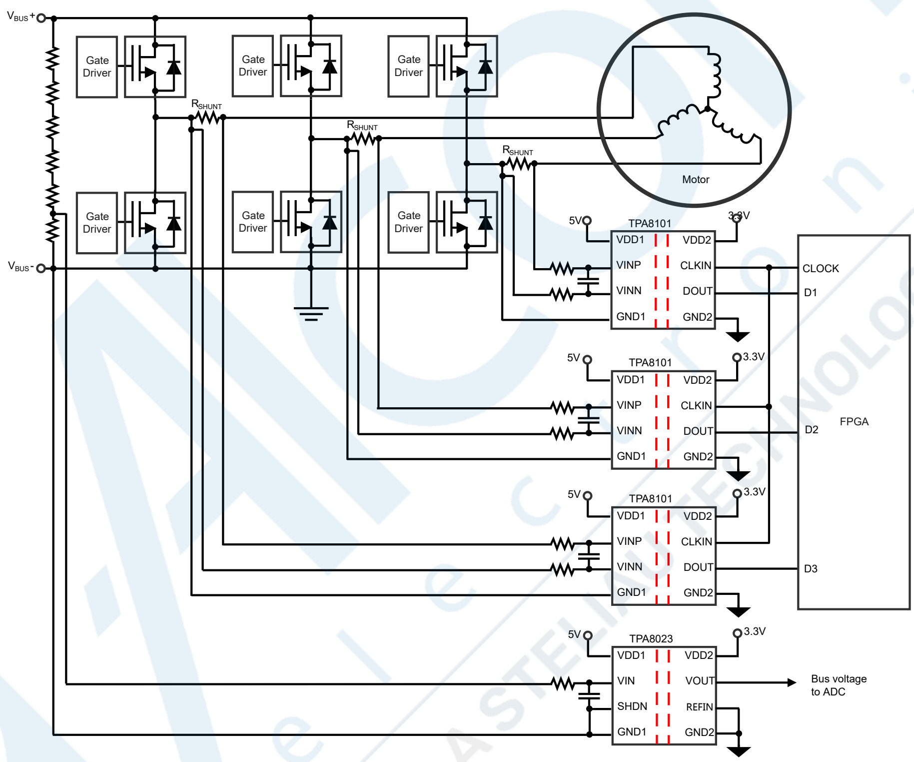
$$V_{OUT} = V_{IN} + V_{REFIN} \quad (1)$$

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application



Motor Drive Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, power supplies, and other industrial applications.

The TPA8101/8000/8001/8002 are optimized for current sensing applications with shunt resistors. The figure in the typical application section shows a typical operation of the TPA8101/8000/8001/8002 for current sensing in a motor drive application. Phase current is measured by the shunt resistors, R_{SHUNT}. The differential input and the high common-mode transient immunity of the TPA8101/8000/8001/8002 ensure reliable and accurate operation in high-noise environments.

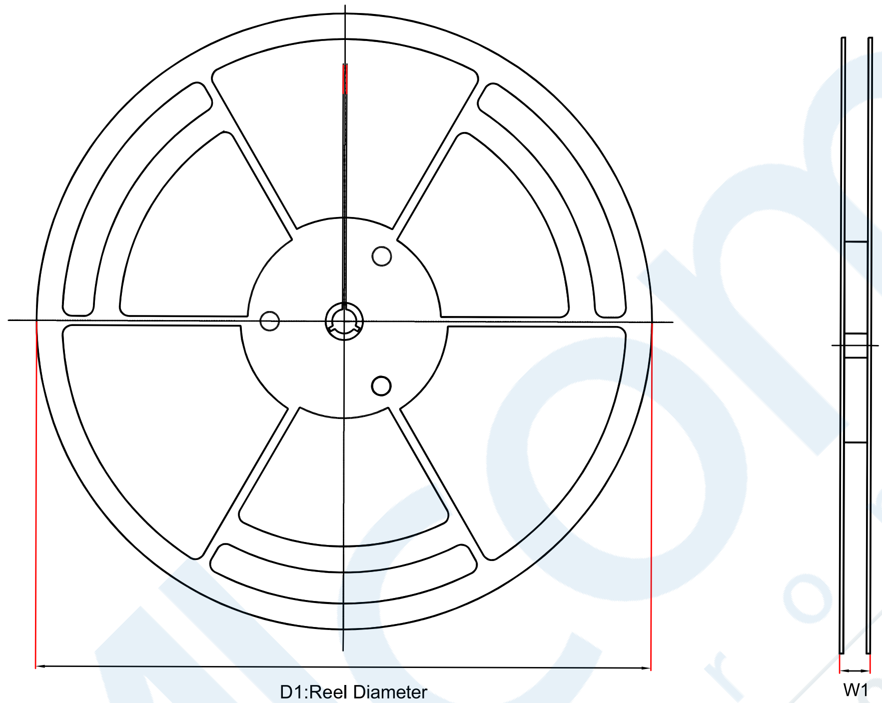
The DC bus voltage is measured by TPA8023 with high-impedance input and a wide input voltage range.

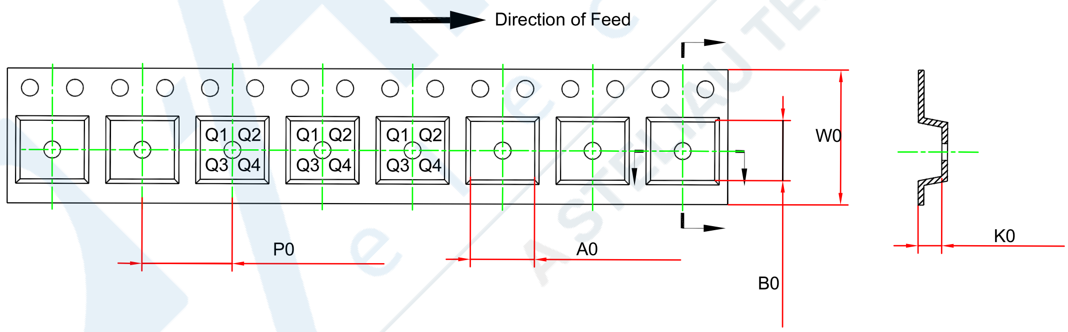
Power Supply Recommendation

In a typical frequency inverter application, the high-side power supply (VDD1) of the device is derived by the floating power supply of the upper gate driver. A Zener diode with a shunt resistor can be used to provide the high-side power supply of the device, or a low-cost low-dropout regulator (LDO) may be used to reduce the noise on the power supply. Place a 0.1-μF bypass capacitor as close as possible to the VDD1 pin of the device for best performance, an additional 1-μF to 10-μF capacitor may be used for better filtering.

To decouple the low-side power supply, place a 0.1-μF capacitor placed as close to the VDD2 pin of the device as possible, and an additional 1-μF to 10-μF capacitor may be used for better filtering.

Tape and Reel Information





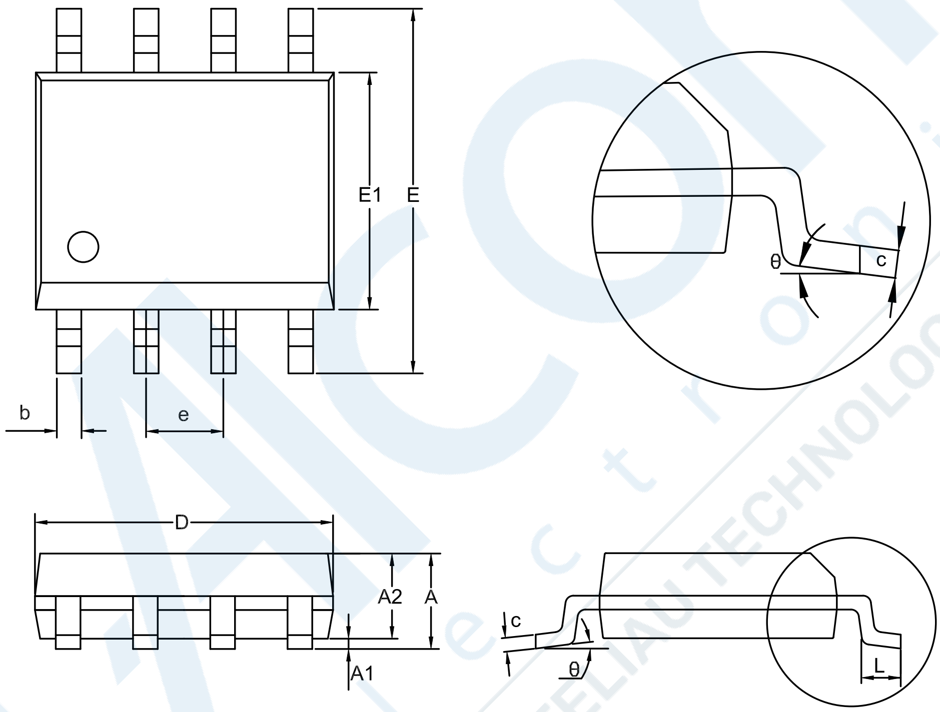
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA8023-SO1R	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TPA8023-SO1R-S	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TPA8023-SOAR	WSOP8	330.0	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8023-SOAR-S	WSOP8	330.0	21.6	11.95	6.2	3.1	16.0	16.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



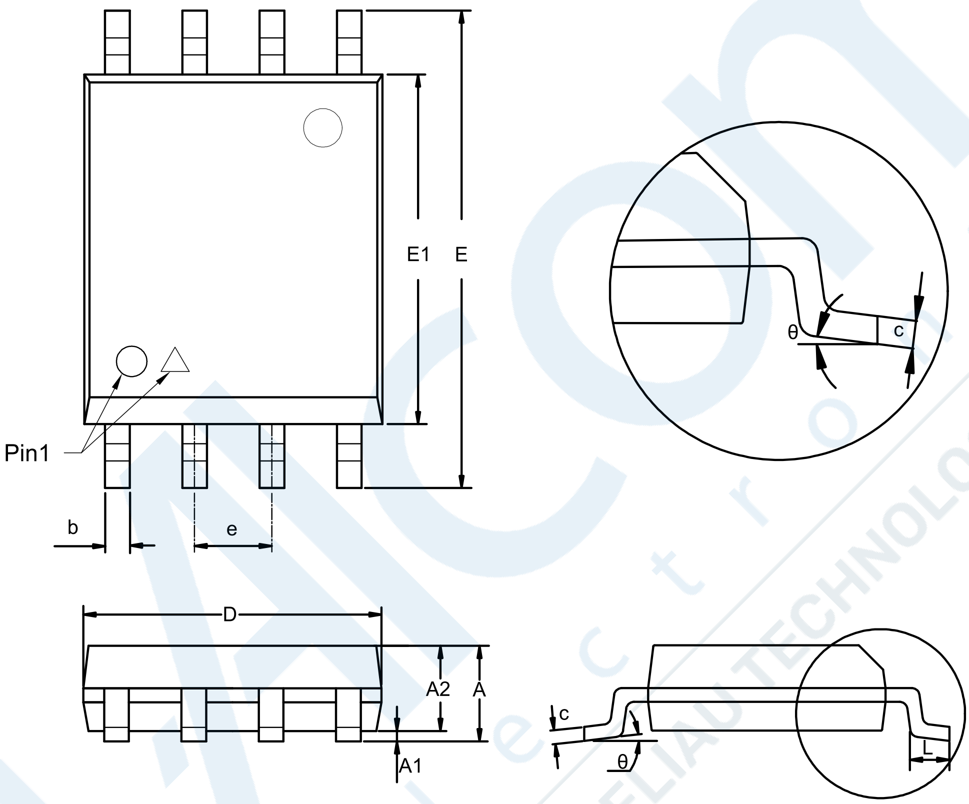
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

WSOP8

Package Outline Dimensions SOA(WSOP-8-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA8023-SO1R	−40 to 125°C	SOP8	A8023	MSL3	Tape and Reel, 4000	Green
TPA8023-SO1R-S (1)	−40 to 125°C	SOP8	A8023	MSL3	Tape and Reel, 4000	Green
TPA8023-SOAR	−40 to 125°C	WSOP8	A8023	MSL3	Tape and Reel, 1000	Green
TPA8023-SOAR-S (1) (2)	−40 to 125°C	WSOP8	A8023	MSL3	Tape and Reel, 1000	Green

(1) Passed AEC-Q100 Reliability Test.
(2) For future products, contact the 3PEAK factory for more information and samples.

Green: Defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

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