CA-IS3417WT 1700-V Output Off-State Voltage and Low EMI Reinforced Isolated HV Switch With Opto-Compatible Input

1 Key Features

- Normally Open (1-Form-A) Device
- Opto-Compatible Input
  - No Optical Attenuation and Aging Problems of Traditional Optocouplers
  - 5.5-V Maximum Input Reverse Voltage
- Integrate Back-to-Back SiC MOSFET
  - Output Off-State Voltage Up to 1700V (min)
  - 1-µA (max) Output Off-State Leakage Current
  - 50-Ω (typ) Output On-State Resistance
  - Output On-State Current Up to 50mA
  - Turn-On and Turn-Off Time < 300µs
- Wide Operating Temperature Range: –40°C to 125°C
- High CMTI: ±150kV/µs (typ)
- Low EMI: Passed Test According to CISPR32 Class B Standard With 2-Layer PCB Design
- Safety-Related Certifications (Pending):
  - 5-kV_{RMS} Isolation for 1 Minute per UL 1577
  - 7070-V_{PK} V_{IOTM} and 2121-V_{PK} V_{IORM} per DIN EN IEC 60747-17 (VDE 0884-17)
- 12-Pin Wide Body SOIC Package
  - Creepage and Clearance ≥ 8mm (Input-Output)
  - Creepage and Clearance ≥ 5.84mm (Across Output Terminals)

2 Applications

- Solid State Relay
- Battery Management System
- Energy Storage
- Solar System
- EV Charging Infrastructure

3 Description

The CA-IS3417WT is low-EMI, opto-compatible input, reinforced isolated HV (high-voltage) switch. The input stage (primary side) is an emulated diode (e-diode). While maintaining the input characteristics of the optocoupler, it also has better consistency, long-term stability and higher reliability. Unlike traditional optical MOS relays, this device's signal transmission characteristics will not attenuate over time. Also, compared with traditional mechanical relays, the CA-IS3417WT features long term reliability and excellent aging characteristics.

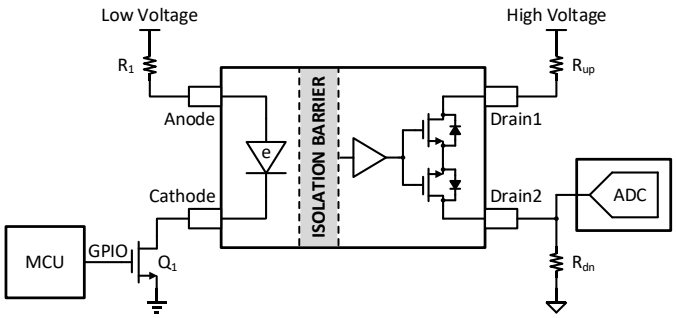
The output stage (secondary-side) of CA-IS3417WT integrates back-to-back SiC MOSFET with up to 1700-V standoff voltage. It can operate stably at higher ambient temperatures because of SiC MOSFET's better high-temperature characteristics and reliability.

The CA-IS3417WT devices are packaged in wide body, 12-pin SOIC packages and the pinout is compatible with most of industry standard optical MOS relays. The isolation voltage between primary-side and secondary-side is up to 5kV_{RMS} @ 1 minute. This device is specified over the extended industrial temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3417WT	SOIC12-WB (WT)	7.5mm × 10.3mm

Typical Application



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Output Off-State Voltage	Isolation Rating	Package
CA-IS3417WT	1700V	$5kV_{RMS}$	SOIC12-WB (WT)

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5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.05.22	NA

6 Pin Descriptions and Functions

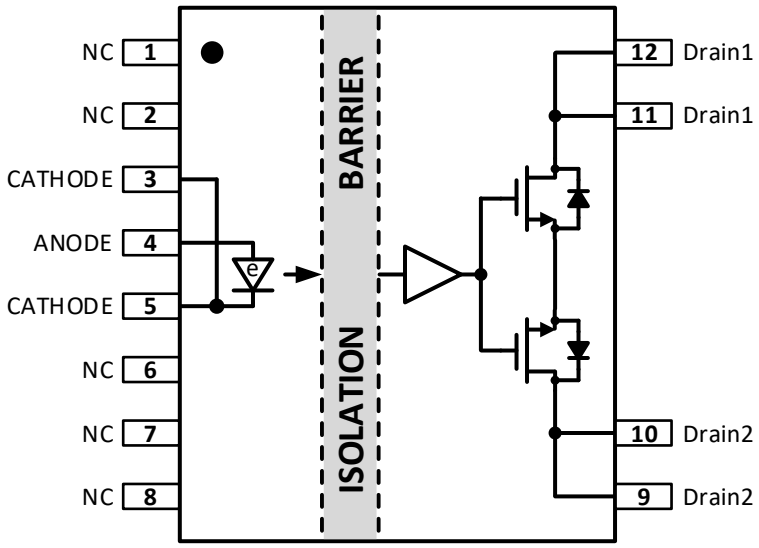


Figure 6-1 Pin Configuration

Table 6-1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
NC	1, 2, 6, 7, 8	--	No internal connection.
ANODE	4	Input	Anode of the emulator diode.
CATHODE	3, 5	Input	Cathode of the emulator diode.
Drain2	9, 10	Output	Switch output, MOSFET's second drain.
Drain1	11, 12	Output	Switch output, MOSFET's first drain.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
$I_{F(ON)}$	Input forward current (diode turns on)		50	mA
I_{TP}	Transient peak input current (100-µs pulse duration)		1	A
V_R	Input reverse voltage		6.5	V
P_I	Input maximum power dissipation		110	mW
I_{ON}	Output on-state current	–75	75	mA
I_{AV}	Output avalanche current[2] (T_A = 25°C)	–1	1	mA
P_O	Output maximum power dissipation		1	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. 5 minutes accumulated over lifetime with the period ≤ 1 minute, duty cycle ≤ 0.1%, guaranteed by bench characterization test.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Drain1 to Drain2	±3	kV
		All other pins	±8	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
$I_{F(ON)}$	Input forward current (diode turns on)	7	10	30	mA
$V_{F(OFF)}$	Input voltage across anode and cathode (diode turns off)	–5.5		0.9	V
I_{ON}	Output on-state current	–50		50	mA
V_{OFF}	Output off-state voltage	–1700		1700	V
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC		PACKAGE	UNIT
		SOIC12-WB (WT)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	°C/W

7.5 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	~ 2.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6 Safety-Related Certifications

VDE (Pending)	UL (Pending)
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10	Recognized under UL 1577 Component Recognition Program
Reinforced insulation	Single protection
Certification Number:	Certification Number:

7.7 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical specifications are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input to Output Characteristics						
V_F	Input forward voltage	I_F = 10mA	1.5	1.8	2.1	V
I_R	Input reverse current	V_R = 5.5V		0.01	1	μA
C_T	Input capacitance	V_F = 0.5V, f = 1MHz		5		pF
$\|V_{OFF}\|$	Output off-state voltage (across Drain1 and Drain2)	I_{OFF} = 10μA	1700			V
I_{OFF}	Output off-state leakage current	V_{OFF} = 1700V, T_A = 25°C		10	500	nA
		V_{OFF} = 1700V, T_A = 125°C		100	1000	
		V_{OFF} = 1700V, T_A = –40°C to 125°C			1000	
C_{OFF}	Output capacitance	V_F = 0.5V, f = 1MHz		5		pF
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 1000V	±100	±150		kV/μs
Coupled Electrical Characteristics						
I_{FT}	Turn-on current threshold			6	7	mA
I_{FC}	Turn-off current threshold		2	4		mA
R_{ON}	Output On-State Resistance	I_F = 10mA, I_{ON} = 10mA, T_A = 25°C		50	300	Ω
		I_F = 10mA, I_{ON} = 10mA, T_A = 125°C		50	300	
		I_F = 10mA, I_{ON} = 10mA, T_A = –40°C to 125°C			300	

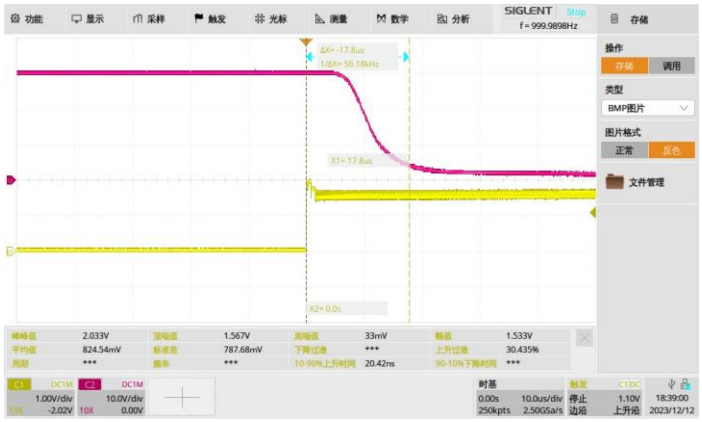
7.8 Timing Characteristics

Over recommended operating conditions (unless otherwise noted). All typical specifications are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Turn-on propagation delay	I_F = 10mA, R_L = 3kΩ, V_{DD} = 40V, see Figure 8-1 and Figure 8-2		10	100	μs
t_F	Fall time			10	100	
t_{ON}	Turn-on time (t_{ON} = t_{DHL} + t_F)			20	200	
t_{DLH}	Turn-off propagation delay			15	150	
t_R	Rise time			15	150	
t_{OFF}	Turn-off time (t_{OFF} = t_{DLH} + t_R)			30	300	

7.9 Typical Characteristics

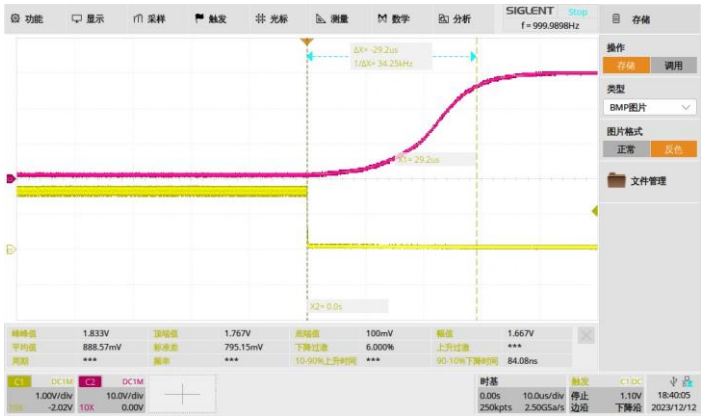
All typical specifications are at T_A = 25°C (unless otherwise noted).



Yellow: input voltage; Red: output voltage

Turn-on time: 17.8µs

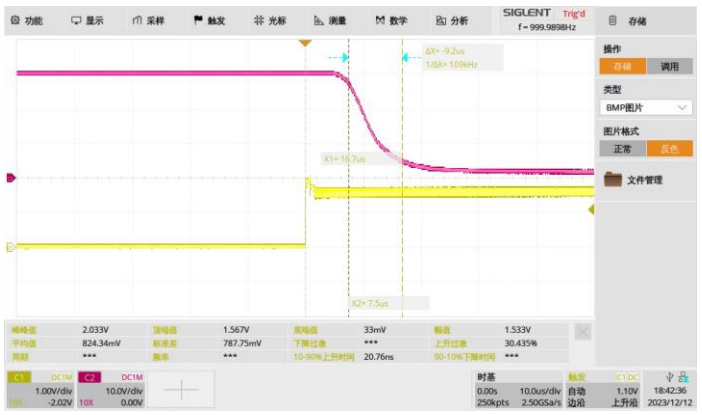
Figure 7-1 Turn-on Time Testing Waveforms



Yellow: input voltage; Red: output voltage

Turn-off time: 29.2µs

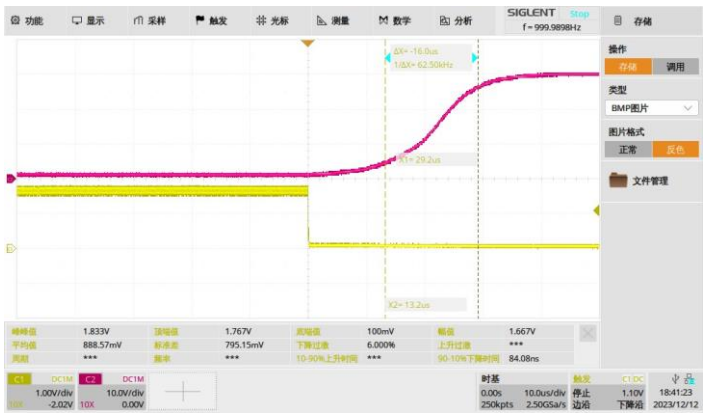
Figure 7-2 Turn-off Time Testing Waveforms



Yellow: input voltage; Red: output voltage

Fall time (90%-10%): 9.2µs

Figure 7-3 Fall Time Testing Waveforms



Yellow: input voltage; Red: output voltage

Rise time (10%-90%): 16µs

Figure 7-4 Rise Time Testing Waveforms

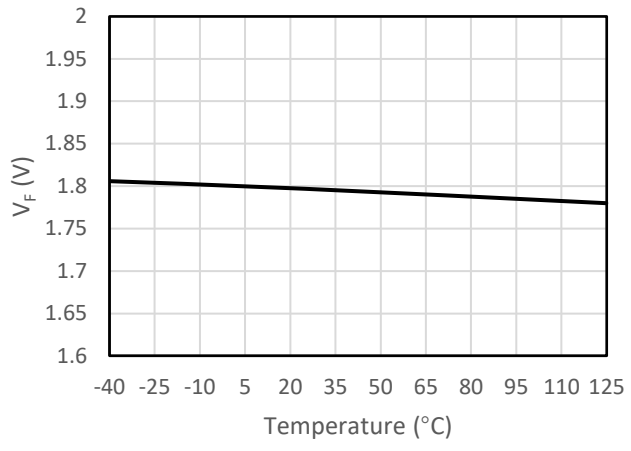


Figure 7-5 Input Forward Voltage vs Temperature

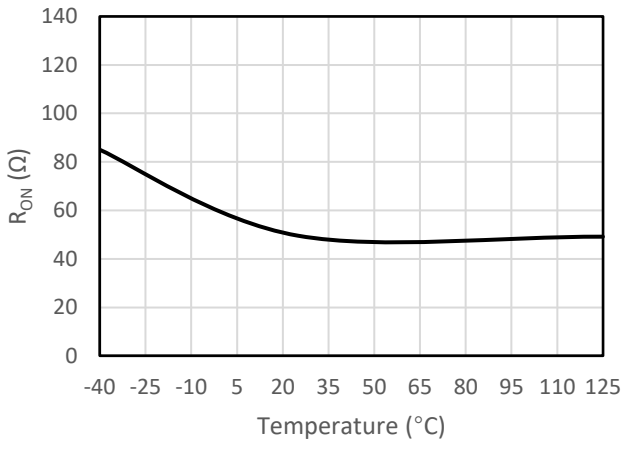


Figure 7-6 Output On-State Resistance vs Temperature

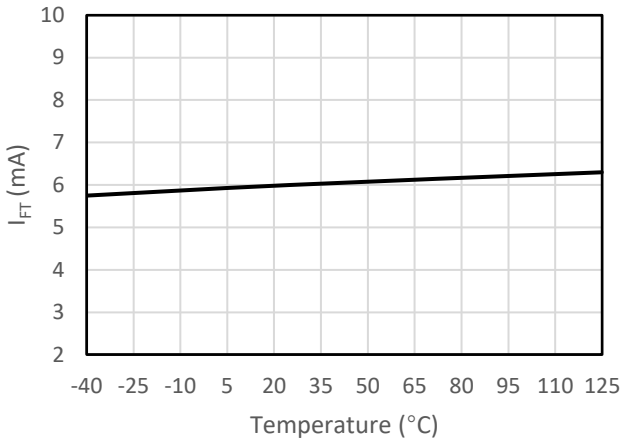


Figure 7-7 Turn-on Current Threshold vs Temperature

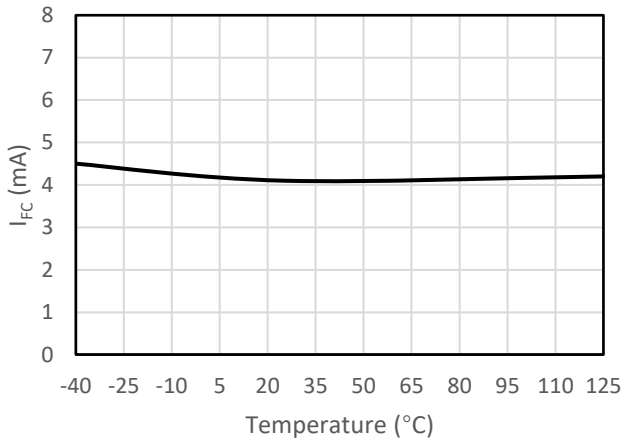


Figure 7-8 Turn-off Current Threshold vs Temperature

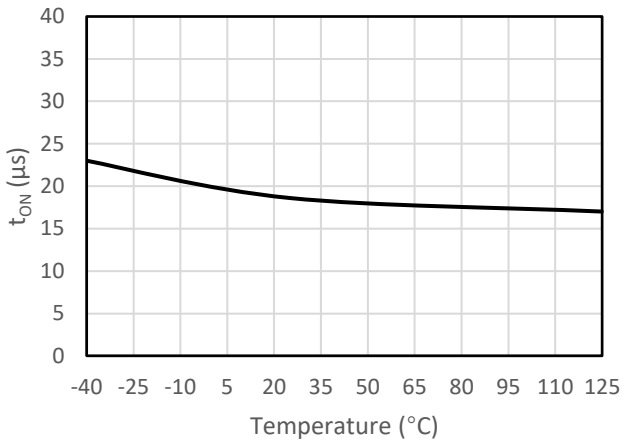


Figure 7-9 Turn-On Time vs Temperature

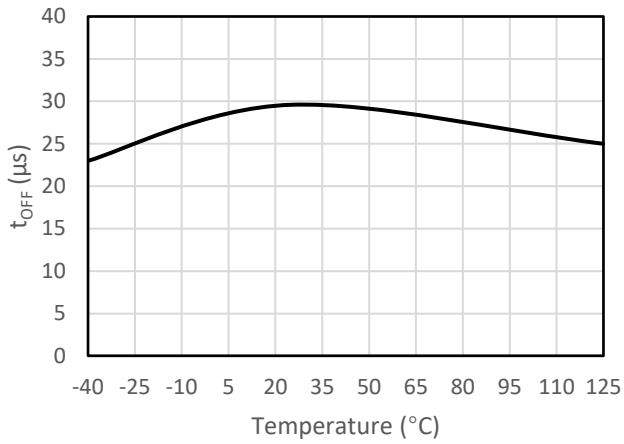


Figure 7-10 Turn-Off Time vs Temperature

8 Parameter Measurement Information

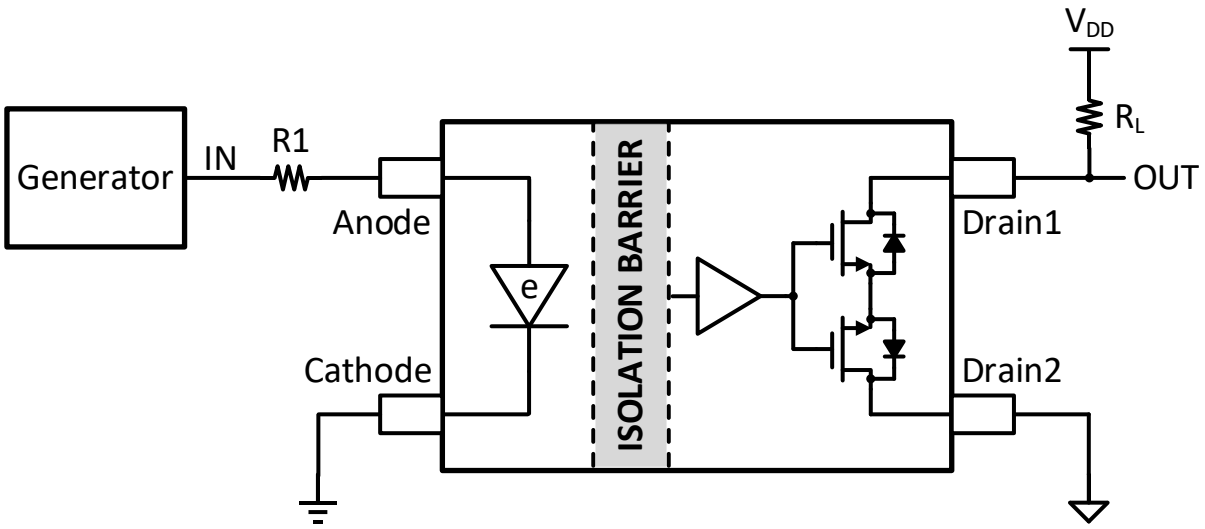


Figure 8-1 Timing Characteristics Testing Circuit

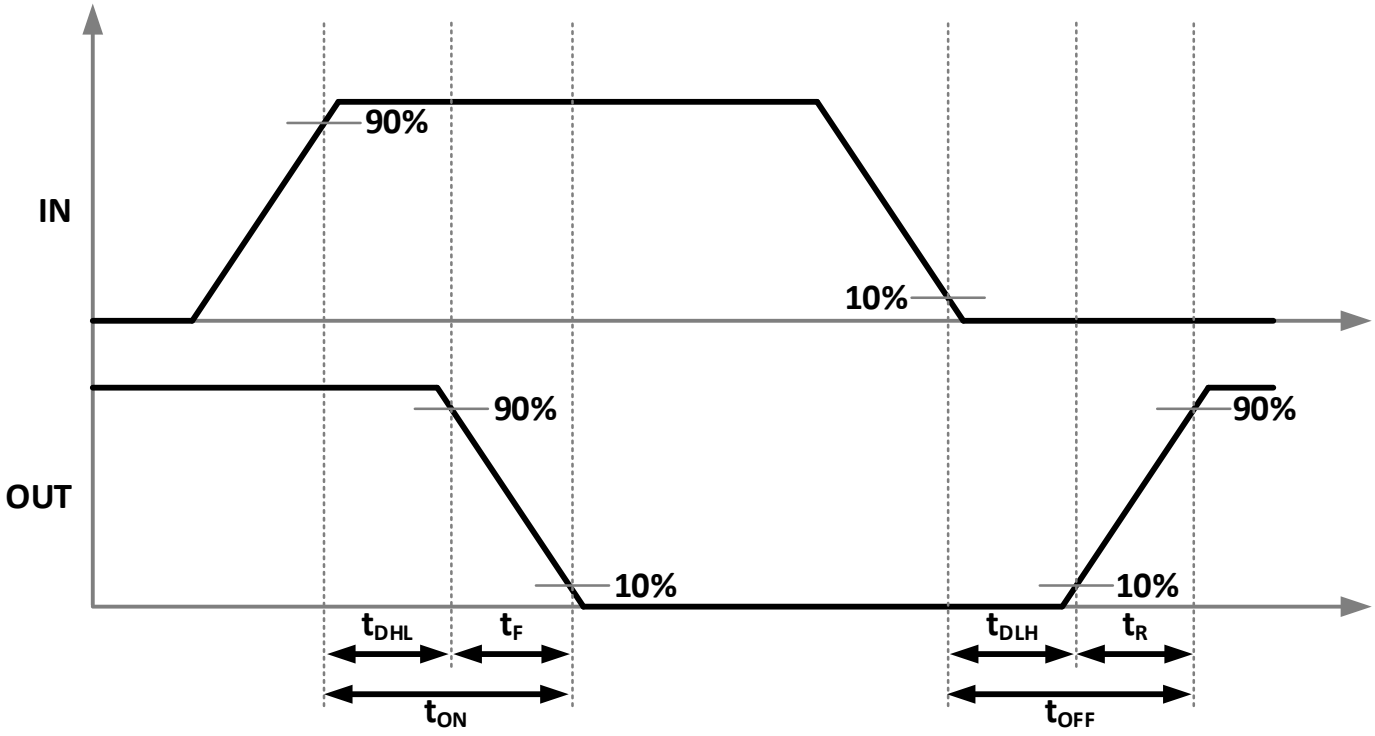


Figure 8-2 Timing Waveforms

9 Detailed Description

9.1 Overview

The CA-IS3417WT is low-EMI, opto-compatible input, reinforced isolated HV switch. The input stage (primary side) is an emulated diode (e-diode). While maintaining the input characteristics of the optocoupler, it also has better consistency, long-term stability and higher reliability. Unlike traditional optical MOS relays, this device's signal transmission characteristics will not attenuate over time. Also, compared with traditional mechanical relays, the CA-IS3417WT features long term reliability and excellent aging characteristics.

The output stage (secondary-side) of CA-IS3417WT integrates back-to-back SiC MOSFET with up to 1700-V standoff voltage. It can operate stably at higher ambient temperatures because of SiC MOSFET's better high-temperature characteristics and reliability.

When a positive voltage applies to the input of e-diode and the input forward current I_F exceeds the turn-on current threshold I_{FT}, circuit on primary side operates normally to transmit the high-level voltage across the isolation barrier by transmitter (TX); On the secondary side, the receiver (RX) demodulates this signal and converts it to the power supply and control signal required by the post driver stage, which finally turns on the back-to-back SiC MOSFET. If the input forward current I_F is smaller than the turn-off current threshold I_{FC}, the TX stops signal modulation and RX does not receive any power and signal, thus the output of post driver stage keeps low-level voltage and the back-to-back SiC MOSFET turns off. In conclusion, the secondary side of the CA-IS3417WT does not require additional power supply and this device only needs to apply an input forward current I_F exceeding a certain threshold on the primary side to turn on the output-stage switch. Also, the CA-IS3417WT is optimized in the signal modulation, demodulation and energy transmission to ensure that the two-layer PCB design can pass the EMI test according to the CISPR32 Class B standard.

The CA-IS3417WT devices are packaged in wide body, 12-pin SOIC packages and the pinout is compatible with most of industry standard optical MOS relays. The isolation voltage between primary-side and secondary-side is up to $5kV_{RMS}$ @ 1 minute. This device is specified over the extended industrial temperature range of –40°C to 125°C.

9.2 Device Function Mode

The truth table of CA-IS3417WT is shown in Table 9-1.

Table 9-1 Truth Table of Device

Input	Output State of Switch
$I_F > I_{FT}$	Turn On
$I_F < I_{FC}$	Turn Off
Input Floating	Turn Off

10 Application and Implementation

10.1 Application Overview

The CA-IS3417 is isolated HV switch with opto-compatible input and the typical application circuit is shown in Figure 10-1. The emulated diode (e-diode) on primary side features 1.8-V (typical value) forward voltage (V_F) which is close to the traditional optical isolated switch. The recommended input forward current I_F is 10mA (typical value). The recommended current-limiting resistor is 150Ω and 320Ω respectively when the power supply is 3.3V and 5V on primary side. Also, the GPIO (general purpose input and output) of a micro controller (MCU) could be used to control on and off of this device through an external MOSFET or bipolar transistor (Q1).

The output off-state voltage of CA-IS3417WT is up to 1700V, which is suitable for voltage sampling, insulation monitoring and fault diagnosis in the high-voltage battery system. When CA-IS3417WT is used in an 800-V battery system, a series resistor (Rup) with megaohm value is chosen following with several hundred microamps of on-state current and several tens of microwatts of on-state power consumption. A proper PCB layout is recommended to help dissipate heat from the device to the PCB and keep the junction temperature (T_J) under the absolute maximum rating.

To meet with the system requirements in isolation rating, it is recommended to leave enough clearance and creepage between the primary side and secondary side, and across Drain1 and Drain2. Also, any top layer PCB routing underneath the body of the package or between Drain1 and Drain2 should be avoided.

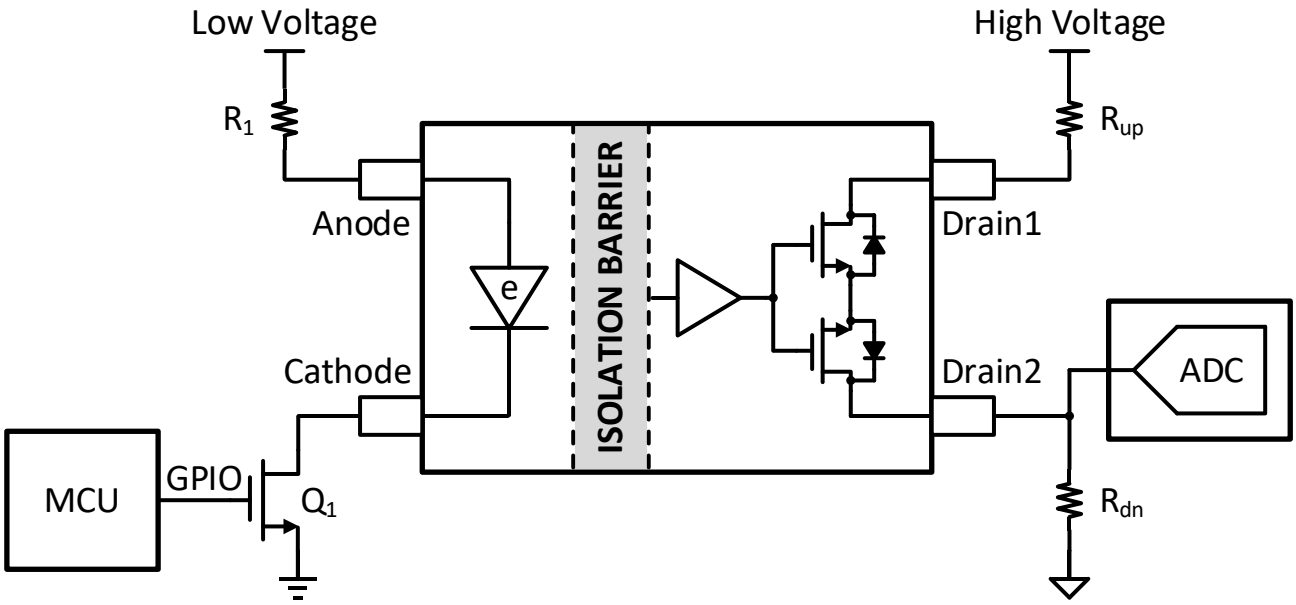


Figure 10-1 Typical Application Circuit

10.2 Insulation Resistance Monitoring Application

In automotive and industrial applications, the insulation resistance from each of the battery terminal to the chassis ground in high voltage battery pack should be monitored throughout its lifetime to check the integrity of insulation and then ensure the system safety.

There are two methods to measure the insulation resistance according to the different reference grounds of the sampling voltage: one is that the reference ground of the sampling ADC or MCU is at the same potential as the negative electrode of high-voltage battery (Battery V– Reference architecture); the other is that the reference ground of the sampling ADC or MCU is at the same potential as the chassis ground (Chassis Ground Reference architecture). The following sections describe these two different design architectures using the CA-IS3417WT isolated HV switch to monitor the insulation resistance of high voltage battery pack.

10.2.1 Battery V– Reference Architecture

If the reference ground of the sampling ADC or MCU is at the same potential as the battery V– reference, the measurement circuits are shown in Figure 10-2 and Figure 10-3 with the CA-IS3417WT simplified as SW1 and SW2. R_{ISOP} and R_{ISON} are the insulation resistance between battery V+ and chassis ground, battery V– and chassis ground respectively. Select R_1, R_{DIV1} and R_{DIV2} resistors in the voltage divider to scale the measured voltages down to the appropriate ADC measurement range. V_{PACK} is the battery voltage. Compared with the voltage dividing resistors, the on-resistance of CA-IS3417WT is very small and is ignored in the following calculations.

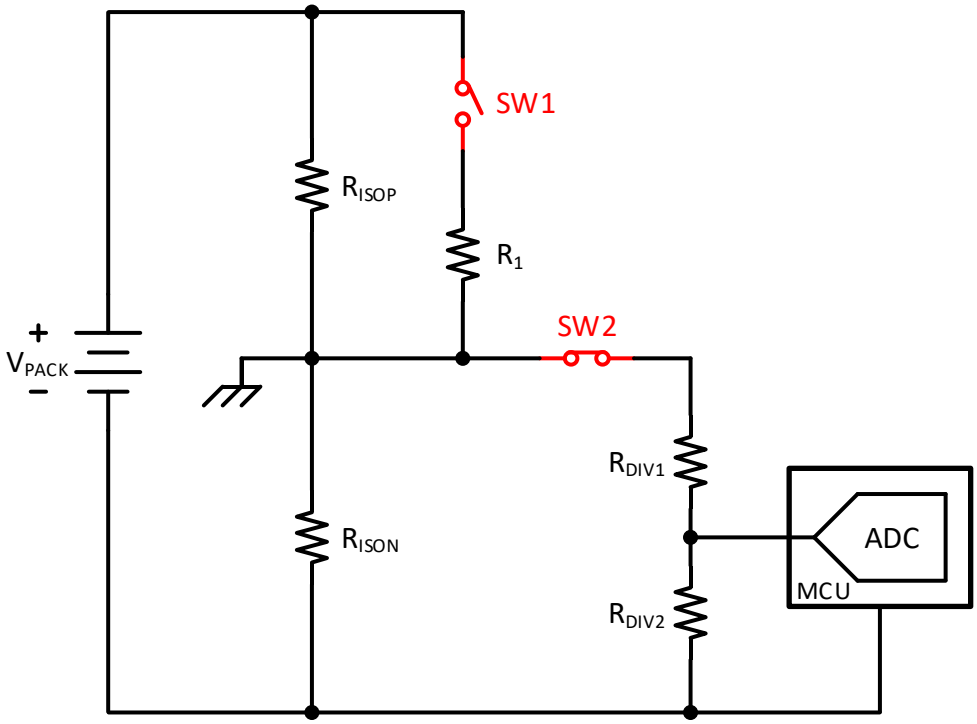


Figure 10-2 Insulation Resistance Monitoring Method 1 (SW1 Open, SW2 Closed)

To calculate the insulation resistance R_{ISOP} and R_{ISON}, two ADC measurements must be taken.

Step I: SW1 open and SW2 closed as shown in Figure 10-2.

The input voltage of ADC could be calculated according to the Equation 1.

$$V_{ADC1} = V_{PACK} \times \frac{R_{ISON} \,||\, (R_{DIV1} + R_{DIV2})}{R_{ISON} \,||\, (R_{DIV1} + R_{DIV2}) + R_{ISOP}} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad \textbf{(Equation 1)}$$

Step II: SW1 closed and SW2 open as shown in Figure 10-3.

The input voltage of ADC could be calculated according to the Equation 2.

$$V_{ADC2} = V_{PACK} \times \frac{R_{ISON} \,||\, (R_{DIV1} + R_{DIV2})}{R_{ISON} \,||\, (R_{DIV1} + R_{DIV2}) + R_{ISOP} \,||\, R_1} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad \textbf{(Equation 2)}$$

With above two measurement equations, R_{ISOP} and R_{ISON} could be calculated to check whether the system is under safe state.

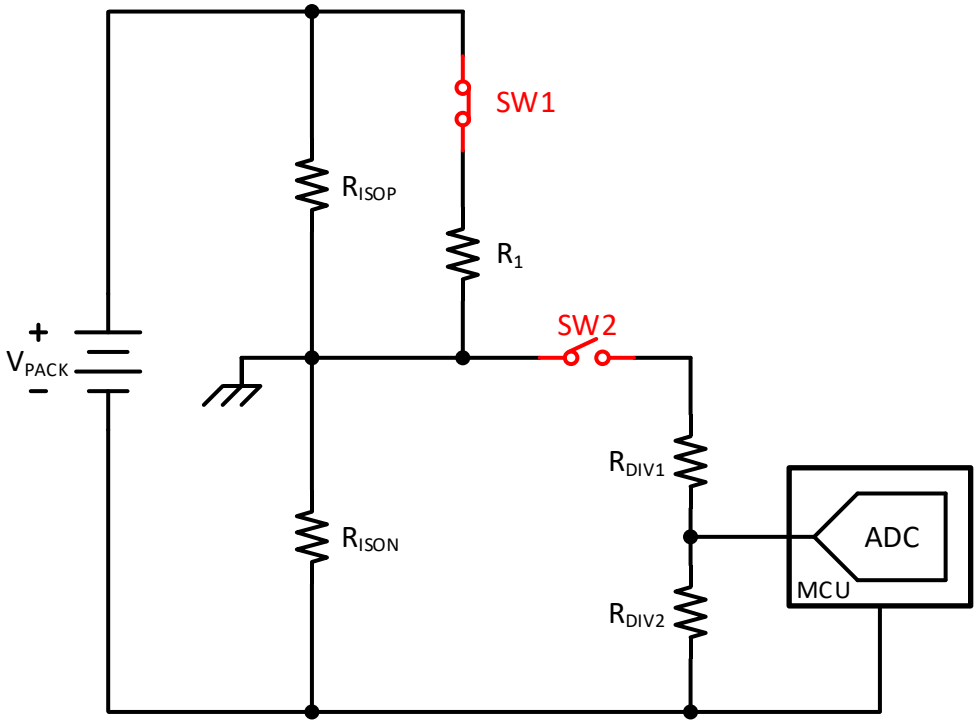


Figure 10-3 Insulation Resistance Monitoring Method 1 (SW1 Closed, SW2 Open)

10.2.2 Chassis Ground Reference Architecture

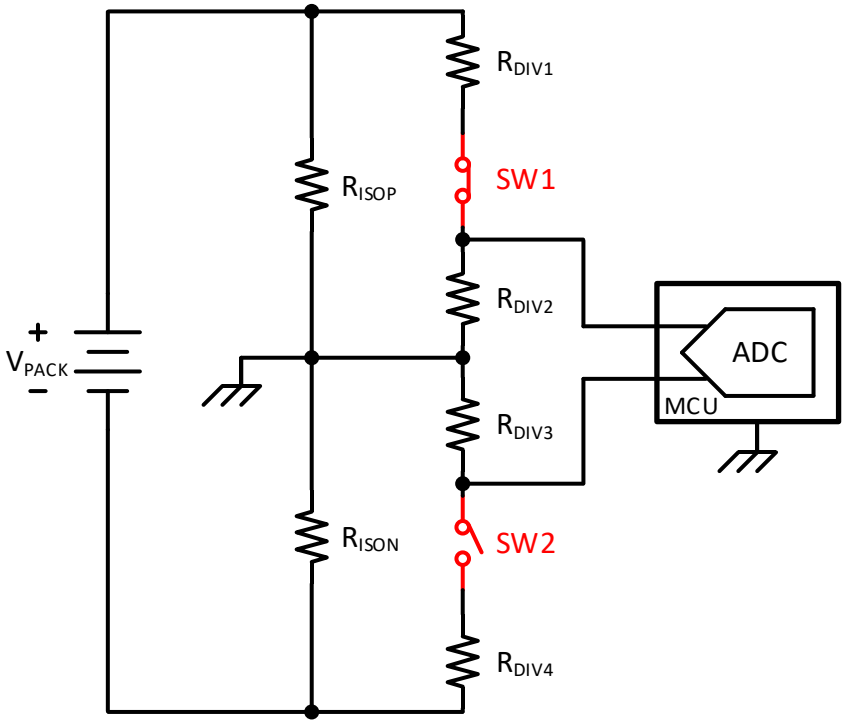


Figure 10-4 Insulation Resistance Monitoring Method 2 (SW1 Closed, SW2 Open)

If the reference ground of the sampling ADC or MCU is at the same potential as the chassis ground, the measurement circuits are shown in Figure 10-4 and Figure 10-5 with the CA-IS3417WT simplified as SW1 and SW2. R_{ISOP} and R_{ISON} are the insulation resistance between battery V+ and chassis ground, battery V– and chassis ground respectively. Select R_{DIV1}, R_{DIV2}, R_{DIV3} and R_{DIV4} resistors in the voltage divider to scale the measured voltages down to the appropriate ADC measurement range. V_{PACK} is the

battery voltage. Compared with the voltage dividing resistors, the on-resistance of CA-IS3417WT is very small and is ignored in the following calculations.

To calculate the insulation resistance R_{ISOP} and R_{ISON}, two ADC measurements must be taken.

Step I: SW1 closed and SW2 open as shown in Figure 10-4.

The input voltage of ADC could be calculated according to the Equation 3.

$$V_{ADC1} = V_{PACK} \times \frac{R_{ISOP} \,||\, (R_{DIV1} + R_{DIV2})}{R_{ISOP} \,||\, (R_{DIV1} + R_{DIV2}) + R_{ISON}} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad \textbf{(Equation 3)}$$

Step II: SW1 open and SW2 closed as shown in Figure 10-5.

The input voltage of ADC could be calculated according to the Equation 4.

$$V_{ADC2} = -V_{PACK} \times \frac{R_{ISON} \,||\, (R_{DIV3} + R_{DIV4})}{R_{ISON} \,||\, (R_{DIV3} + R_{DIV4}) + R_{ISOP}} \times \frac{R_{DIV3}}{R_{DIV3} + R_{DIV4}} \quad \textbf{(Equation 4)}$$

With above two measurement equations, R_{ISOP} and R_{ISON} could be calculated to check whether the system is under safe state.

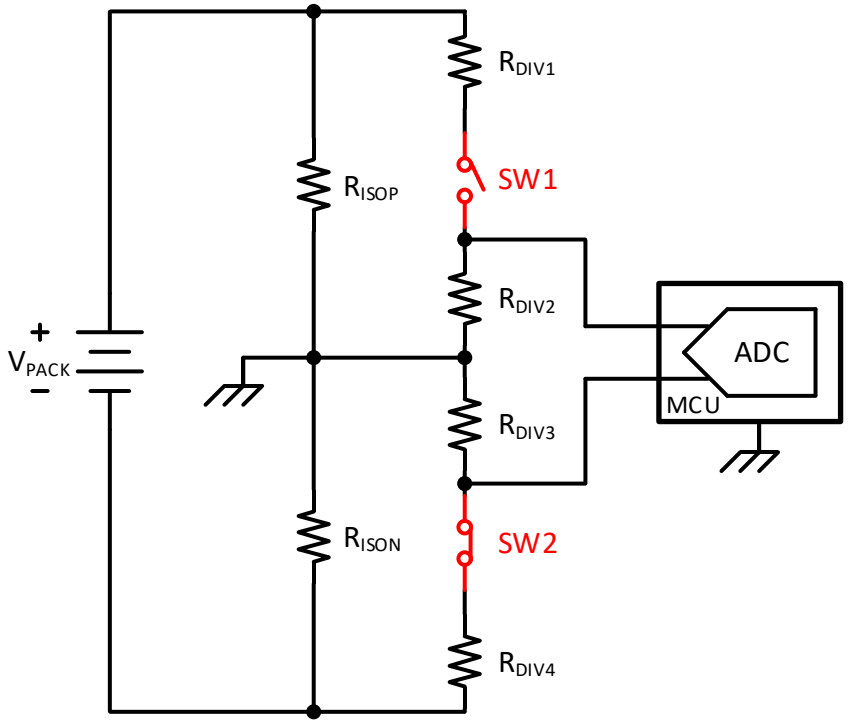
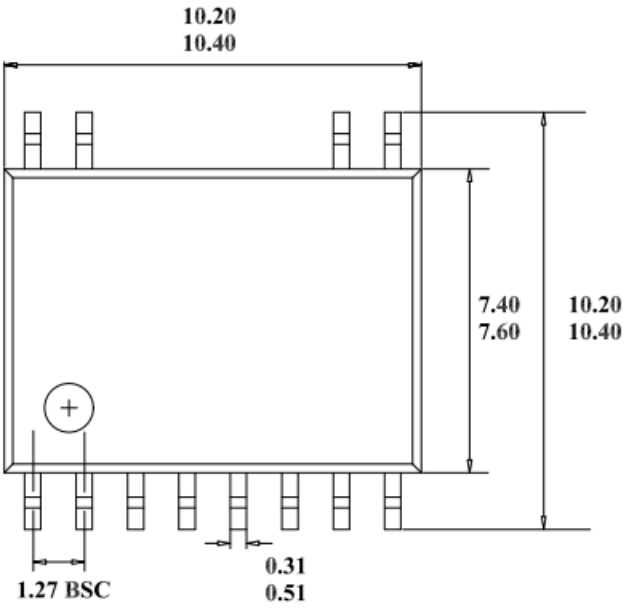


Figure 10-5 Insulation Resistance Monitoring Method 2 (SW1 Open, SW2 Closed)

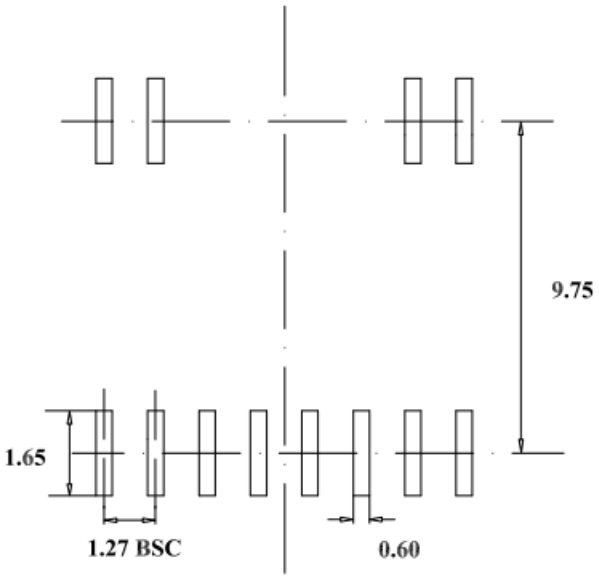
11 Package Information

11.1 SOIC12-WB Package

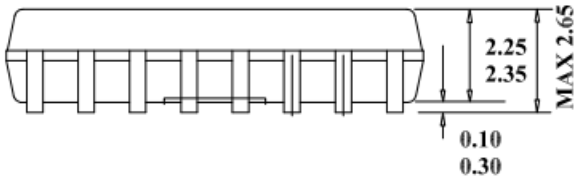
The values for the dimensions are shown in millimeters.



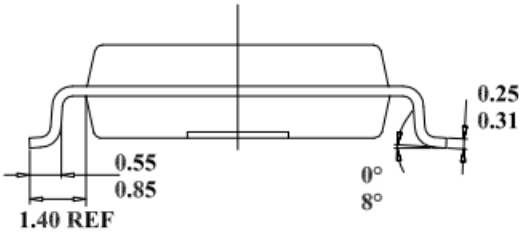
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

12 Soldering Information

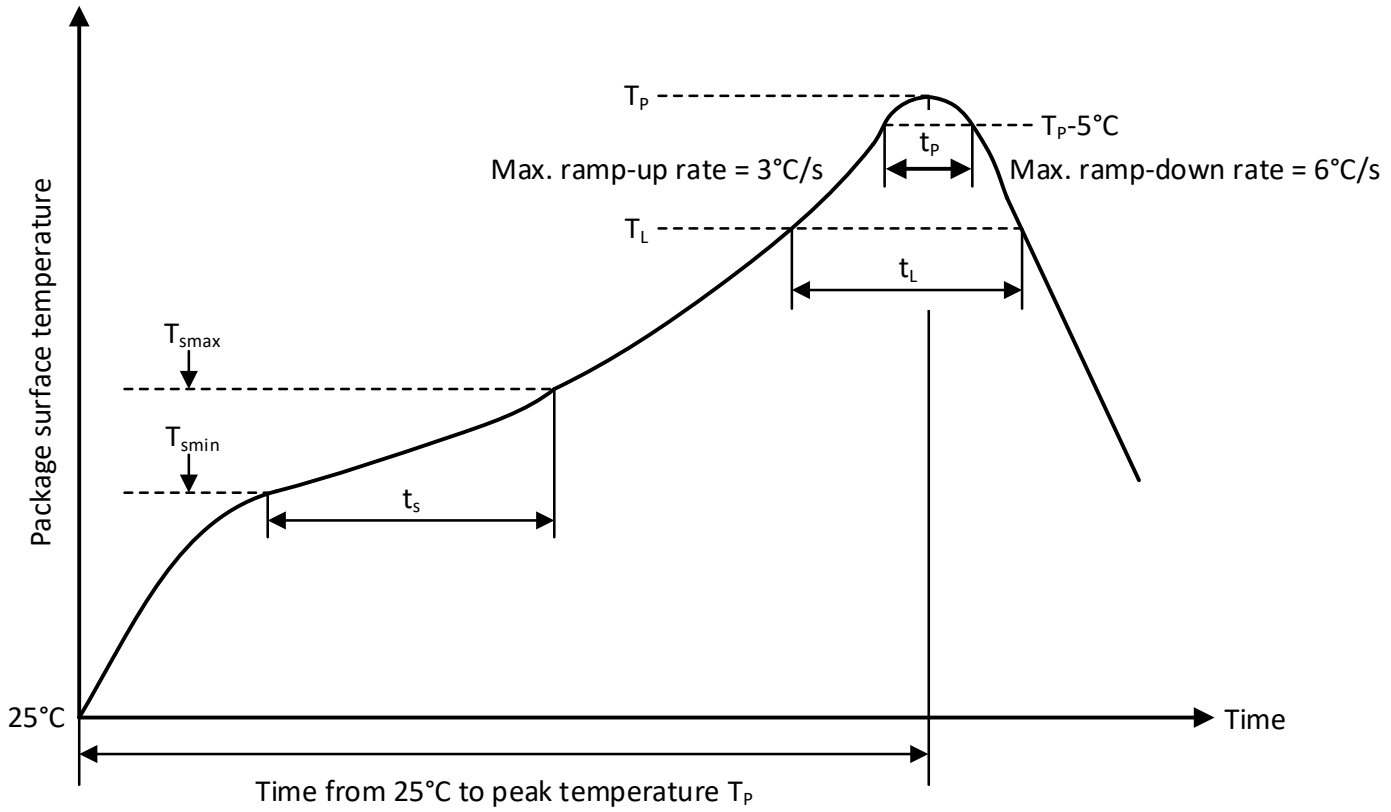


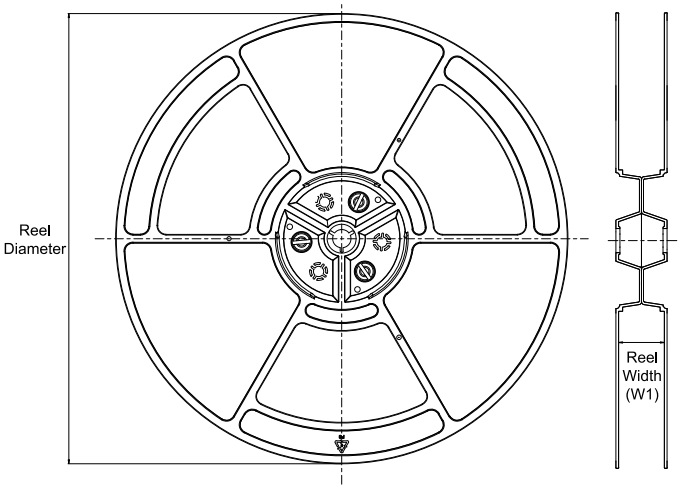
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

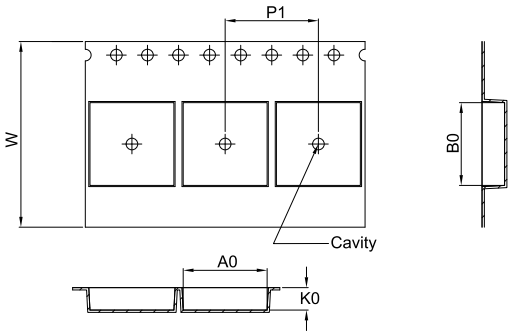
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

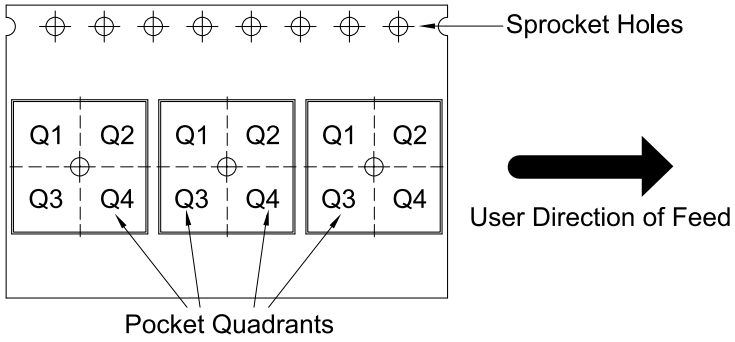


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3417WT	SOIC	WT	12	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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