CA-IS302x Low-Power Bidirectional I2C Isolators

1 Key Features

- **Bidirectional Data Transfer from DC to 2MHz**
- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: > 40 years
  - Withstands up to 3.75kV$_{RMS}$ (narrow-body package), 5kV$_{RMS}$ (wide-body packages) and 7.5kV$_{RMS}$ (super wide-body packages) isolation rating for 60s (V$_{ISO}$)
  - ±150 kV/µs typical CMTI
  - Schmitt trigger inputs for high noise immunity
  - High electromagnetic immunity and withstands ±12.8kV surge voltage
  - ±8kV Human Body Model ESD Protection
- **3.0V to 5.5V Wide Supply Operation**
- **Wide Operating Temperature Range: -40°C to 125°C**
- **RoHS-Compliant Packages**
  - Narrow-body SOIC8 (S) package
  - Wide-body SOIC8-WB (G) package
  - Wide-body SOIC16-WB (W) package
  - Super Wide-body SOIC8-WWB (WG) package
- **Open-drain Outputs**
  - 3.5mA Side A sink current capability
  - 35mA Side B sink current capability
- **Safety Regulatory Approvals**
  - VDE certification according to DIN EN IEC60747-17(VDE 0884-17):2021-10
  - UL certification according to UL 1577
  - CQC certification according to GB4943.1-2022

2 Applications

- I^{2}C, SMBus, PMBus™ Interfaces
- Motor control systems
- Medical Equipment
- Battery Management
- Instrumentation

3 Description

The CA-IS302x devices are complete dual-channel, galvanic digital isolators with up to 3.75kV$_{RMS}$ (narrow-body package)/5kV$_{RMS}$ (wide-body package)/7.5kV$_{RMS}$ (super wide-body package) isolation rating and ±150kV/µs typical CMTI. All device versions have Schmitt trigger inputs for high noise immunity and each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier to provide high electromagnetic immunity and low EMI. These devices feature high-integration design and only require fewer external components, V$_{DDA}$, V$_{DDB}$ bypass capacitors and pull-up resistors, to build an isolated I^{2}C interface.

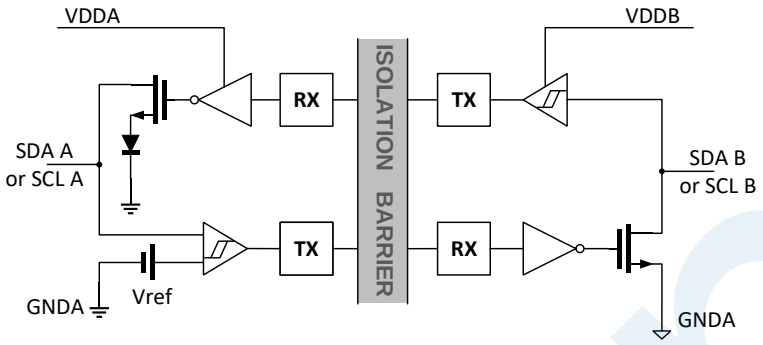
This family of devices operates from DC to 2MHz. The CA-IS3020 offers two bidirectional, open-drain channels for applications, such as multi-master I^{2}C, that require data and clock to be transmitted in both directions on the same line. The CA-IS3021 provides an isolated I^{2}C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). All devices feature independent 3.0V to 5.5V supplies on each side of the isolator and the logic levels are set independently on either side by V$_{DDA}$ and V$_{DDB}$. A simplified block diagram for a single CA-IS302x bidirectional channel is shown in the figure below.

The CA-IS302x series of devices are specified over -40°C to +125°C operating temperature range and are available in 8-pin SOIC narrow body package, 8-pin/16-pin SOIC wide body package and 8-pin SOIC super wide-body package. The wide temperature range and high isolation voltage make the devices ideal for use in harsh industrial environments.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3020 CA-IS3021	SOIC8(S)	4.90mm × 3.90mm
	SOIC8-WB(G)	5.85mm × 7.50mm
	SOIC16-WB(W)	10.30mm × 7.50mm
CA-IS3020	SOIC8-WWB(WG)	6.40mm × 14.00mm

CA-IS302x Functional Block Diagram



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	# of Bidirectional Channels	# of Unidirectional Channels	Rated Voltage (V_{RMS})	Default Output	Package
CA-IS3020S	2	0	3.75	Open drain	SOIC8 (S)
CA-IS3020G	2	0	5.0	Open drain	SOIC8-WB (G)
CA-IS3020W	2	0	5.0	Open drain	SOIC16-WB (W)
CA-IS3020WG	2	0	7.5	Open drain	SOIC8-WWB (WG)
CA-IS3021S	1	1	3.75	Open drain	SOIC8 (S)
CA-IS3021G	1	1	5.0	Open drain	SOIC8-WB (G)
CA-IS3021W	1	1	5.0	Open drain	SOIC16-WB (W)

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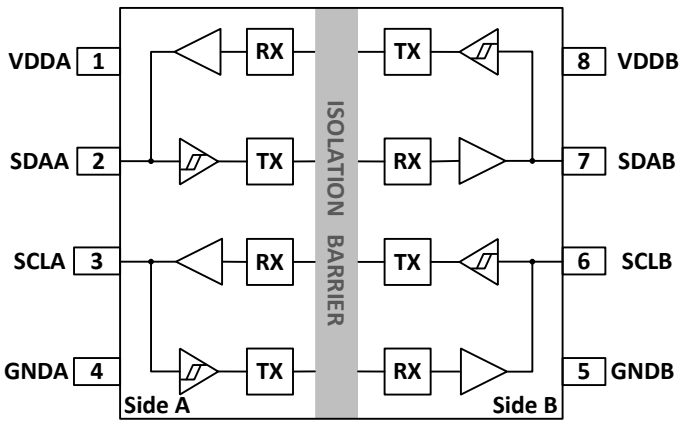
5 Revision History

Revision Number	Description	Revision Date	Page Changed
Version 1.00	N/A	--	N/A
Version 1.01	Change POD and tape information	2023/02/09	18, 19, 20, 22
Version 1.02	Update VDE information	2023/09/13	8, 9
Version 1.03	Update VDE, UL, CQC information Update the test conditions of V_{IOSM}	2024/04/13	1, 8, 9
Version 1.04	Add part number for SOIC8-WWB package: CA-IS3020WG	2024/07/02	1, 2, 4, 7, 8, 9, 14, 21, 23
	Update VDE information		8, 9
	Update recommended land patterns for SOIC8, SOIC8-WB and SOIC16-WB		17, 18, 19
	Update recommended operation conditions for V_{ILA}, V_{ILB} and V_{IHB}		6

6 Pin Descriptions and Functions

CA-IS3020 SOIC8 / SOIC8-WB / SOIC8-WWB Top View



CA-IS3021 SOIC8 / SOIC8-WB Top View

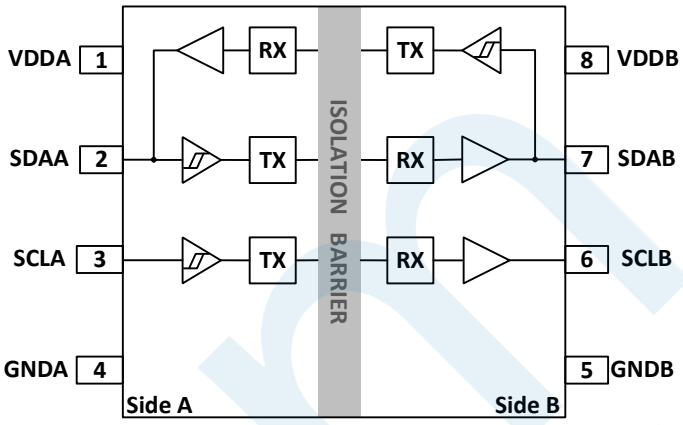


Figure 6-1 CA-IS3020/CA-IS3021 SOIC-8, SOIC8-WB and SOIC8-WWB Top View

Table 6-1 CA-IS3020S/CA-IS3020G/CA-IS3020WG Pin Description

Pin Name	Pin Number	Type	Description
VDDA	1	Power	Power supply for side A.
SDAA	2	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	3	Digital I/O	Bidirectional clock input/output on side A. SCLA is translated to/from SCLB and is an open-drain output.
GNDA	4	Ground	Ground reference for side A.
GNDB	5	Ground	Ground reference for side B.
SCLB	6	Digital I/O	Bidirectional clock input/output on side B. SCLB is translated to/from SCLA and is an open-drain output.
SDAB	7	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	8	Power	Power supply for side B.

Table 6-2 CA-IS3021S/CA-IS3021G Pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power	Power supply for side A.
SDAA	2	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	3	Digital Input	Clock input on side A. SCLA is translated to SCLB.
GNDA	4	Ground	Ground reference for side A.
GNDB	5	Ground	Ground reference for side B.
SCLB	6	Digital Output	Clock output on side B. SCLB is translated from SCLA and is an open-drain output.
SDAB	7	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	8	Power	Power supply for side B.

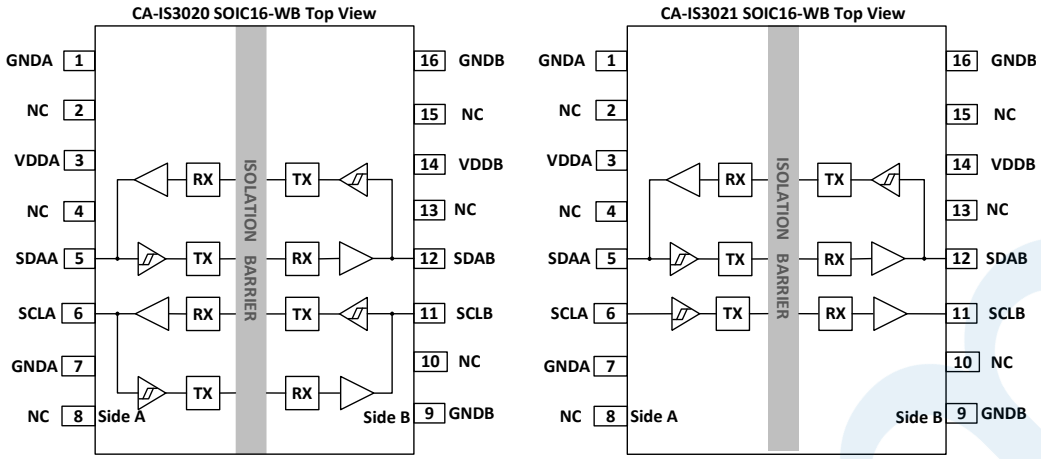


Figure 6-2 CA-IS3020/CA-IS3021 SOIC16-WB Top View

Table 6-3 CA-IS3020W Pin Description

Pin name	Pin number	Type	Description
GNDA	1, 7	Ground	Ground reference for side A.
NC	2, 4, 8	--	No connect. Do not connect these pins externally.
VDDA	3	Power	Power supply for side A.
SDAA	5	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	6	Digital I/O	Bidirectional clock input/output on side A. SCLA is translated to/from SCLB and is an open-drain output.
GNDB	9, 16	Ground	Ground reference for side B.
NC	10, 13, 15	--	No connect. Do not connect these pins externally.
SCLB	11	Digital I/O	Bidirectional clock input/output on side B. SCLB is translated to/from SCLA and is an open-drain output.
SDAB	12	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	14	Power	Power supply for side B.

Table 6-4 CA-IS3021W Pin Description

Pin name	Pin number	Type	Description
GNDA	1, 7	Ground	Ground reference for side A.
NC	2, 4, 8	--	No connect. Do not connect these pins externally.
VDDA	3	Power	Power supply for side A.
SDAA	5	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	6	Digital Input	Clock input on side A. SCLA is translated to SCLB.
GNDB	9, 16	Ground	Ground reference for side B.
NC	10, 13, 15	--	No connect. Do not connect these pins externally.
SCLB	11	Digital Output	Clock output on side B. SCLB is translated from SCLA and is an open-drain output.
SDAB	12	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	14	Power	Power supply for side B.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Power supply voltage[2]	-0.5	6.0	V
SDAA, SCLA	Input/Output voltage	-0.5	V_{DDA} + 0.5[3]	V
SDAB, SCLB	Input/Output voltage	-0.5	V_{DDB} + 0.5[3]	V
I_{OA}	Output Current	-20	20	mA
I_{OB}	Output Current	-100	100	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. The maximum voltage must not exceed 6V.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±8000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	V

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Power supply voltage	3.0	5.5	V
V_{SDDA}, V_{VSCLA}	A side input voltage	0	V_{DDA}	V
V_{SDDB}, V_{VSCLB}	B side input voltage	0	V_{DDB}	V
V_{ILA}	A side Input low voltage	0	0.47	V
V_{IHA}	A side Input high voltage	0.7 x V_{DDA}	V_{DDA}	V
V_{ILB}	B side Input low voltage	0	0.8	V
V_{IHB}	B side Input high voltage	2	V_{DDB}	V
I_{OLA}	A side Output current (low level)	0.5	3.5	mA
I_{OLB}	B side Output current (low level)	0.5	35	mA
C_A	Maximum load capacitance on A side		40	pF
C_B	Maximum load capacitance on B side		400	pF
f_{MAX}[1]	Maximum Frequency		2	MHz
T_A	Environmental temperature	-40	125	°C
T_J	Junction temperature	-40	150	°C

Note:

1. This maximum signal transmission rate is the maximum signal frequency at the maximum bus capacitance load and the maximum pull-down current. If the capacitance load is smaller, a higher signal transmission rate is possible.

7.4 Thermal Information

THERMAL METRIC		CA-IS302x				UNIT
		SOIC8 (S)	SOIC8-WB (G)	SOIC16-WB (W)	SOIC8-WWB (WG)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.0	92.3	86.5	68.3	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
P_D	Maximum power dissipation (both sides)	V_{DDA} = V_{DDB} = 5.5V, T_J = 150°C, C_A = 40pF, C_B = 400pF; Input a 1-MHz 50% duty cycle clock signal			86	mW
P_{DA}	Maximum power dissipation (side-A)				34	mW
P_{DB}	Maximum power dissipation (side-B)				52	mW

7.6 Insulation Specifications

Parameters		Test conditions	Value				Unit
			S	G	W	WG	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	4	8	8	15	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	4	8	8	15	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	28	28	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	>600	>600	>600	>600	V
	Material group	In accordance with IEC 60664-1	I	I	I	I	
IEC 60664-1 over-voltage category		Rated mains voltage ≤ 150V_{RMS}	I-IV	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-IV	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	N/A	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	N/A	I-III	I-III	I-IV	
DIN V VDE V 0884-17:2021-10[2]							
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	1414	1414	2828	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	1000	1000	2000	V_{RMS}
		DC voltage	566	1414	1414	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	5300	7070	7070	10600	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-μs waveform per IEC 62368-1	5000	9846	9846	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	6500	12800	12800	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety test of the sub-category 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	≤5	≤5	≤5	pC
		Method a, after environmental test of the sub-category 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	≤5	≤5	≤5	
		Method b1, routine test (100% production test) and preprocessing (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (certified, G/W/WG) $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s (certified, S)	≤5	≤5	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1MHz	~0.5	~0.5	~0.5	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	$>10^{9}$	$>10^{9}$	
	Contaminant level		2	2	2	2	
UL 1577							
V_{ISO}	Maximum solation voltage	$V_{TEST} = V_{ISO}$, t = 60s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3750	5000	5000	7500	V_{RMS}

Notes:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the

printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN EN IEC60747-17(VDE 0884-17):2021-10; EN IEC60747- 17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022
Basic Isolation (SOIC8): VIORM: 566V_{PK} VIOTM: 5300V_{PK} VIOSM: 6500V_{PK} Reinforced Isolation (SOIC8-WB / SOIC16-WB): VIORM: 1414V_{PK} VIOTM: 7070V_{PK} VIOSM: 12800V_{PK} Reinforced Isolation (SOIC8-WWB): Pending VIORM: 2828V_{PK} VIOTM: 10600V_{PK} VIOSM: 12800V_{PK}	SOIC8: 3750V_{RMS} SOIC8-WB: 5000V_{RMS} SOIC16-WB: 5000V_{RMS} SOIC8-WWB: 7500V_{RMS} (Pending)	SOIC8-WB / SOIC16-WB: Reinforced insulation (Altitude ≤ 5000m)
Reinforced insulation Certificate number: 40057278 Basic insulation Certificate number: 40052786	Certificate number: E511334	Certificate number: SOIC8-WB: CQC24001434134 SOIC16-WB: CQC23001406424

7.8 Electrical Characteristics

Over recommended operating conditions, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Side A						
V_{ILTA}	Logic low input threshold (SDAA and SCLA)		470	500	520	mV
V_{IHTA}	Logic high input threshold (SDAA and SCLA)		500	560	620	mV
V_{HYSA}	Voltage input hysteresis	V_{IHTA} -V_{ILTA}	40	60	80	mV
V_{OLA}	Logic low output voltage (SDAA and SCLA) [1]	0.5mA ≤ (I_{SDAA} and I_{SCLA}) ≤ 3.5mA	630	700	760	mV
ΔV_{OITA}	Logic-low output voltage to logic-high input voltage threshold difference (SDAA and SCLA)[1, 2]	0.5mA ≤ (I_{SDAA} and I_{SCLA}) ≤ 3.5mA	100			mV
Side B						
V_{ILTB}	Logic low input threshold (SDAB and SCLB)		1.13	1.33	1.53	V
V_{IHTB}	Logic low output voltage (SDAB and SCLB)		1.55	1.75	1.97	V
V_{HYSB}	Voltage input hysteresis	V_{IHTB} -V_{ILTB}	0.30	0.42	0.54	V
V_{OLB}	Logic-low output voltage (SDAB and SCLB)	0.5mA ≤ (I_{SDAB} and I_{SCLB}) ≤ 35mA			0.4	V
Both Sides						
$\|I_L\|$	Input leakage currents, SDAA, SCLA, SDAA, and SCLA	V_{SDAA} = V_{SCLA} = VDDA V_{SDAB} = V_{SCLB} = VDDB			1	µA
C_I	Input capacitance to local ground (SDA1, SCL1, SDA2, and SCL2)			3		pF
CMTI	Common mode transient immunity	See Figure 8-3	±100	±150		kV/µs
V_{DDUV}	VDD_ Undervoltage-lockout threshold[3]		1.95	2.24	2.53	V

Notes:

1. This parameter applies to the CA-IS3020 (SDAA, SCLA) and CA-IS3021 SDAA bidirectional lines only.
2. ΔV_{OITA} = V_{OLA} – V_{IHTA}. This is the minimum difference between logic-low output voltage and a logic-high input voltage.
3. Any $V_{DD\_}$ voltage on both sides, less than the minimum will ensure device lockout. $V_{DD\_}$ voltage on both side A and side B greater than the maximum will prevent device lockout.

7.9 Supply Current Characteristics

Over recommended operating conditions, unless otherwise specified, see Figure 8-1 for more information.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
3V ≤ V_{DDA}, V_{DDB} ≤ 3.6V						
CA-IS3020	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		4.9	5.7	mA
		I_{DDB}		4.7	5.2	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.4	2.8	
		I_{DDB}		2.2	2.6	
CA-IS3021	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.9	4.4	
		I_{DDB}		2.4	3.7	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		1.7	2.6	
		I_{DDB}		1.8	2.8	
4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V						
CA-IS3020	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		5.0	5.7	mA
		I_{DDB}		4.7	5.2	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.4	2.8	
		I_{DDB}		2.2	2.6	
CA-IS3021	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		3.0	4.5	
		I_{DDB}		2.5	3.8	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		1.8	2.7	
		I_{DDB}		1.9	2.9	

7.10 Timing Requirements

PARAMETER		MIN	TYP	MAX	UNIT
t_{SP}	Input noise filter	10	25		ns

7.11 Timing Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3V ≤ (V_{DDA}, V_{DDB}) ≤ 3.6V							
t_{fA}	Fall Time (SDAA, SCLA)	See Figure 8-1 R1 = 953Ω C1 = 40pF	A side input from 0.7 x V_{DDA} to 0.3 x V_{DDA}	18	23	28	ns
			A side input from 0.9 x V_{DDA} to 900mV	32	40	48	
t_{fB}	Fall Time (SDAB, SCLB)	See Figure 8-1 R2 = 95.3Ω C2 = 400pF	B side input from 0.7 x V_{DDB} to 0.3 x V_{DDB}	12	16	20	
			B side input from 0.9 x V_{DDB} to 400mV		30	60	
t_{PLHA-B}	Propagation Delay, Side A to Side B	See Figure 8-1 R1 = 953Ω R2 = 95.3Ω C1 = C2 = 10pF	A side input = 0.55V to B side output = 0.7 x V_{DDB}		100	135	
t_{PHLAB}	Propagation Delay, Side A to Side B		A side input = 0.7V to B side output = 0.4V		100	130	
PWD_{AB}	Pulse Width Distortion		$\lvert t_{PHLAB} - t_{PLHAB} \rvert$		7	30	
t_{PLHBA}[1]	Propagation Delay, Side B to Side A		B side input = 0.4 x V_{DDB} to A side output = 0.7 x V_{DDA}		80	100	
t_{PHLBA}[1]	Propagation Delay, Side B to Side A		B side input = 0.4 x V_{DDB} to A side output = 0.9V		90	120	
PWD_{BA}[1]	Pulse Width Distortion		$\lvert t_{PHLBA} - t_{PLHBA} \rvert$		5	20	
t_{LOOPA}[1]	Loop propagation delay on Side A	See Figure 8-2 R1 = 953Ω C1 = 40pF R2 = 95.3Ω C2 = 400pF	A side input = 0.4V to A side output = 0.3 x V_{DDA}		200	220	
4.5V ≤ (V_{DDA}, V_{DDB}) ≤ 5.5V							
t_{fA}	Fall Time (SDAA, SCLA)	See Figure 8-1 R1 = 1430Ω C1 = 40pF	A side input from 0.7 x V_{DDA} to 0.3 x V_{DDA}	10	12	14	ns
			A side input from 0.9 x V_{DDA} to 900mV	40	50	60	
t_{fB}	Fall Time (SDAB, SCLB)	See Figure 8-1 R2 = 143Ω C2 = 400pF	B side input from 0.7 x V_{DDB} to 0.3 x V_{DDB}	8	10	12	
			B side input from 0.9 x V_{DDB} to 400mV	20	28	36	
t_{PLHAB}	Propagation Delay, Side A to Side B	See Figure 8-1 R1 = 1430Ω R2 = 143Ω C1 = C2 = 10pF	A side input = 0.55V to B side output = 0.7 x V_{DDB}		100	120	
t_{PHLAB}	Propagation Delay, Side A to Side B		A side input = 0.7V to B side output = 0.4V		70	90	
PWD_{AB}	Pulse Width Distortion		$\lvert t_{PHLAB} - t_{PLHAB} \rvert$		30	45	
t_{PLHBA}[1]	Propagation delay, side B to side A		B side input = 0.4 x V_{DDB} to A side output = 0.7 x V_{DDA}		110	130	
t_{PHLBA}[1]	Propagation delay, Side B to side A		B side input = 0.4 x V_{DDB} to A side output = 0.9V		100	150	
PWD_{BA}[1]	Pulse Width Distortion		$\lvert t_{PHLBA} - t_{PLHBA} \rvert$		8	20	
t_{LOOPA}[1]	Loop propagation delay on side A	See Figure 8-2 R1 = 1430Ω C1 = 40pF R2 = 143Ω C2 = 400pF	A side input = 0.4V to A side output = 0.3 x V_{DDA}		210	230	

Note:
1. This parameter applies to the CA-IS3020 (SDAA, SCLA) and CA-IS3021(SDAA) bidirectional lines only.

8 Parameter Measurement Information

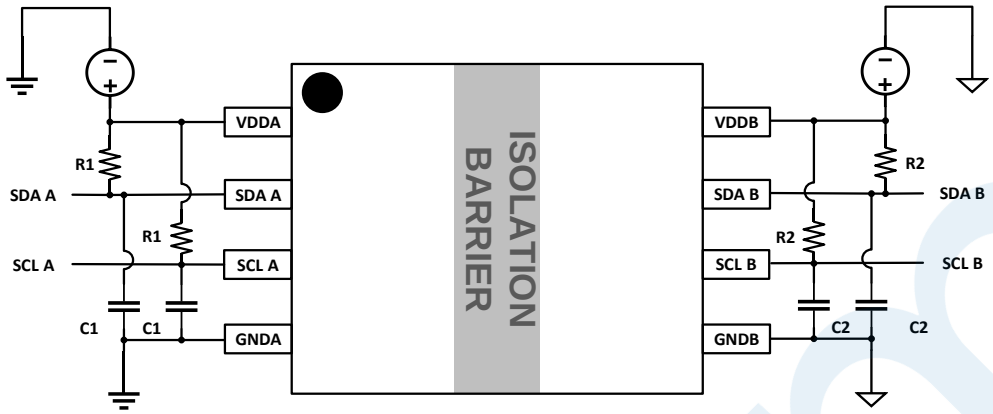


Figure 8-1 Test Circuit

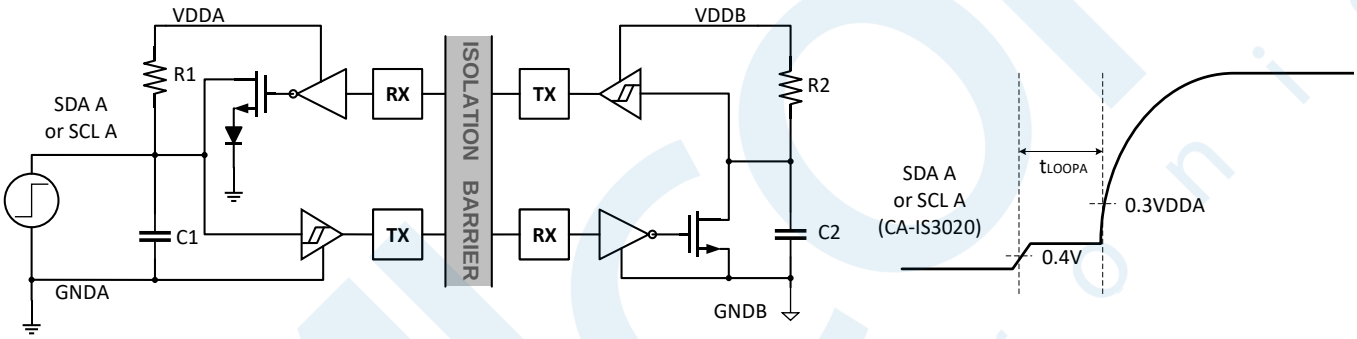


Figure 8-2 t_{LOOPA} Test Circuit and Timing Diagram

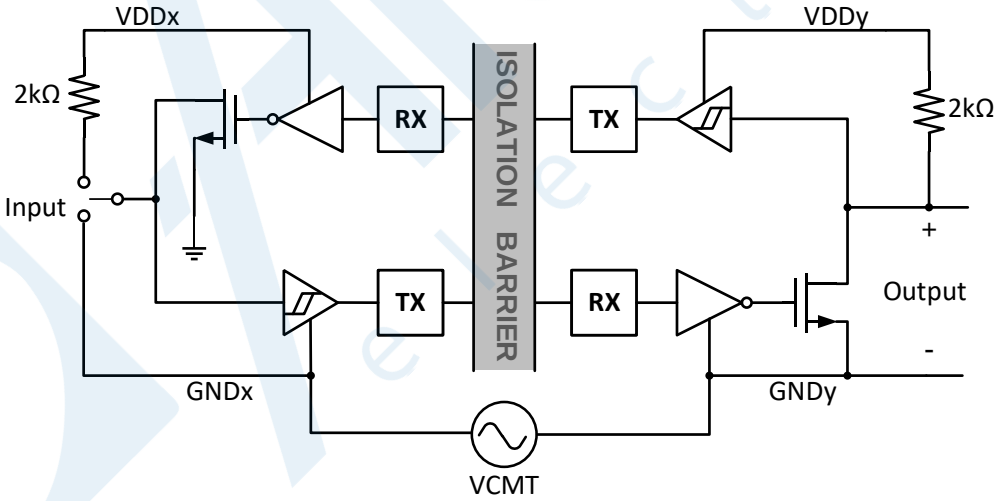


Figure 8-3 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS302x family of devices is complete dual-channel, bidirectional galvanic digital isolators with up to 3.75kV$_{RMS}$ (narrow-body package), 5kV$_{RMS}$ (wide-body package) and 7.5kV$_{RMS}$ (super wide-body package) isolation rating and ±150kV/μs typical CMTI. All devices have Schmitt trigger inputs for high noise immunity and each isolation channel has logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier. The CA-IS3020 offers two bidirectional, open-drain channels for applications, such as multi-master I^{2}C, that require data and clock to be transmitted in both directions on the same line. The CA-IS3021 provides an isolated I^{2}C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). All devices can support up to 2.0MHz operating frequency and feature independent 3.0V to 5.5V supplies (V_{DDA} and V_{DDB}) on each side of the isolator to setup the logic levels independently on either side, see Table 9-1 for the CA-IS302x key features.

The CA-IS302x family are specified over the -40°C to +125°C operating temperature range. The wide temperature range and high isolation voltage make the devices ideal for use in harsh industrial environments.

Table 9-1 key Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION[1]	MAXIMUM FREQUENCY
CA-IS3020	Bidirectional (SCL) Bidirectional (SDA)	Narrow-body package: 3750V$_{RMS}$ Wide-body package: 5000V$_{RMS}$ Super wide-body package: 7500V$_{RMS}$	2MHz
CA-IS3021	Unidirectional (SCL) Bidirectional (SDA)	Narrow-body package: 3750V$_{RMS}$ Wide-body package: 5000V$_{RMS}$	

Note:
1. For more details, please see the *Insulation Specifications* table.

9.2 Functional Block Diagrams

Compared with inductive isolation, the CA-IS302x devices based on capacitive isolation can get low power at high frequency operation, reduces propagation delay and jitter, and provide good immunity to magnetic fields. See Figure 9-1 and Figure 9-2 the CA-IS302x function block diagram for more details. To build the bidirectional signal path, the CA-IS302x integrated two unidirectional isolated signal lines for each bidirectional line. All of output channels provide open-drain output to comply with the standard I^{2}C interface. Side A is designed to connect to the low capacitance I^{2}C node with up to 40pF of load capacitance, while side B is designed for connecting to a fully loaded I^{2}C bus with up to 400pF of load capacitance.

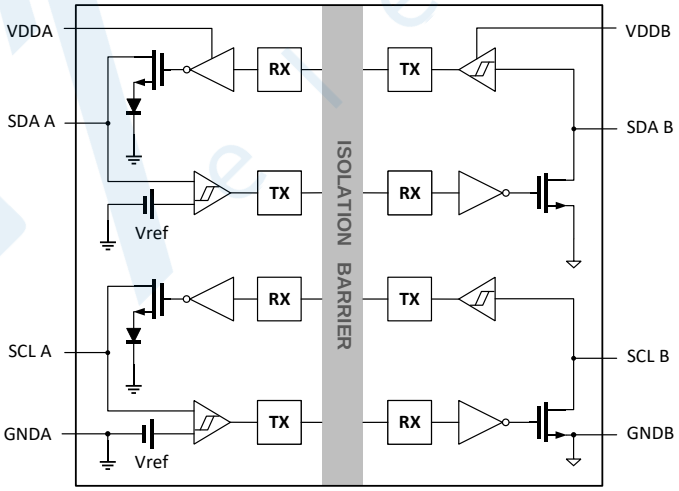


Figure 9-1 The Block Diagram for CA-IS3020

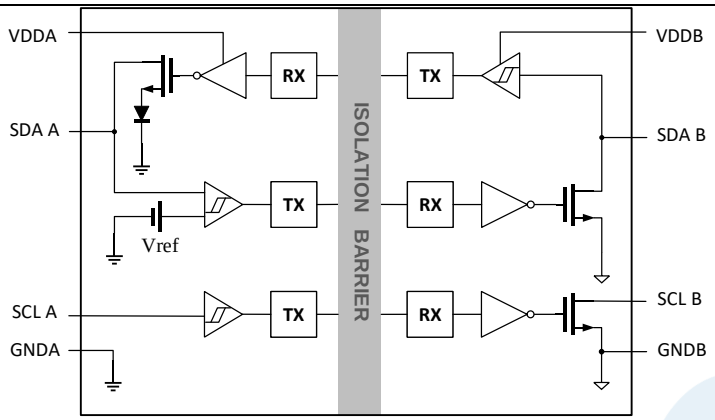


Figure 9-2 The Block Diagram for CA-IS3021

9.3 Device Operation Modes

Table 9-2 lists the CA-IS302x functional modes. For optimal performance, ensure that the load capacitance on side A (C_A) is ≤ 40pF, and the load capacitance on side B (C_B) is ≤ 400pF. The maximum static output loading on side A is 3.5mA, while on side B, the maximum static output current is 35mA. For the bidirectional isolation channels, to prevent latch-up action, the A-side outputs comprise special buffers that regulate the logic-low voltage at approximately 700mV, and the maximum input logic-low voltage is 400mV. The internal comparator with hysteresis determines whether the logic-low level comes from the input or output based on the logic-low voltages at SDAA and SCLA pins. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B and thus preventing a latching action. The B side features conventional buffers that do not regulate logic-low output voltage. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device.

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions with 1.95V minimum threshold and 2.53V maximum threshold. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage event is detected on either of the supplies (V_{DDA}≤ 1.95V or/and V_{DDB} ≤ 1.95V), all bidirectional outputs become high-impedance and are pulled high by the external pullup resistor on the open-drain outputs.

Table 9-2 Truth Table

POWER STATE	INPUT	OUTPUT
V_{DDA} or V_{DDB} < 1.95V	X	Hi-Z
V_{DDA} and V_{DDB} > 2.53V	L	L
V_{DDA} and V_{DDB} > 2.53V	H	Hi-Z
V_{DDA} and V_{DDB} > 2.53V	Hi-Z[2]	Indeterminate

Notes:
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. Invalid input condition as an I²C system requires that a pull-up resistor to VDD_ is connected on the bus.

10 Application and Implementation

10.1 Overview

The Inter IC (I²C) bus is a simple, 2-wire bus for communication between different ICs (system controller, remote sensor, actuator etc. circuitry). 2-wire interfaces use only a data line (SDA) and a clock line (SCL) and allow to connect multiple slaves on the same bus without needing chip-select signals. Because 2-wire interfaces have only one data line, they can operate in half-duplex mode only, this means data can only be transmitted or received on a given cycle, also, the data line should be bidirectional. For the multi-master I²C applications, both data and clock lines need to transmit in both directions on the same line. The CA-IS302x family of digital isolators offers two bidirectional channels (CA-IS3020) or one unidirectional channel for clock and one

bidirectional channel for data (CA-IS3021), is ideal for use in I²C bus to provide the required isolation between different ground potentials of the system circuitry to prevent ground loop currents that otherwise may falsify the acquired data. The I²C bus can operate in Standard mode, Fast mode, or High-speed mode, with maximum data rates of 100kbps (Standard mode), 400kbps (Fast mode), 1.7Mbps (High-speed mode with C_{bus} = 400pF). The CA-IS302x digital isolators can support up to 2.0MHz operating frequency, thus can support most of I²C communication applications.

10.2 Typical Application

The CA-IS302x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. These devices do not require special power-supply sequencing, the logic levels are set independently on either side by V_{DDA} and V_{DDB}. The SDAA, SCLA, SDAB, SCLB pins have open-drain outputs, requiring pull-up resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 35mA for side B, and 3.5mA for side A. So the minimum pullup resistors on the input lines must be selected in such a way that input current drawn is ≤ 3.5mA on side A and output current drawn is ≤ 35mA on side B. The maximum pull-up resistors on the input lines and output lines depend on the load and rise time requirements on the respective lines.

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with at least 0.1μF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 and Figure 10-2 show typical operating circuit of the CA-IS3020 and CA-IS3021.

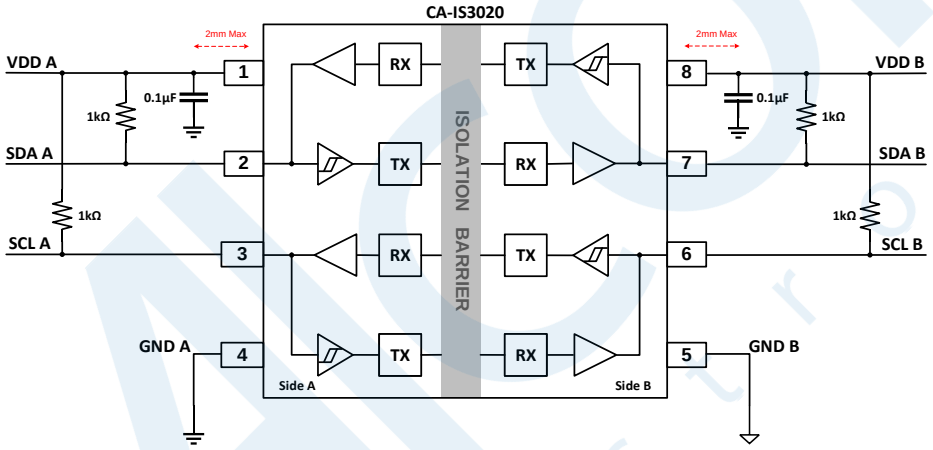


Figure 10-1 The Typical Application Circuit for CA-IS3020

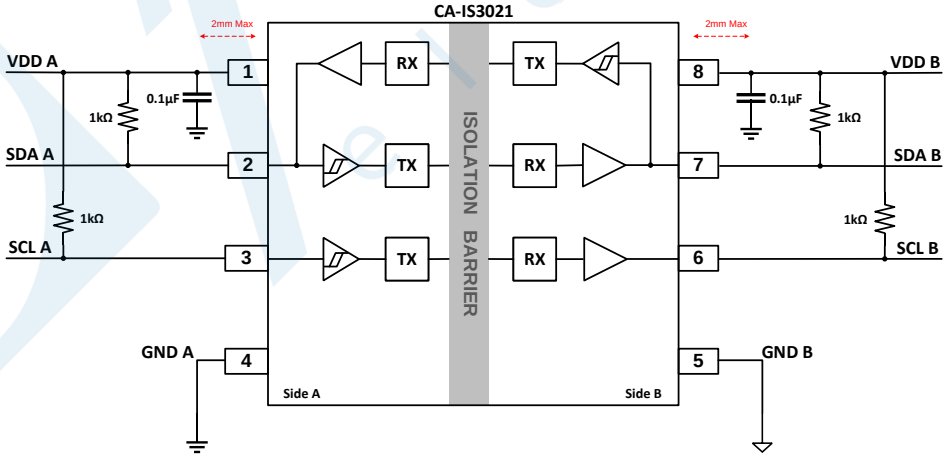
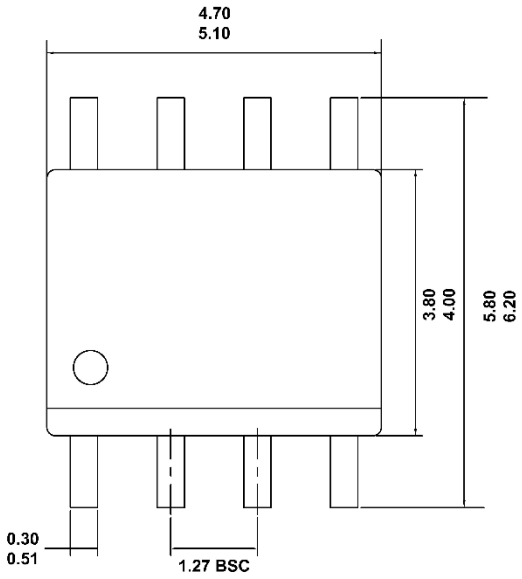


Figure 10-2 The Typical Application Circuit for CA-IS3021

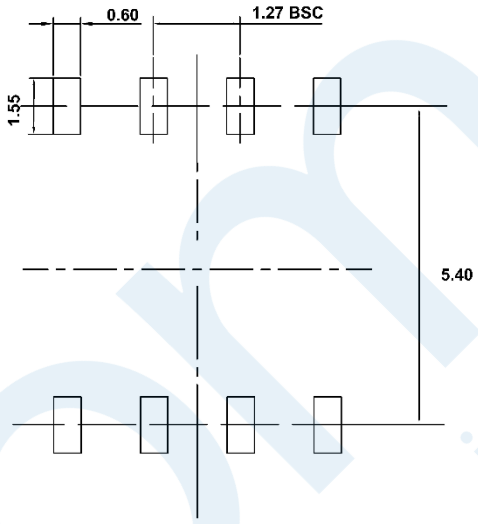
11 Package Information

11.1 SOIC8 (S) Package

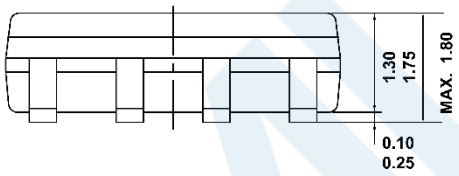
The values for the dimensions are shown in millimeters.



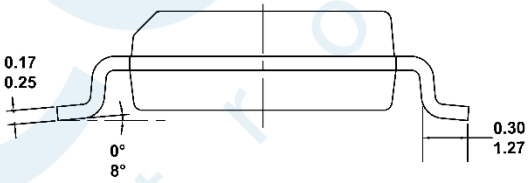
TOP VIEW



RECOMMENDED LAND PATTERN



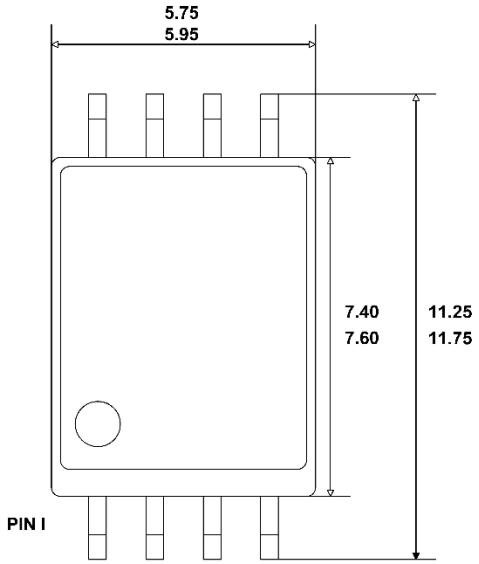
FRONT VIEW



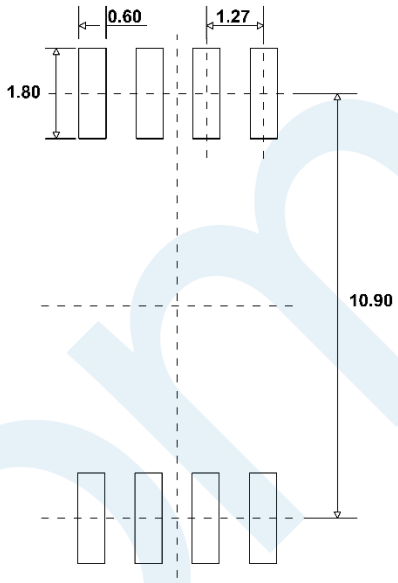
LEFT SIDE VIEW

11.2 SOIC8-WB (G) Package

The values for the dimensions are shown in millimeters.



TOP VIEW



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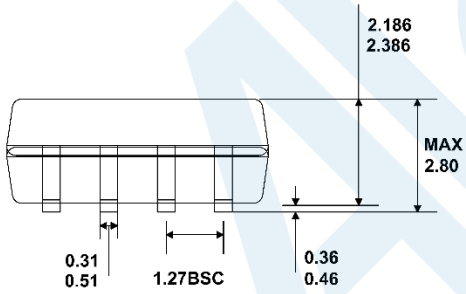
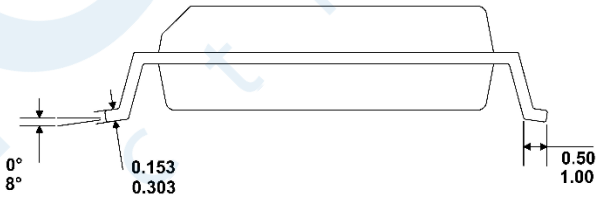


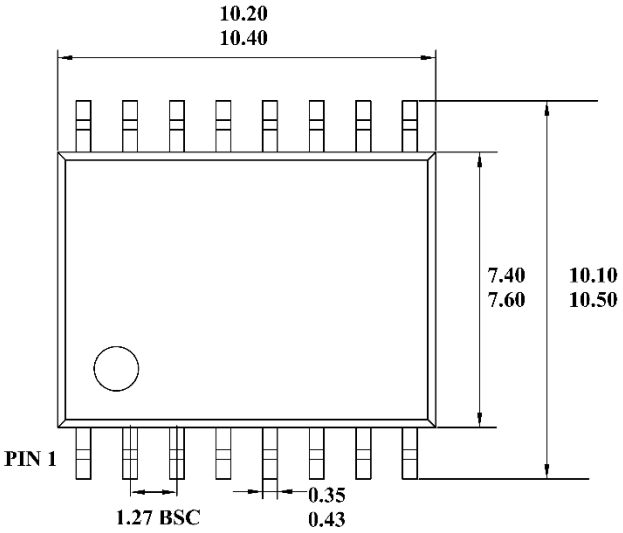
FRONT VIEW



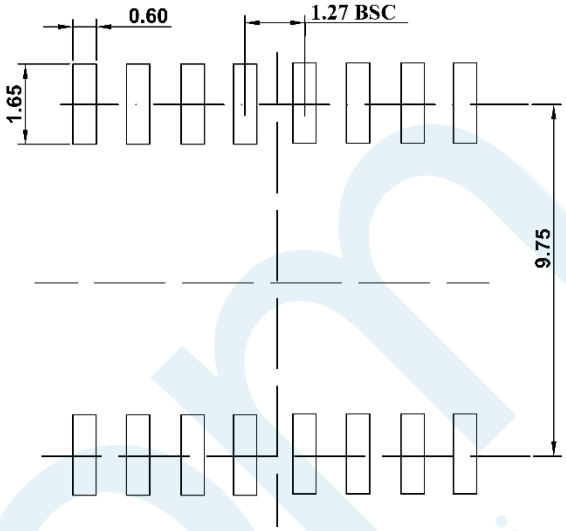
LEFT-SIDE VIEW

11.3 SOIC16-WB (W) Package

The values for the dimensions are shown in millimeters.



TOP VIEW



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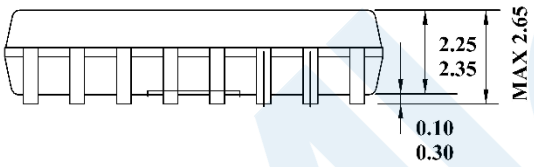
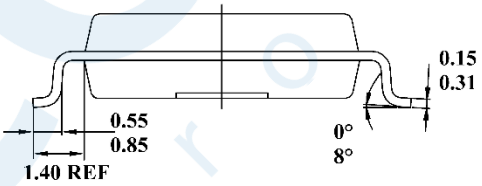


FRONT VIEW



LEFT SIDE VIEW

11.4 SOIC8-WWB (WG) Package

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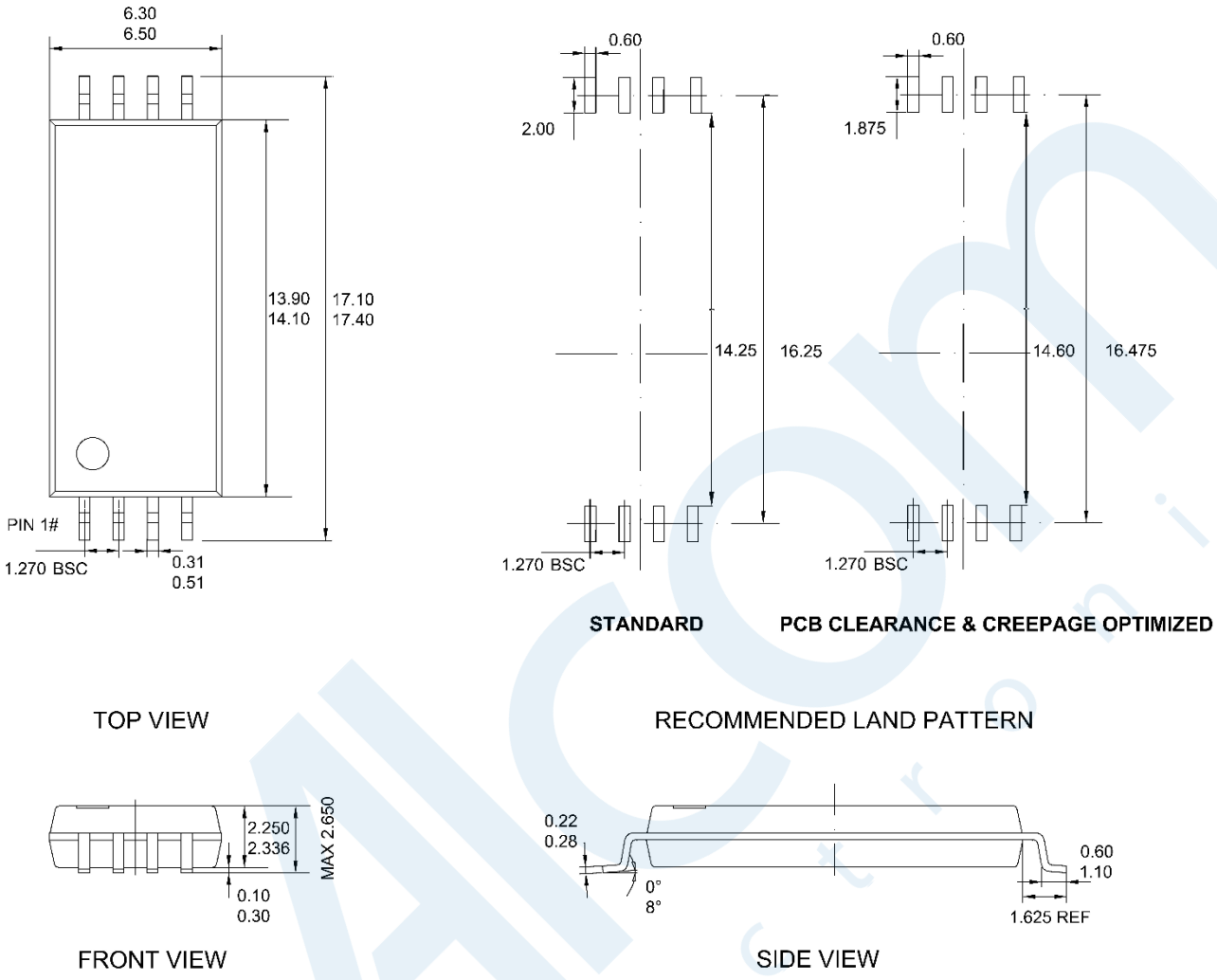


12 Soldering Information

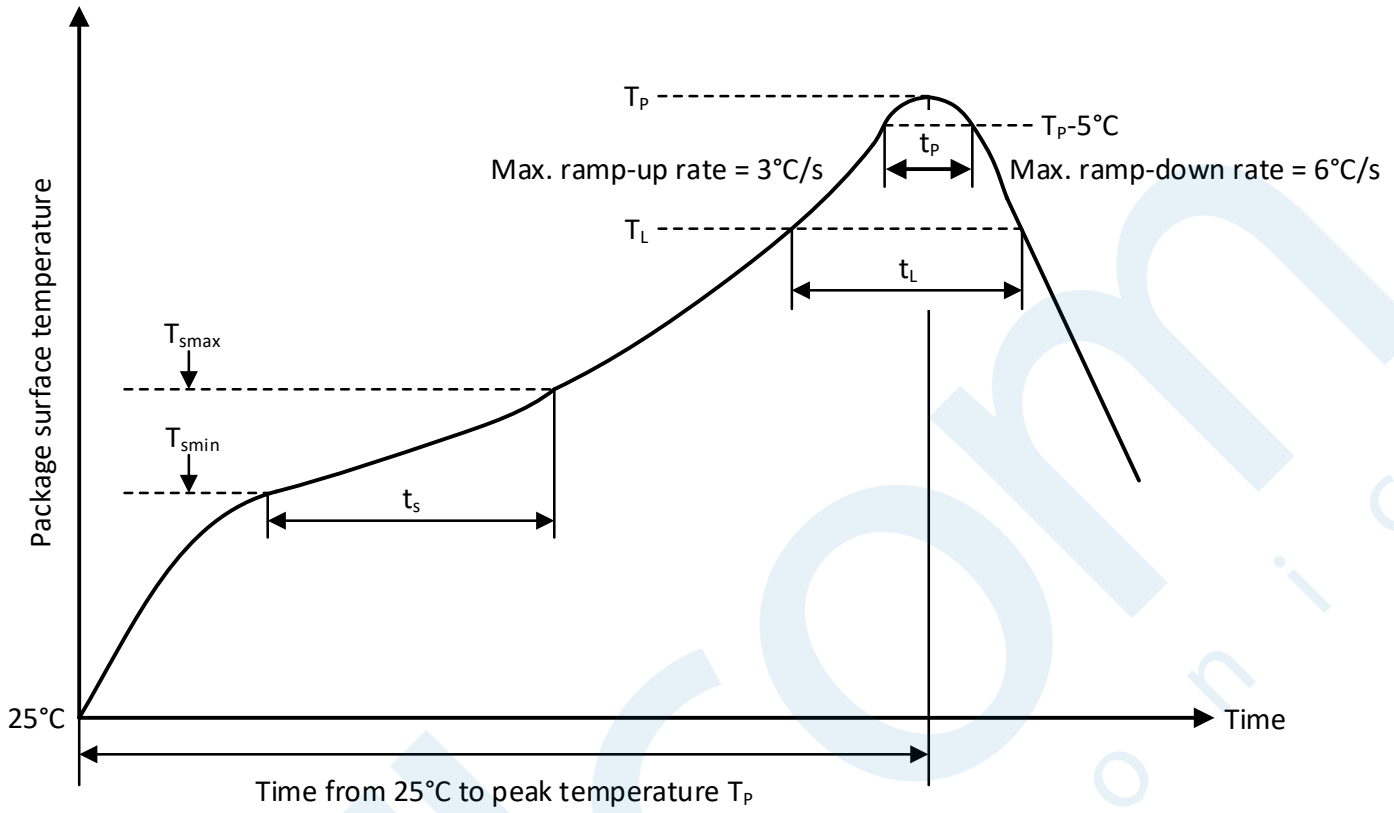


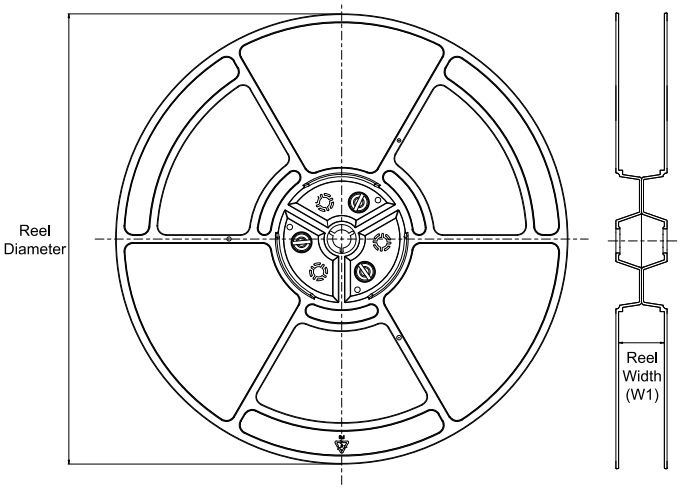
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

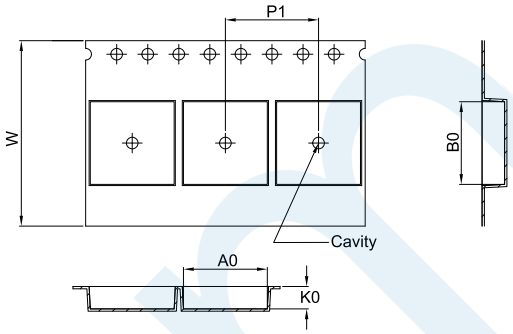
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Soldering Information

REEL DIMENSIONS

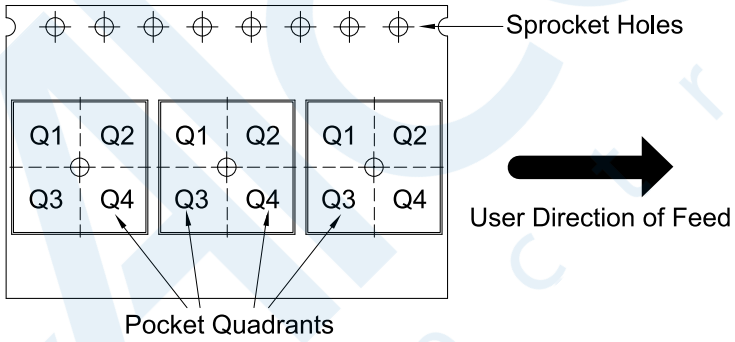


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3020S	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3020G	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3021S	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3021G	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3020W	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3021W	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3020WG	SOIC	WG	8	500	330	16.4	17.70	6.80	2.80	24.00	16.00	Q1

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