GOWINSEMI's Arora V FPGA series provides SRAM based FPGA devices with increased logic resources, interfaces and performance. Arora V FPGAs include DDR3 memory interfacing, 12.5Gbps CDR based SERDES supporting multiple protocols and flexible packaging options making it the ideal choice for communications, server, imaging, and automotive applications requiring high interface and computing throughput by providing best performance/watt.

Arora V is supported by GOWIN EDA providing an efficient and easy to use FPGA hardware development environment support multiple RTL based programming languages, synthesis, placement & routing, bitstream generation and download, power analysis and in-device logic analyzer.

Arora V FPGA Product Features:

FPGA Fabric Architecture

- Up to 138K LUTs(GW5A(T)-138)
- Up to 23K LUTs(GW5A-25)
- Block SRAM with multiple modes
    - Single Port, Semi-Dual Port, True Dual Port, and Semi Dual Port with ECC function
    - Byte write enable
    - ECC error detection and correction
- High performance DSP
    - Multipliers support 12x12, 27x36, 27x18-bit modes
    - Includes 48-bit accumulator
    - Supports DSP cascading
    - Embedded pipeline and bypass registers
    - Pre-addtion operation for filter function
    - Internal feedback loop and barrel shifter
- Advanced Clocking
    - Up to 32 global clocks
    - Up to 6/12 high-performance PLLs
    - Up to 16/24 high speed edge clocks

Flexible GPIO

- Adjustable drive strength
    - 4mA, 8mA, 12mA, 16mA, 24mA drive
- Bus keeper, pull up/down and open drain
- Hot Socket and input hysteresis
- Slew Rate option for output signal

ADC

- 60dB SNR and 1kHz Signal Bandwidth
- Flexible X-channel oversampling ADC
- No external voltage source required

Configuration & Programming

- JTAG, SSPI, MSPI, CPU, and SERIAL
    - Background programming
    - SPI Flash Programming and Boot
    - Multi-boot
- Bitstream encryption and Security
- SEU error detection and correction
- Supports OTP, each device has a unique 64-bit DNA identifer

High Speed Interfaces

- SERDES(GW5AT-138)
    - 270Mbps-12.5Gbps operation
    - CDR (Clock Data Recovery)
    - Dedicated RX and TX Channels
    - Integrated 8b/10b encoder/decoder
    - PCI 2.0 hardcore
        - x1, x2, x4, x8 lanes
        - Supports root complex and end point
- MIPI D-PHY RX hardcore(GW5A(T)-138)
    - 20Gbps D-PHY RX Hard PHY

    - 8 data lanes + 2 clock lanes
    - 2.5Gbps/lane
    - Built-in SoT HS-Sync, word and lane alignment
    - MIPI DSI and MIPI CSI-2 RX link layer IPs
- MIPI D-PHY RX/TX hardcore(GW5A-25)
    - 4 data lanes + 1 clock lane
    - 2.5Gbps/lane(RX/TX)
    - Built-in SoT HS-Sync, word and lane alignment
    - MIPI DSI and MIPI CSI-2 RX link layer IPs
- GPIOs support MIPI C-PHY RX/TX and D-PHY RX/TX(GW5A-25)
    - 1.2Gbps/lane
    - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX/TX device interface
- GPIOs support MIPI D-PHY RX(GW5AT-138)
    - 5Gbps/lane
    - GPIOs can be configured as MIPI DSI and MIPI CSI-2 RX device interface
- External DRAM Interfaces
    - Supports various memory types
        - DDR2, DDR3, PSRAM, HyperRAM, RPC
    - Up to 1333 Mbps (GW5A(T)-138) or 1066 Mbps (GW5A-25)