AMIC

A25L040B Series

Ultra Low Power, 4M-bit

Preliminary *Serial Multi I/O Flash Memory*

Document Title

Ultra Low Power, 4M-bit Serial Multi I/O Flash Memory

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	March 3, 2022	Preliminary

Ultra Low Power, 4M-bit Serial Multi I/O Flash Memory

Preliminary

FEATURES

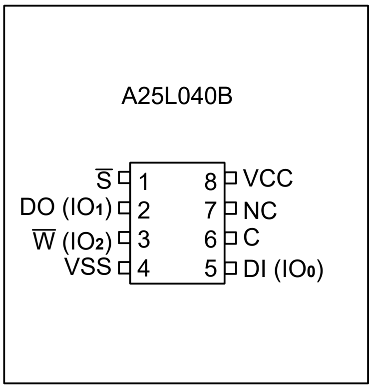
- 4M-bit Serial Flash
  - 512K-Byte
  - 256 Bytes per programmable page
- Standard, Dual
  - Standard SPI: C, $\overline{S}$, DI, DO, $\overline{W}$
  - Dual SPI: C, $\overline{S}$, IO_0, IO_1, $\overline{W}$
- High Speed Clock Frequency
  - 104MHz for fast read with 30pF load
  - Dual I/O Data transfer up to 208Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with $\overline{W}$ Pin
  - Top/Bottom Block protection
- Minimum 100,000 Program/Erase Cycles
- Data Retention
  - 20-year data retention typical
- Fast Program/Erase Speed
  - Page Program time: 1.1ms typical
  - Sector Erase time: 2.6ms typical
  - Block Erase time: 2.6ms typical
  - Chip Erase time: 5.2ms typical
- Flexible Architecture
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- Low Power Consumption
  - 0.65uA typical deep power down current
  - 8uA typical standby current
- Advanced Security Features
  - 128-Bit Unique ID for each device
  - 3x512-Byte security registers with OTP locks
  - Discoverable parameters (SFDP) register
- Single Power Supply Voltage
  - Full voltage range: 2.3V~3.6V
- Package Information
  - DIP8 (300mil)
  - SOP8 (150mil)
  - SOP8 (209mil)
  - USON (2*3mm)
  - WSON8 (6*5mm)
  - All Pb-free (Lead-free) products are RoHS compliant

GENERAL DESCRIPTION

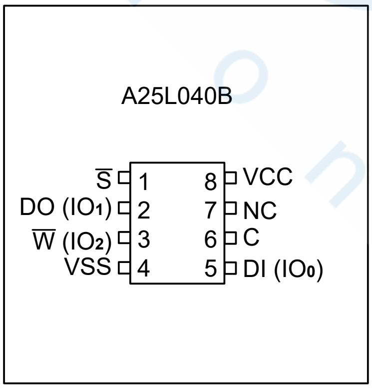
The A25L040B(4M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O_0 (DI), I/O_1 (DO), $\overline{W}$. The Dual I/O data is transferred with speed of 208Mbits/s.

Pin Configurations

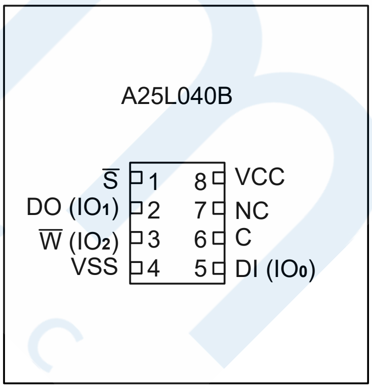
■ **DIP8(300mil)**



■ **SOP8(150mil / 209mil)**



■ **USON8(2*3mm) / WSON8(6*5mm)**

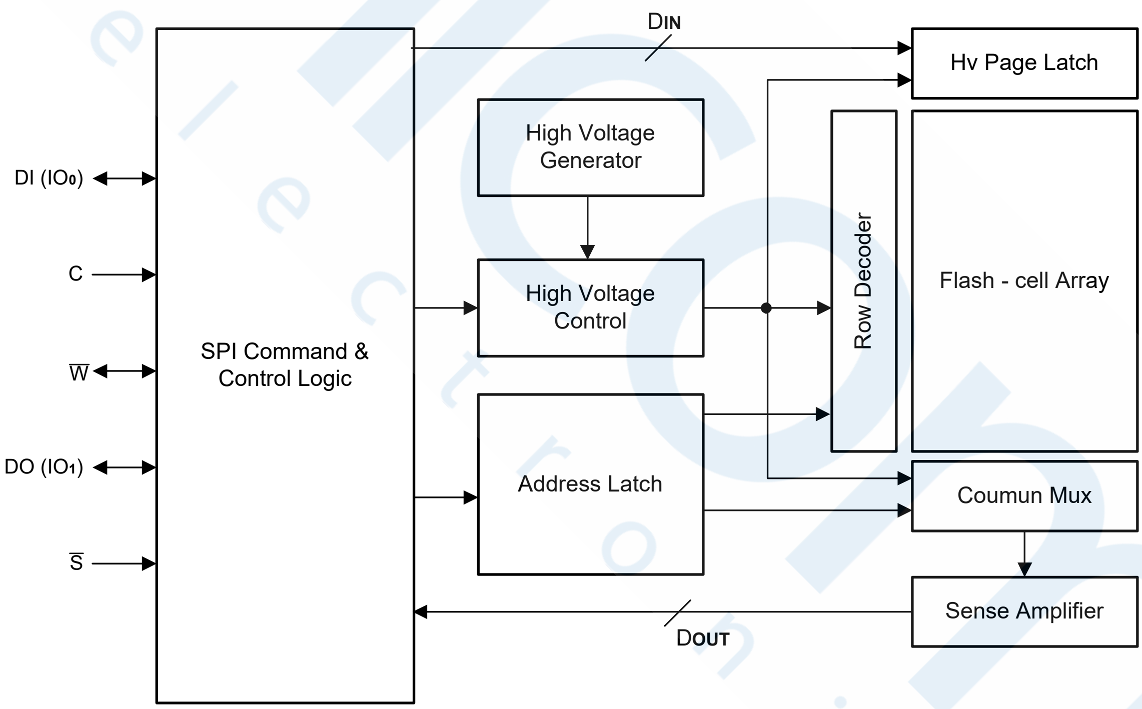


Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	$\overline{S}$	I	Chip Select Input
2	DO (IO_1)	I/O	Data Output (Data Input Output 1)
3	$\overline{W}$	I/O	Write Protect Input
4	VSS		Ground
5	DI (IO_0)	I/O	Data Input (Data Input Output 0)
6	C	I	Serial Clock Input
7	NC		Not Connection
8	VCC		Power Supply

Notes: $\overline{S}$ must be driven high if chip is not selected. Please don't leave $\overline{S}$ floating any time after power is on.

Block Diagram



MEMORY ORGANIZATION

A25L040B

Each device has	Each block has	Each sector has	Each page has	
512K	64K/32K	4K	256	bytes
2K	256/128	16	-	pages
128	16/8	-	-	sectors
8/16	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

A25L040B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
7	127	07F000H	07FFFFH
	......	......	......
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	......	......	......
	96	060000H	060FFFH
......	......	......	......
	......	......	......
	......	......	......
......	......	......	......
	......	......	......
	......	......	......
2	47	02F000H	02FFFFH
	......	......	......
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	......	......	......
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	......	......	......
	0	000000H	000FFFH

DEVICE OPERATION

SPI Mode
Standard SPI
The A25L040B features a serial peripheral interface on 4 signals bus: Serial Clock (C), Chip Select ($\overline{S}$), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of C and data shifts out on the falling edge of C.

Dual SPI
The A25L040B supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command the DI and DO pins become bidirectional I/O pins: IO_0 and IO_1.

DATA PROTECTION

The A25L040B provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - 0.5K Sector Erase (SE05K) / Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: $\overline{W}$ goes low to protect the BP0~BP4 bits and SRP0~1 bits.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table 1.0 A25L040B Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
x	x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000H-07FFFFH	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000H-07FFFFH	128KB	Upper 1/4
0	0	0	1	1	4 to 7	040000H-07FFFFH	256KB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/4
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/2
0	x	1	x	x	0 to 7	000000H-07FFFFH	512KB	ALL
1	0	0	0	1	7	07F000H-07FFFFH	4KB	Upper 1/128
1	0	0	1	0	7	07E000H-07FFFFH	8KB	Upper 1/64
1	0	0	1	1	7	07C000H-07FFFFH	16KB	Upper 1/32
1	0	1	0	x	7	078000H- 07FFFFH	32KB	Upper 1/16
1	0	1	1	0	7	078000H-07FFFFH	32KB	Upper 1/16
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/128
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/64
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/32
1	1	1	0	x	0	000000H-007FFFH	32KB	Lower 1/16
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/16
1	x	1	1	1	0 to 7	000000H-07FFFFH	512KB	ALL

Table 1.1 A25L040B Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
x	x	0	0	0	0 to 7	000000H-07FFFFH	512KB	ALL
0	0	0	0	1	0 to 6	000000H-06FFFFH	448KB	Lower 7/8
0	0	0	1	0	0 to 5	000000H-05FFFFH	384KB	Lower 3/4
0	0	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/2
0	1	0	0	1	1 to 7	010000H-07FFFFH	448KB	Upper 7/8
0	1	0	1	0	2 to 7	020000H-07FFFFH	384KB	Upper 3/4
0	1	0	1	1	4 to 7	040000H-07FFFFH	256KB	Upper 1/2
0	x	1	x	x	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 7	000000H-07EFFFH	508KB	Lower 127/128
1	0	0	1	0	0 to 7	000000H-07DFFFH	504KB	Lower 63/64
1	0	0	1	1	0 to 7	000000H-07BFFFH	496KB	Lower 31/32
1	0	1	0	x	0 to 7	000000H-077FFFH	480KB	Lower 15/16
1	0	1	1	0	0 to 7	000000H-077FFFH	480KB	Lower 15/16
1	1	0	0	1	0 to 7	001000-07FFFFH	508KB	Upper 127/128
1	1	0	1	0	0 to 7	002000-07FFFFH	504KB	Upper 63/64
1	1	0	1	1	0 to 7	004000-07FFFFH	496KB	Upper 31/32
1	1	1	0	x	0 to 7	008000-07FFFFH	480KB	Upper 15/16
1	1	1	1	0	0 to 7	008000-07FFFFH	480KB	Upper 15/16
1	x	1	1	1	NONE	NONE	NONE	NONE

STATUS REGISTER

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	Reserved	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.
The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.
The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.
The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE), 0.5K Sector Erase (SE05K), 32K Block Erase(BE32) and 64K Block Erase (BE64) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1.

SRP1, SRP0 bits.
The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	$\overline{W}$	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	$\overline{W}$ =0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	$\overline{W}$ =1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be writtento.

Notes:
1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact AMIC Device for details.

LB3, LB2, LB1 bit.
The LB3, LB2, and LB1 bit is a non-volatile One Time Program (OTP) bit in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2, and LB1 is 0, the security registers are unlocked. LB3, LB2, and LB1 can be set to 1 individually using the Write Register instruction. LB3, LB2, and LB1 is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

CMP bit
The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status Registers Memory Protection table for details. The default setting is CMP=0.

SUS1, SUS2 bit
The SUS1 and SUS2 bits are read only bits in the status register (S15, S10) that is set to 1 after executing an Erase/Program Suspend (75H or B0H) command. SUS1 will be set 1 for erase suspend, and SUS2 will be set 1 for program suspend. The SUS1 and SUS2 bits will be cleared to 0 by Erase/Program Resume (7AH or 30H) command as well as a power-down, power- up cycle.

COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of C after $\overline{S}$ is driven low. Then, the one-Byte command code must be shifted in to the device, with most significant bit first on DI, and each bit is latched on the rising edges of C.
See Table 2, every command sequence starts with a one-Byte command code. Depending on the command, this might be followed by address Bytes, or by data Bytes, or by both or none. $\overline{S}$ must be driven high after the last bit of the command sequence has been completed. For the commands of Read, Fast Read, Read Status Register or Release from Deep Power- Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then $\overline{S}$ must be driven high to return to deselected status.
For the commands of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, $\overline{S}$ must be driven high exactly at a Byte boundary, otherwise the command is rejected, and is not executed. That means $\overline{S}$ must be driven high when the number of clock pulses after $\overline{S}$ being driven low is an exact multiple of eight. For Page Program, if $\overline{S}$ is driven high at any time the input Byte is not a full Byte, nothing will happen and WEL will not be reset.

Table 2. Commands (Standard/Dual SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Volatile SR Write Enable	50H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	S7-S0	S15-S8				
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[1]	(continuous)
Dual I/O Fast Read	BBH	A23-A8[2]	A7-A0 M7-M0[2]	(D7-D0)[1]			(continuous)
Continuous Read Mode Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte	
Dual Input Page Program	A2H	A23-A16	A15-A8	A7-A0	D7-D0		
Sector Erase(0.5K)	8AH	A23-A16	A15-A8	A7-A0			
Sector Erase(4k)	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Enable Reset	66H						
Reset	99H						
Program/Erase Suspend	75/B0H						
Program/Erase Resume	7A/30H						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Manufacturer/ Device ID by Dual I/O	92H	A23-A8	A7-A0, M7-M0	(MID7-MID0) (DID7-DID0)			(continuous)
Read Unique ID	4BH	dummy	dummy	dummy	dummy	(UID7-UID0)	(continuous)
Read Identification	9FH	(MID7- M0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Erase Security Registers[3]	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers[3]	42H	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	
Read Security Registers[3]	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

Notes:

1. Dual Output data
   IO_0 = (D6, D4, D2, D0) IO_1 = (D7, D5, D3, D1)
2. Dual Input Address
   IO_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
3. Security Registers Address:
   Security Register1: A23-A16=00H, A15-A12=01H, A11-A9=0H, A8-A0= Byte Address;
   Security Register2: A23-A16=00H, A15-A12=02H, A11-A9=0H, A8-A0= Byte Address;
   Security Register3: A23-A16=00H, A15-A12=03H, A11-A9=0H, A8-A0= Byte Address.

Table of ID Definitions:

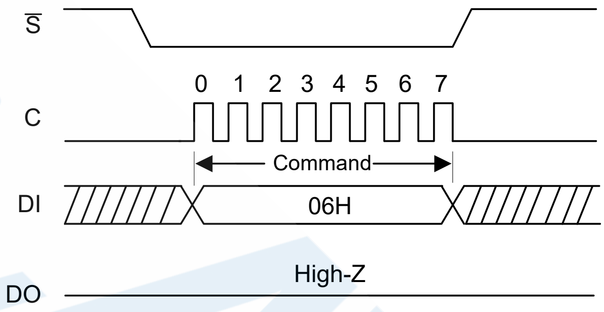
A25L040B

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	37	30	13
90H	37		12
ABH			12

Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), 0.5K Sector Erase (SE05K), 32K Block Erase (BE32), 64K Block Erase (BE64), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: $\overline{S}$ goes low sending the Write Enable command $\overline{S}$ goes high.

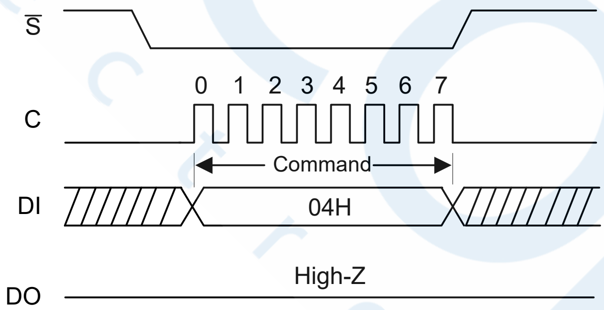
Figure 1. Write Enable Sequence Diagram



Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: $\overline{S}$ goes low Sending the Write Disable command $\overline{S}$ goes high. The WEL bit is reset by following condition: Power- up and upon completion of the Write Status Register, Page Program, Sector Erase, 0.5K Sector Erase (SE05K), 32K Block Erase (BE32), 64K Block Erase(BE64), Chip Erase, Erase/Program Security Registers and Reset commands.

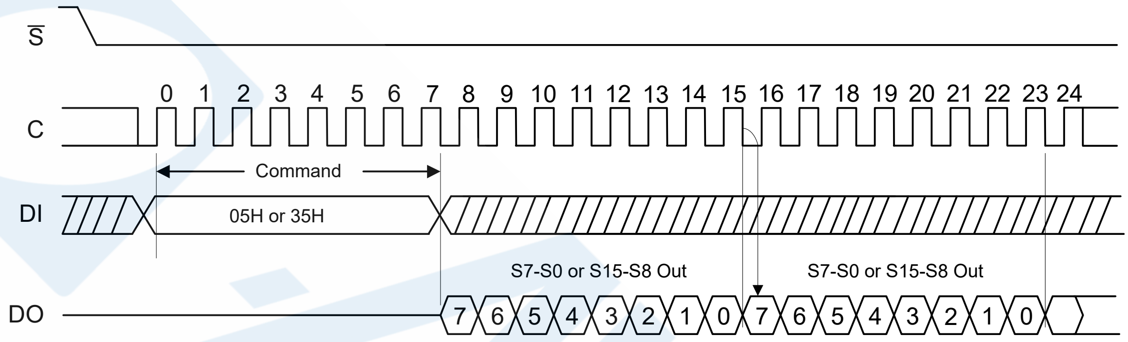
Figure 2. Write Disable Sequence Diagram



Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the DO will output Status Register bits S7~S0. The command code "35H", the DO will output Status Register bits S15~S8.

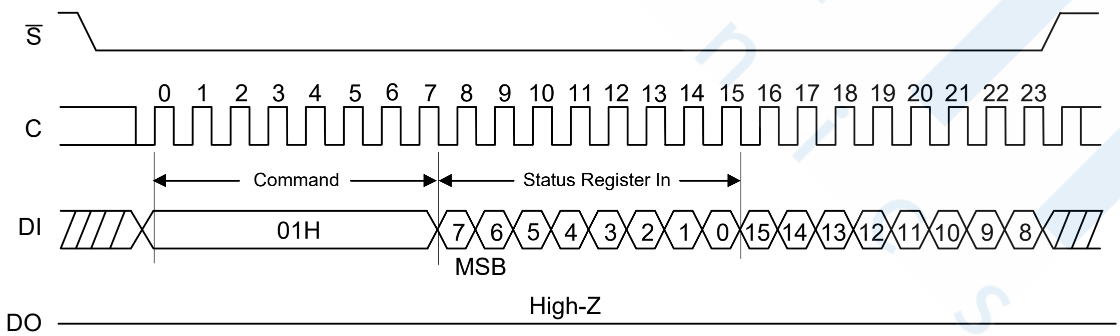
Figure 3. Read Status Register Sequence Diagram



Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).
The Write Status Register (WRSR) command has no effect on S15, S10,S1 and S0 of the Status Register. $\overline{S}$ must be driven high after the eighth or sixteen bit of the data Byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If $\overline{S}$ is driven high after eighth bit of the data Byte, the CMP and QE bit will be cleared to 0. As soon as $\overline{S}$ is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.
The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1, SRP0) bit in accordance with the Write Protect ($\overline{W}$) signal. The Status Register Protect (SRP1, SRP0) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

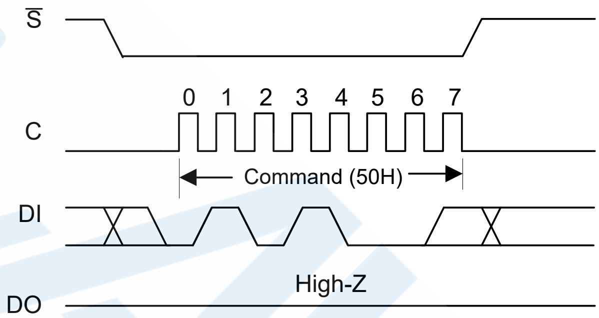
Figure 4. Write Status Register Sequence Diagram



Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

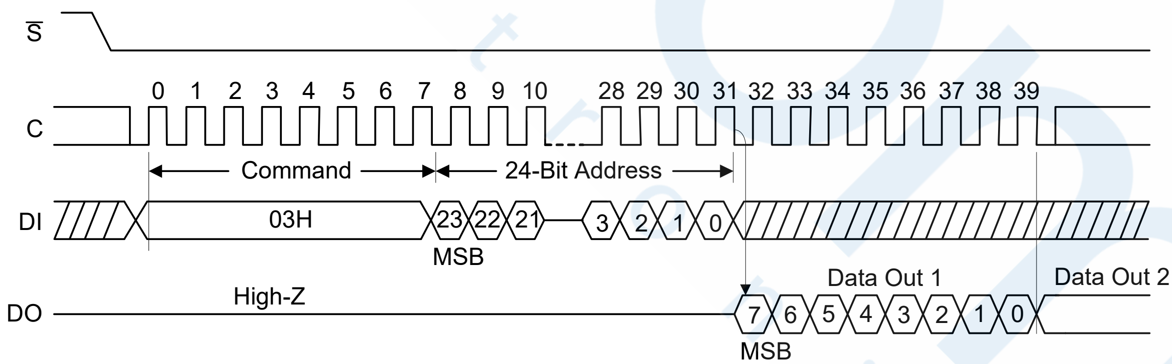
Figure 5. Write Enable for Volatile Status Register Sequence Diagram



Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-Byte address (A23-A0), and each bit is latched-in on the rising edge of C. Then the memory content at that address is shifted out on DO, and each bit is shifted out at a Max frequency f_R on the falling edge of C. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

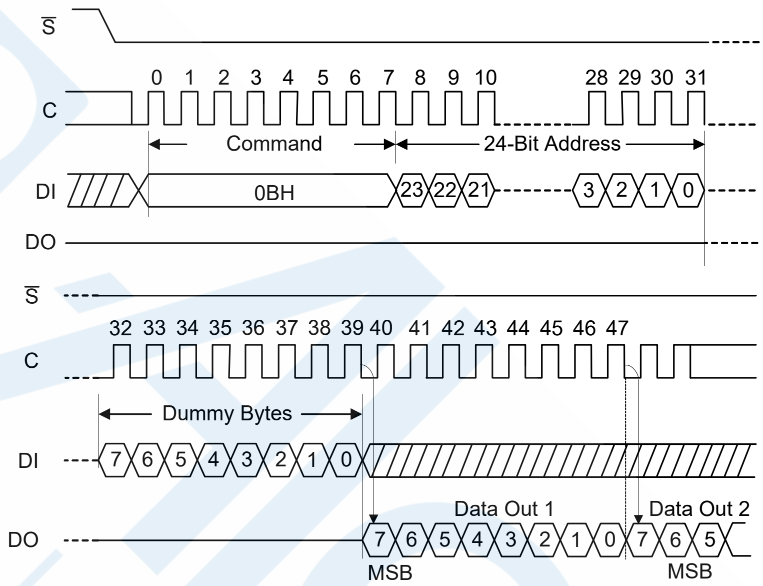
Figure 6. Read Data Bytes Sequence Diagram



Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3- Byte address (A23-A0) and a dummy Byte, and each bit is latched-in on the rising edge of C. Then the memory content at that address is shifted out on DO, and each bit is shifted out at a Max frequency fc, on the falling edge of C. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

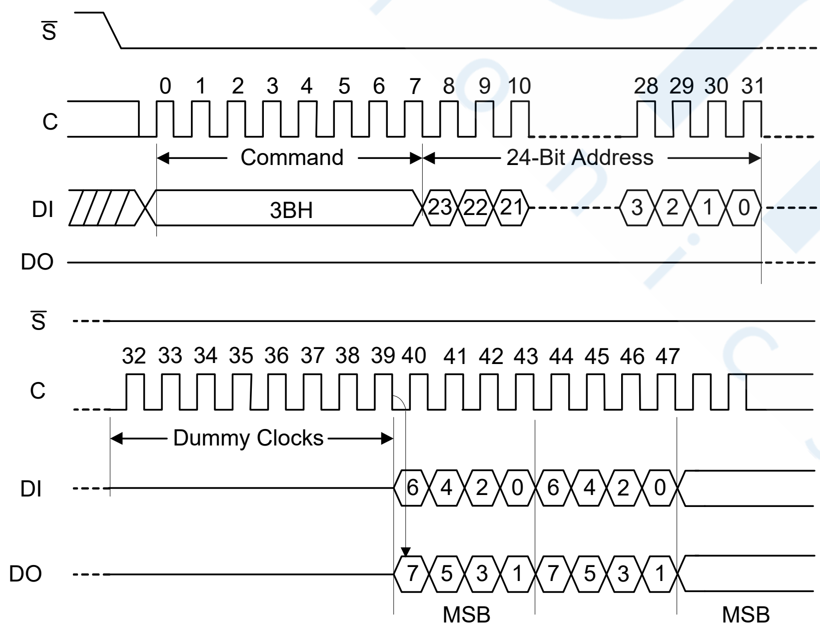
Figure 7. Read Data Bytes at Higher Speed Sequence Diagram



Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-Byte address (A23-A0) and a dummy Byte, each bit being latched in during the rising edge of C, then the memory contents are shifted out 2-bit per clock cycle from DI and DO. The command sequence is shown in followed Figure 8. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 8. Dual Output Fast Read Sequence Diagram



Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-Byte address (A23-0) and a "Continuous Read Mode" Byte 2-bit per clock by DI and DO, and each bit is latched in on the rising edge of C, then the memory contents are shifted out 2-bit per clock cycle from DI and DO. The command sequence is shown in followed Figure 9. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Dual I/O Fast Read with "Continuous Read Mode"
The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-Byte address (A23-A0). If the "Continuous Read Mode" bits (M7-0) =AXH, then the next Dual I/O Fast Read command (after $\overline{S}$ is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure 10. If the "Continuous Read Mode" bits (M7-0) are any value other than AXH, the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure 9. Dual I/O Fast Read Sequence Diagram (M7-0= 0XH or not AXH)

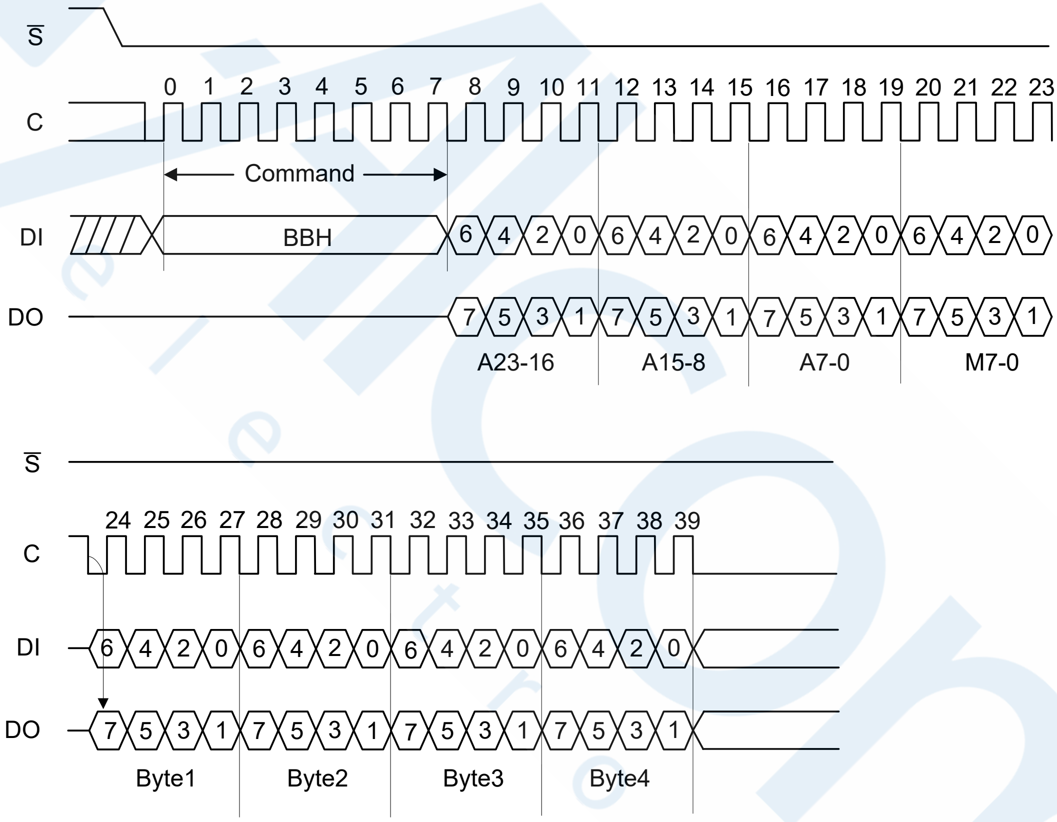
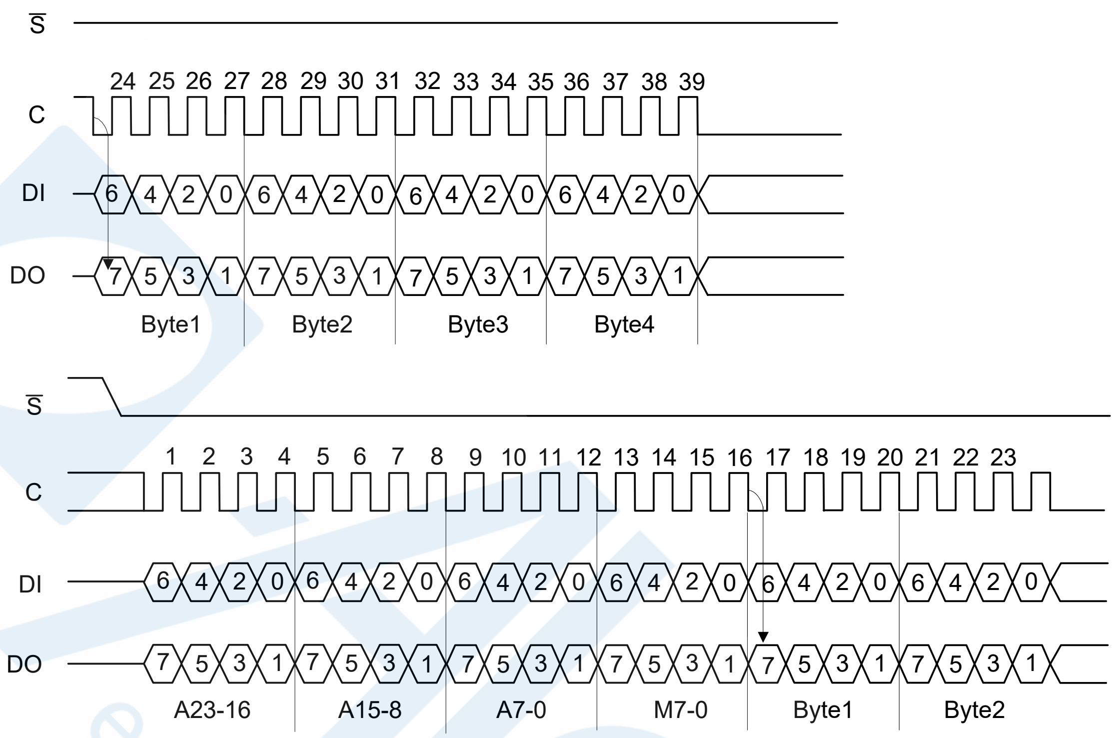


Figure 10. Dual I/O Fast Read Sequence Diagram (M7-0= AXH)



Page Program (PP) (02H)

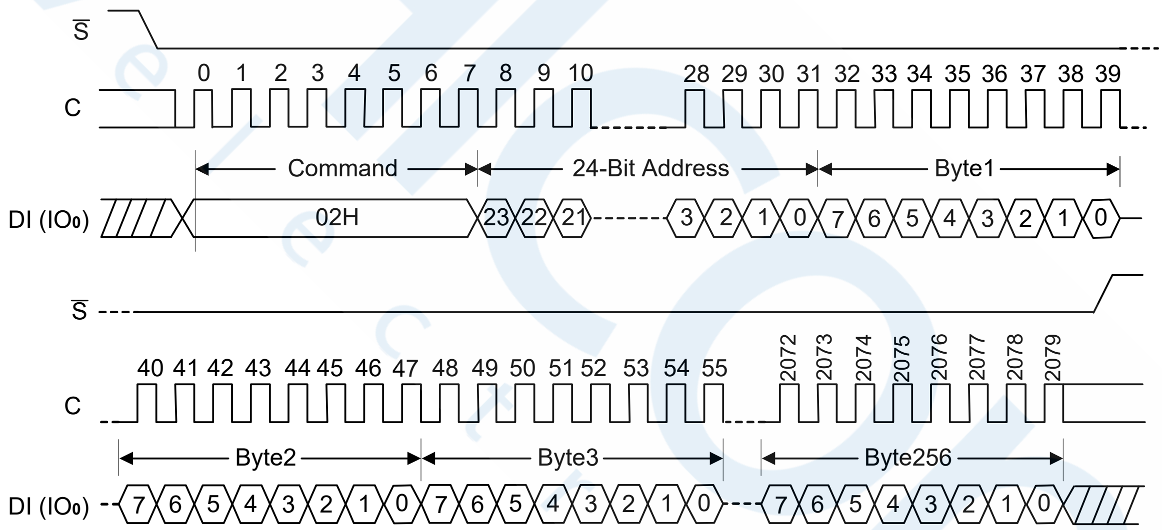
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving $\overline{S}$ Low, followed by the command code, three address Bytes and at least one data Byte on DI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). $\overline{S}$ must be driven low for the entire duration of the sequence. The Page Program command sequence: $\overline{S}$ goes low → sending Page Program command → 3-Byte address on DI → at least 1 Byte data on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 11. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. $\overline{S}$ must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as $\overline{S}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 11. Page Program Sequence Diagram

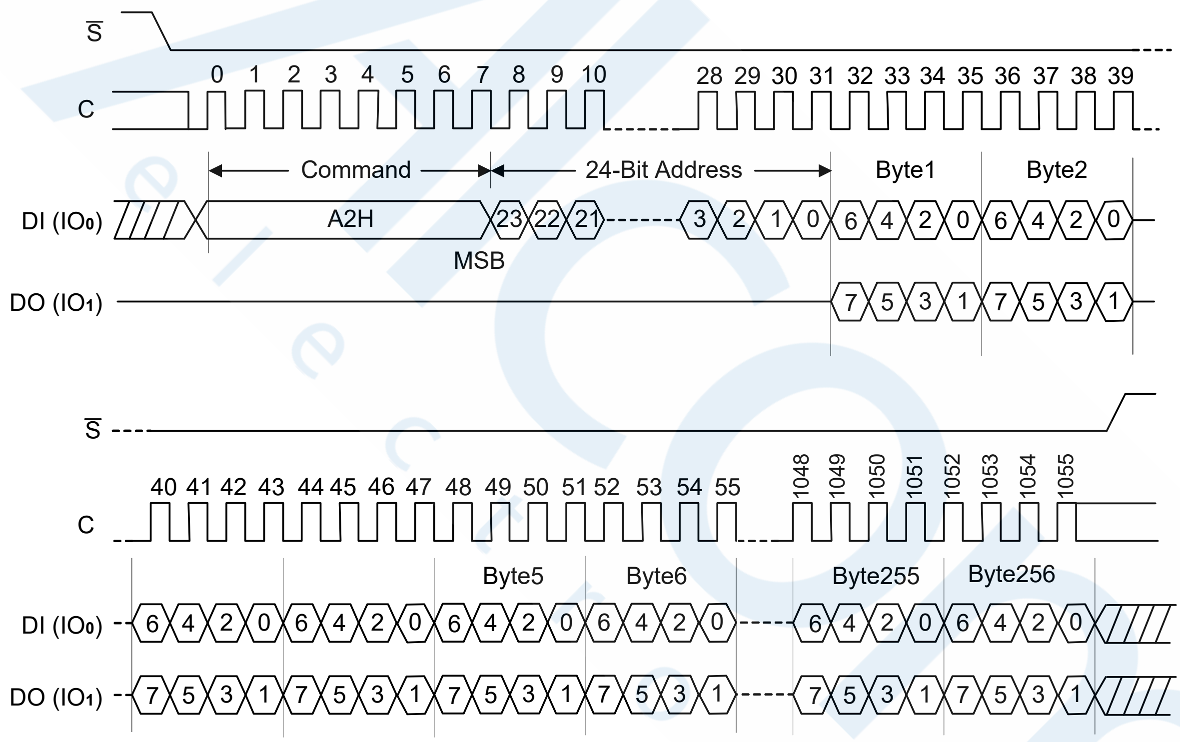


Dual Input Page Program (A2H)

The Dual Input Page Program command is for programming the memory using two pins: IO_0, IO_1. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Dual Input Page Program command. The quad Page Program command is entered by driving $\overline{S}$ Low, followed by the command code (A2H), three address Bytes and at least one data Byte on IO pins.
The command sequence is shown in Figure 12. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. $\overline{S}$ must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Dual Input Page Program command is not executed.

As soon as $\overline{S}$ is driven high, the self-timed Dual Input Page Program cycle (whose duration is t_{PP}) is initiated. While the Dual Input Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Dual Input Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Dual Input Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 12. Dual input Page Program Sequence Diagram

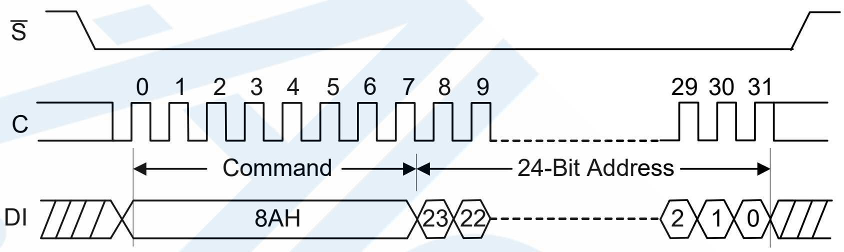


0.5KB Sector Erase (SE05K) (8AH)

The Sector Erase 0.5K (SE05K) command is used to erase all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase 0.5K (SE05K) command is entered by driving $\overline{S}$ low, followed by the command code, and 3-address Byte on DI. Any address inside the sector is a valid address for the Sector Erase 0.5K (SE05K) command. $\overline{S}$ must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: $\overline{S}$ goes low → sending Sector Erase command → 3-Byte address on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 13. $\overline{S}$ must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase 0.5K (SE05K) command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase 0.5K (SE05K) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit (see Table1 & 1a) is not executed.

Figure 13. 0.5K Sector Erase Sequence Diagram

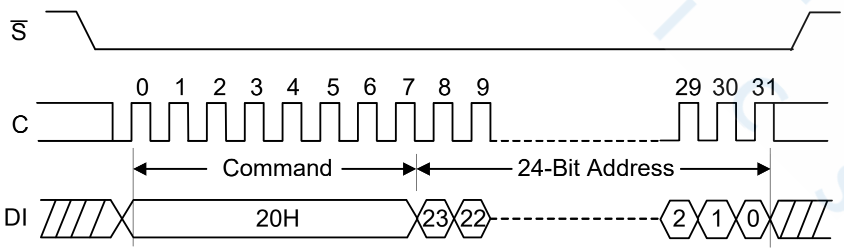


Sector Erase (SE) (20H)

The Sector Erase (SE) command is used to erase all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving $\overline{S}$ low, followed by the command code, and 3-address Byte on DI. Any address inside the sector is a valid address for the Sector Erase (SE) command. $\overline{S}$ must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: $\overline{S}$ goes low → sending Sector Erase command → 3-Byte address on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 14. $\overline{S}$ must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit (see Table1 & 1a) is not executed.

Figure 14. Sector Erase Sequence Diagram

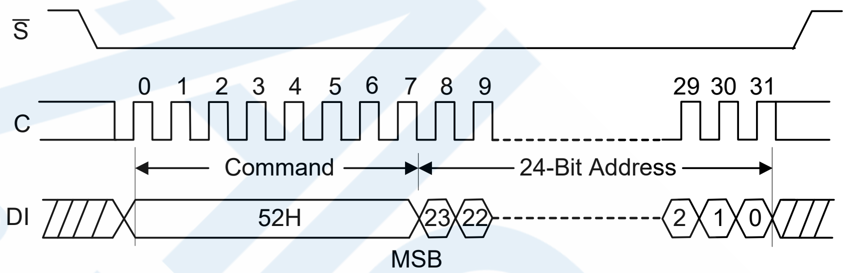


32KB Block Erase (BE32) (52H)

The 32KB Block Erase (BE32) command is used to erase all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE32) command is entered by driving $\overline{S}$ low, followed by the command code, and three address Bytes on DI. Any address inside the block is a valid address for the 32KB Block Erase (BE32) command. $\overline{S}$ must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: $\overline{S}$ goes low → sending 32KB Block Erase command → 3-Byte address on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 15. $\overline{S}$ must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 32KB Block Erase (BE32) command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE32) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits (see Table1 & 1a) is not executed.

Figure 15. 32KB Block Erase Sequence Diagram

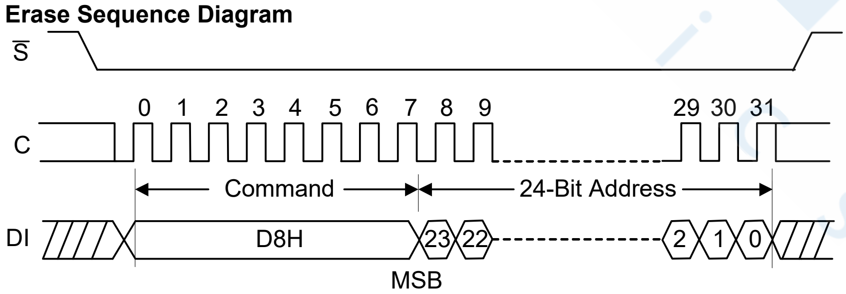


64KB Block Erase (BE64) (D8H)

The 64KB Block Erase (BE64) command is used to erase all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE64) command is entered by driving $\overline{S}$ low, followed by the command code, and three address Bytes on DI. Any address inside the block is a valid address for the 64KB Block Erase (BE64) command. $\overline{S}$ must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: $\overline{S}$ goes low → sending 64KB Block Erase command → 3-Byte address on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 16. $\overline{S}$ must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 64KB Block Erase (BE64) command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE64) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits (see Table1 & 1a) is not executed.

Figure 16. 64KB Block Erase Sequence Diagram

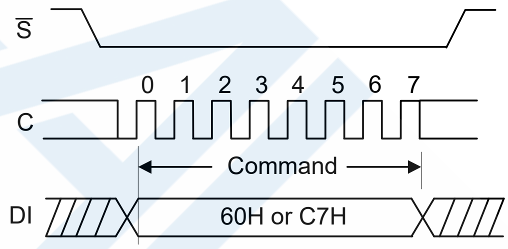


Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is used to erase all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving $\overline{S}$ Low, followed by the command code on Serial Data Input (DI). $\overline{S}$ must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: $\overline{S}$ goes low → sending Chip Erase command → $\overline{S}$ goes high. The command sequence is shown in Figure 17. $\overline{S}$ must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 17. Chip Erase Sequence Diagram



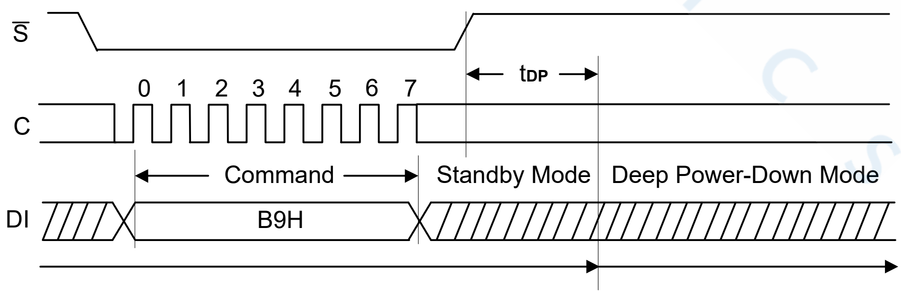
Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving $\overline{S}$ high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. These commands can release the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from deep power down mode, also allows the Device ID of the device to be output on DO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power- Up.

The Deep Power-Down command sequence: $\overline{S}$ goes low → sending Deep Power-Down command → $\overline{S}$ goes high. The command sequence is shown in Figure 18. $\overline{S}$ must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as $\overline{S}$ is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 18. Deep Power-Down Sequence Diagram



Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. When Chip Select ($\overline{S}$) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES2}(max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.
RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/ write cycle in progress.
The RES instruction is ended by $\overline{S}$ goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on C while $\overline{S}$ is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and $\overline{S}$ must remain to high at least t_{RES2} (max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.
The RDP instruction is for releasing from Deep Power-Down Mode.

Figure 19. Release Power-Down/Read Device ID Sequence Diagram

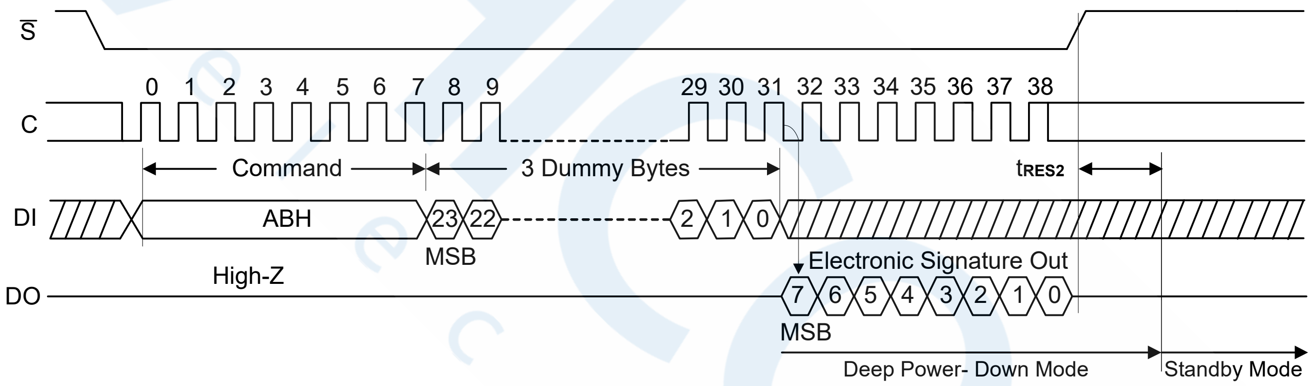
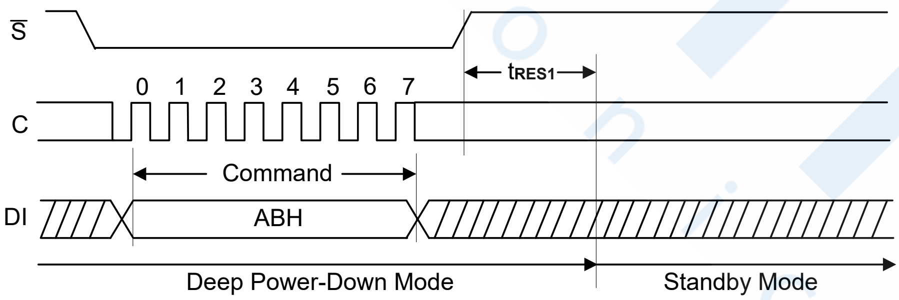


Figure 20. Release Power-Down Sequence Diagram

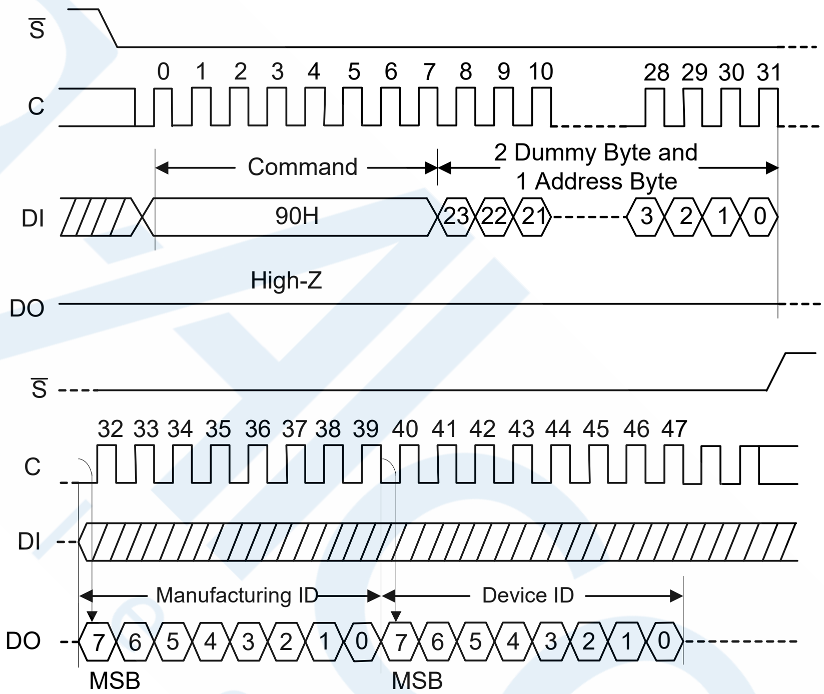


Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the $\overline{S}$ pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of C with most significant bit (MSB) first as shown in Figure 21. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 21. Read Manufacture ID/ Device ID Sequence Diagram

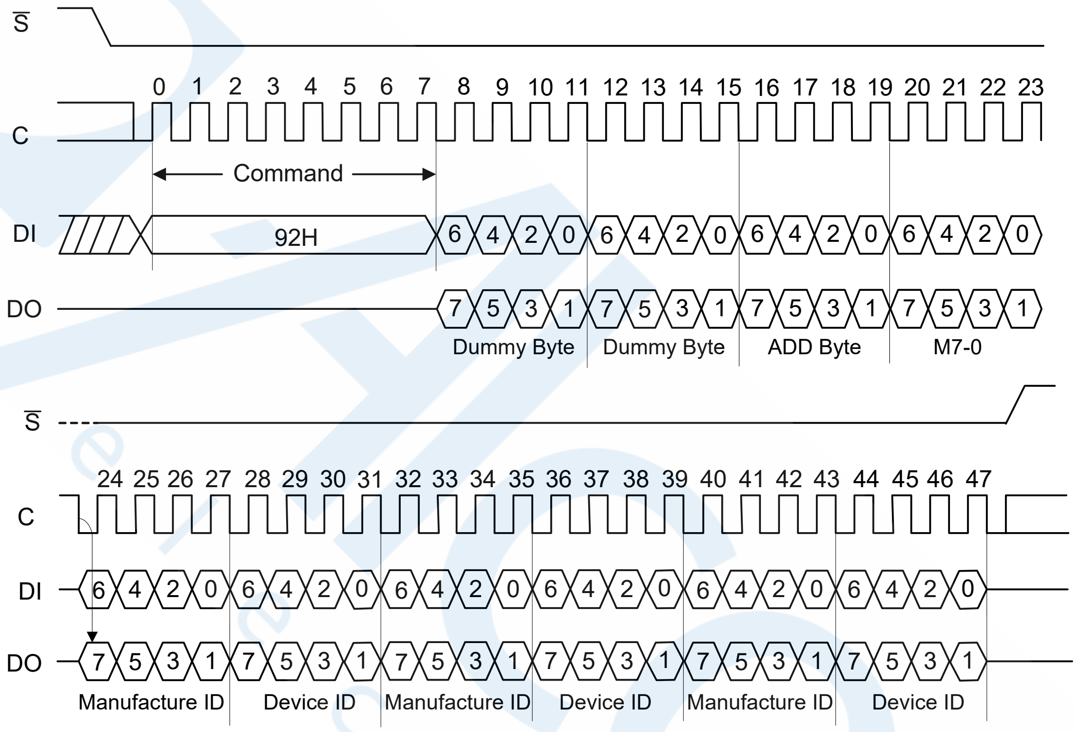


Dual I/O Read Electronic Manufacturer ID/ Device ID (92H)

The Dual I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the $\overline{S}$ pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of C with most significant bit (MSB) first as shown in Figure 22. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 22. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram

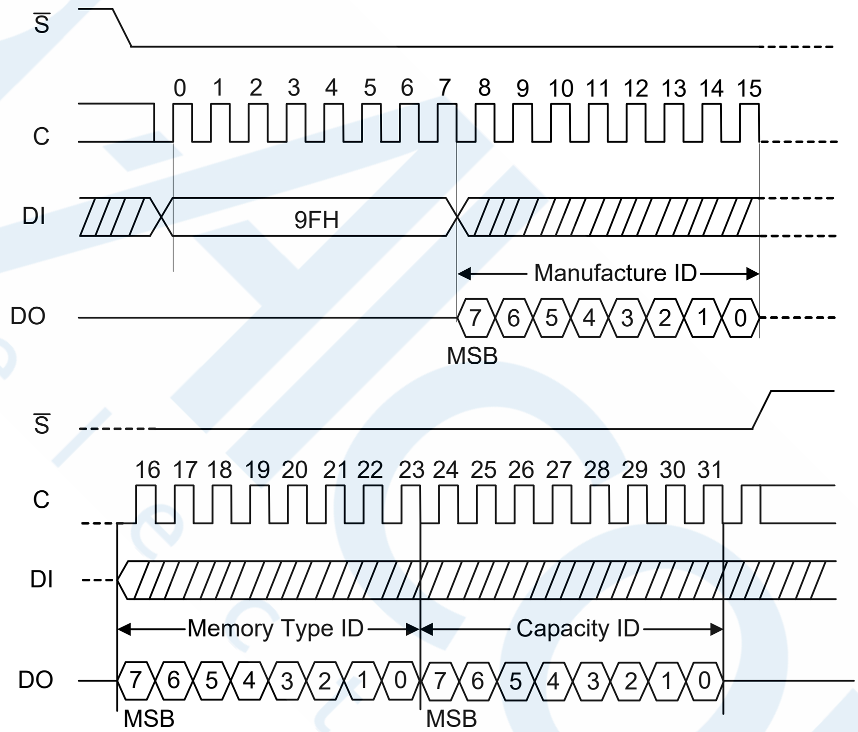


Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two Bytes of device identification. The device identification indicates the memory type in the first Byte, and the memory capacity of the device in the second Byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving $\overline{S}$ low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, each bit is shifted out on the falling edge of Serial Clock. The command sequence is shown in Figure 23. The Read Identification (RDID) command is terminated by driving $\overline{S}$ high at any time during data output. When $\overline{S}$ is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

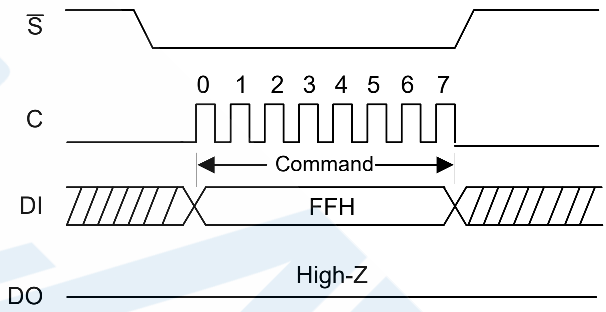
Figure 23. Read Identification ID Sequence Diagram



Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, "Continuous Read Mode" bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.
Because the A25L040B has no hardware reset pin, so if Continuous Read Mode bits are set to "AXH", the A25L040B will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the "AXH" state and allow standard SPI command to be recognized. The command sequence is show in Figure 24.

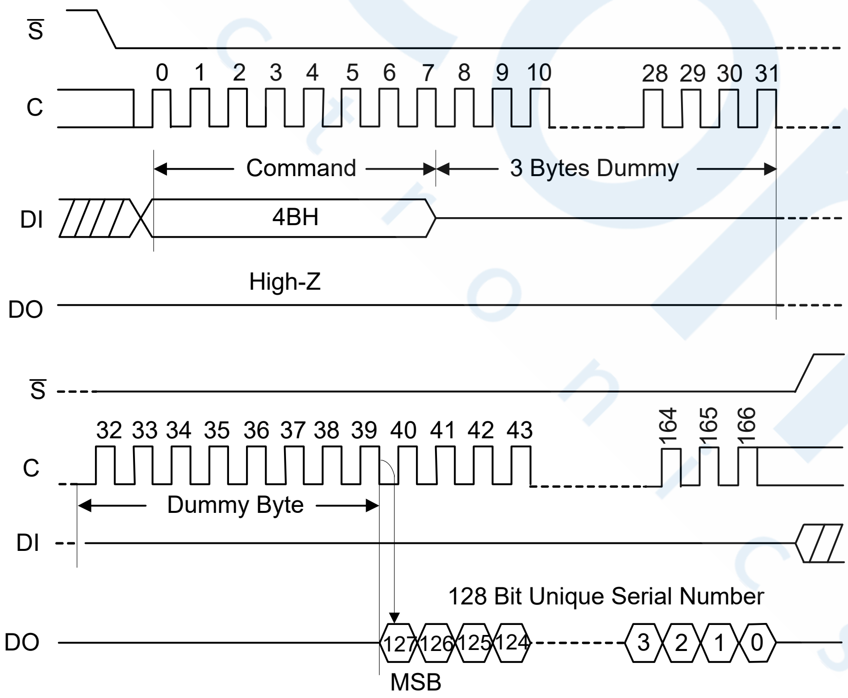
Figure 24. Continuous Read Mode Reset Sequence Diagram



Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each A25L040B device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command sequence: $\overline{S}$ goes low → sending Read Unique ID command → Dummy Byte1 → Dummy Byte2 → Dummy Byte3 → Dummy Byte4 → 128bit Unique ID Out → $\overline{S}$ goes high. The command sequence is show below.

Figure 25. Read Unique ID Sequence Diagram

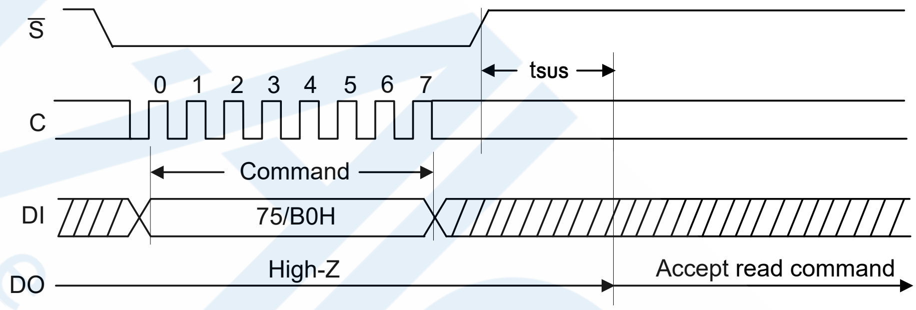


Program/Erase Suspend (PES) (75/B0H)

The Program/Erase Suspend command "75/B0H", allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H) and Erase/Program Security Registers command (44H,42H) and Erase commands (8AH, 20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program suspend. The Write Status Register command (01H) and Erase Security Registers command (44H) and Erase commands (8AH, 20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS2/SUS1 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS2/SUS1 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS2/SUS1 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show in Figure 26.

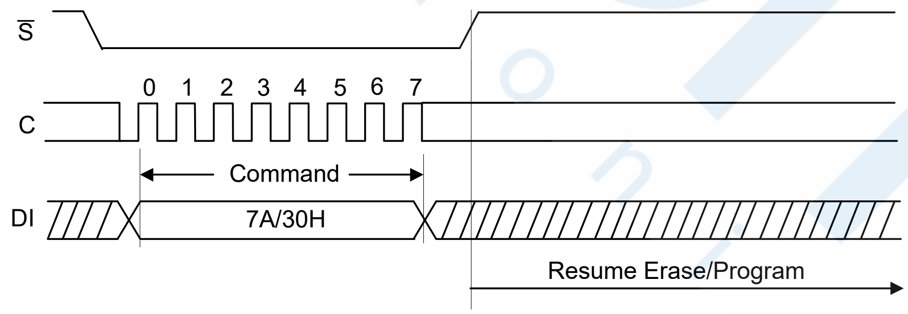
Figure 26. Program/Erase Suspend Sequence Diagram



Program/Erase Resume (PER) (7A/30H)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS2/SUS1 bit equal to 1 and the WIP bit equal to 0. After issued the SUS2/ SUS1 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure 27.

Figure 27. Program/Erase Resume Sequence Diagram



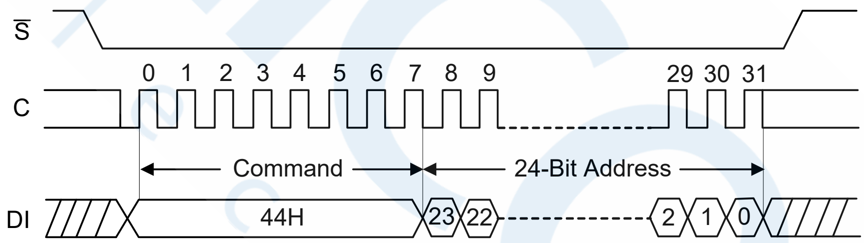
Erase Security Registers (44H)

The A25L040B provides three 512-Byte Security Registers which can be read and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.
The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: $\overline{S}$ goes low → sending Erase Security Registers command → 3-Byte address on DI → $\overline{S}$ goes high. The command sequence is shown in Figure 28. $\overline{S}$ must be driven high after the eighth bit of the last byte of address has been latched in, otherwise the Erase Security Registers command is not executed. As soon as $\overline{S}$ is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB3-1 bits is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A9	A8-A0
Security Registers #1	00H	0001	0	Byte Address
Security Registers #2	00H	0010	0	Byte Address
Security Registers #3	00H	0011	0	Byte Address

Figure 28. Erase Security Registers Command Sequence Diagram

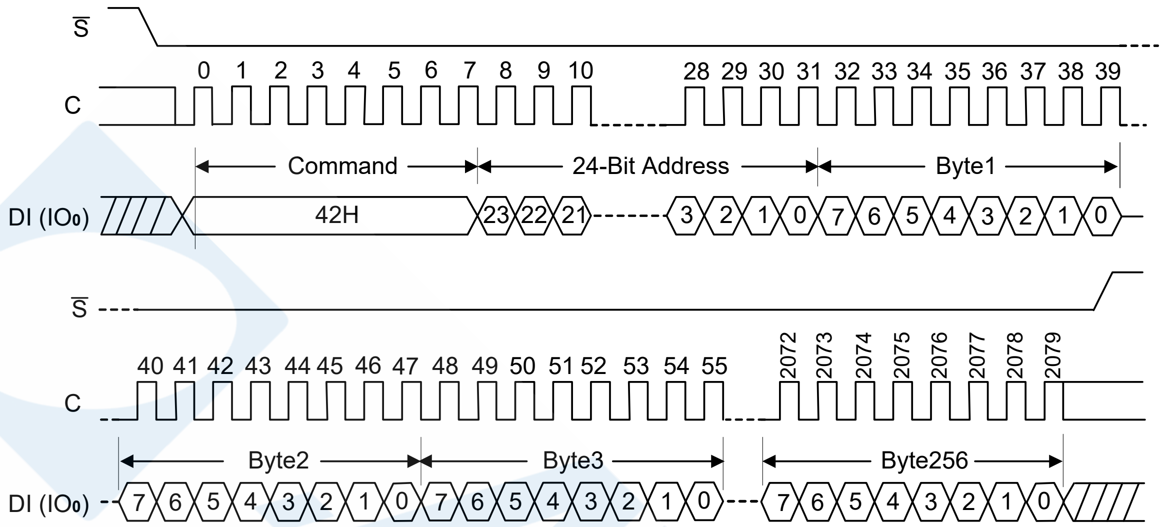


Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving $\overline{S}$ Low, followed by the command code (42H), three address Bytes and at least one data Byte on DI. As soon as $\overline{S}$ is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A9	A8-A0
Security Registers #1	00H	0001	0	Byte Address
Security Registers #2	00H	0010	0	Byte Address
Security Registers #3	00H	0011	0	Byte Address

Figure 29. Program Security Registers Command Sequence Diagram

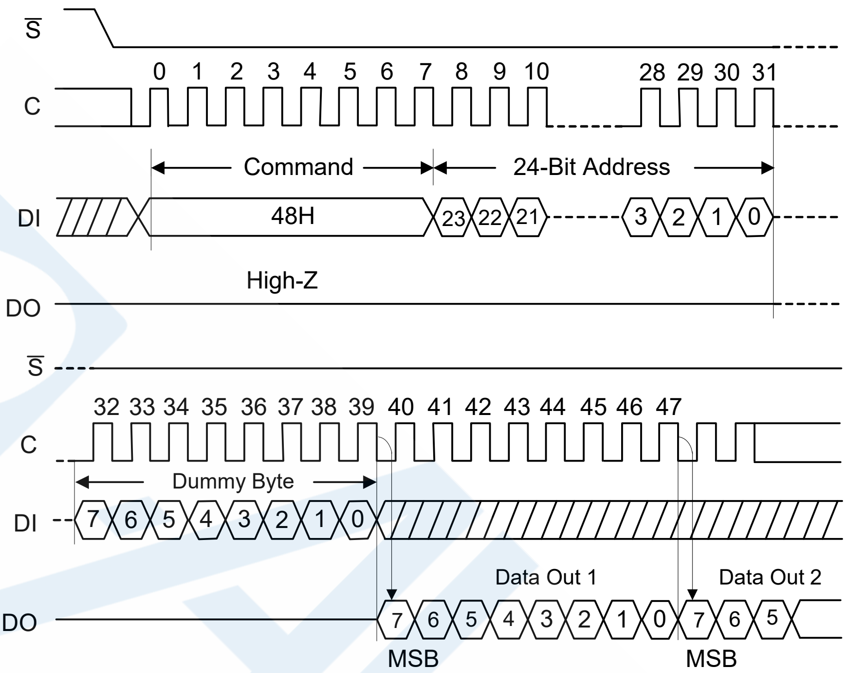


Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-Byte address (A23-A0) and a dummy Byte, and each bit is latched-in on the rising edge of C. Then the memory content, at that address, is shifted out on DO, and each bit is shifted out, at a Max frequency fc, on the falling edge of C. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. Once the A8-A0 address reaches the last Byte of the register (Byte 1FFH), it will reset to 000H, the command is completed by driving $\overline{S}$ high.

Address	A23-A16	A15-A12	A11-A9	A8-A0
Security Registers #1	00H	0001	0	Byte Address
Security Registers #2	00H	0010	0	Byte Address
Security Registers #3	00H	0011	0	Byte Address

Figure 30. Read Security Registers Command Sequence Diagram

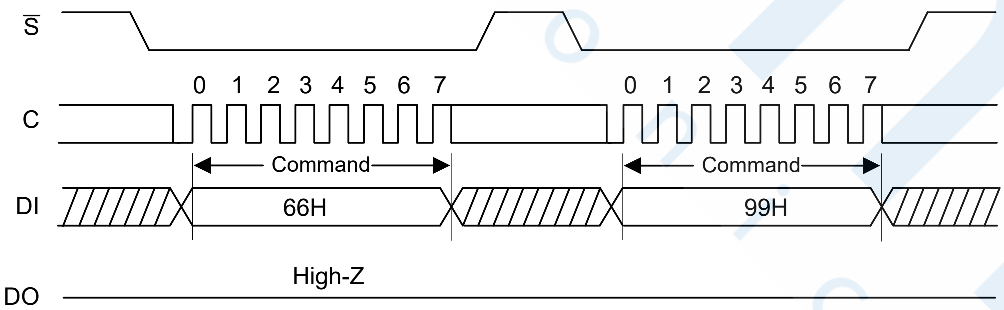


Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Continuous Read Mode bit setting (M7- M0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: $\overline{S}$ goes low → Sending Enable Reset command → $\overline{S}$ goes high → $\overline{S}$ goes low → Sending Reset command → $\overline{S}$ goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} = 30us / 120us / 4ms to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 31. Enable Reset and Reset Command Sequence Diagram



Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure 32. Read Serial Flash Discoverable Parameter Command Sequence Diagram

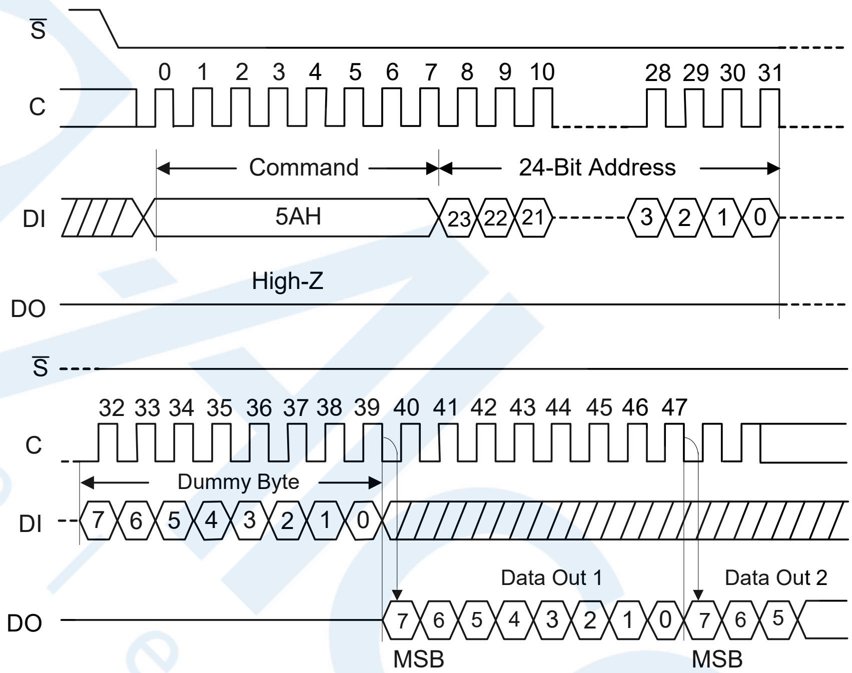


Table 3. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	06H	06H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	06H	06H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (AMIC Device Manufacturer ID)	It indicates AMIC Device manufacturer ID	10H	07:00	37H	37H
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of AMIC Device Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table 4. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing toVolatile Status Registers	0: Nonvolatile status bit; 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	91H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	0b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	0b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	003FFFFFH	
(1-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00000b	00H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	000b	
(1-4-4) Fast Read Opcode		39H	15:08	FFH	FFH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	00000b	00H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	FFH	FFH
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00000b	80H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	100b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	52H	23:16	09H	09H
Sector Type 4 erase Opcode		53H	31:24	8AH	8AH

Table 5. Parameter Table (1): Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
VCC Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
VCC Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2300H=2.300V 2700H=2.700V	63H:62H	31:16	2300H	2300H
HW RESET pin	0=not support 1=support	65H:64H	00	0b	799CH
HW HOLD pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		66H	23:16	FFH	FFH
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B & 16B 32H:8B & 16B & 32B 64H:8B & 16B & 32B & 64B	67H	31:24	00H	00H
Individual block lock	0=not support 1=support	6BH:68H	00	0b	CBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

ELECTRICAL CHARACTERISTICS

Power On/Down and Voltage Drop Timing

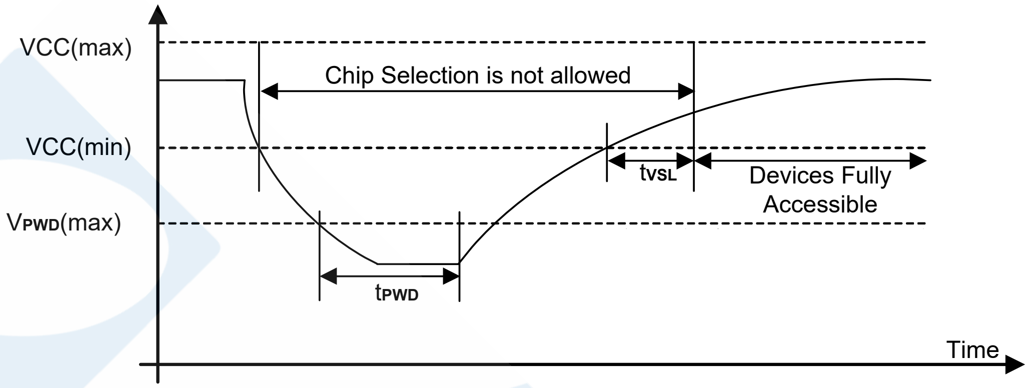


Table 6. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initializationwill occur		1	V
t_{PWD}	The minimum duration for ensuring initialization will occur	300		μs
t_{VSL}	VCC (min) To $\overline{S}$ Low	50	500	μs
V_{WI}	Write Inhibit Voltage	1.5	2.2	V

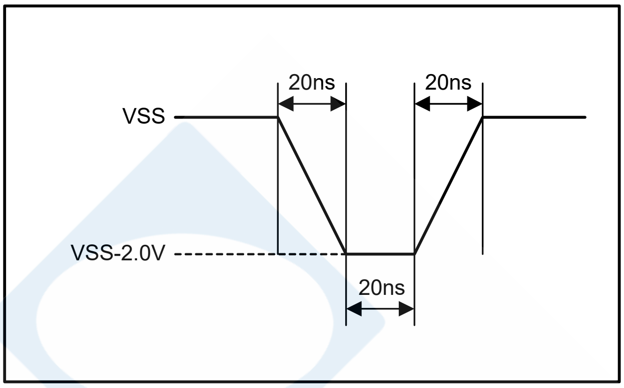
INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each Byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

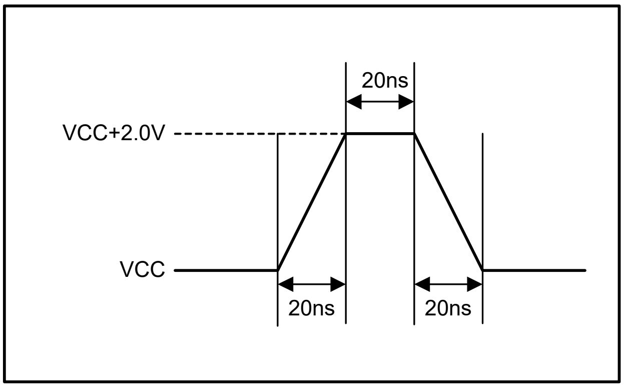
ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
Transient Input / Output Voltage(note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V

Figure 33. Maximum Negative and Positive Overshoot Waveform



Maximum Negative Overshoot Waveform

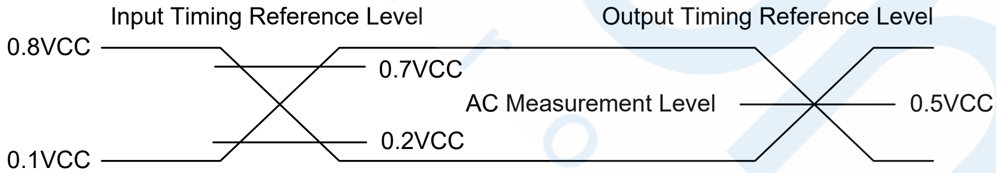


Maximum Positive Overshoot Waveform

CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance			6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			8	pF	V_{OUT}=0V
C_L	Load Capacitance	30			pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 34: Input Test Waveform and Measurement Level



Note: Input pulse rise and fall time are < 5ns

DC CHARACTERISTICS

(T_A = -40°C ~ +85°C, VCC= 2.3V ~ 3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	$\overline{S}$=VCC, V_{IN}=VCC or VSS		8		μA
I_{CC2}	Deep Power-Down Current	$\overline{S}$=VCC, V_{IN}=VCC or VSS		0.6	3.5	μA
I_{CC3}	Operating Current (0B Read)	CLK=0.1VCC / 0.9VCC at 104MHz		3.5	4.4	mA
		CLK=0.1VCC /0.9VCC at 80MHz		2.8	3.4	mA
I_{CC4}	Operating Current (PP)	$\overline{S}$=VCC			1.4	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S}$=VCC			1.4	mA
I_{CC6}	Operating Current (SE)	$\overline{S}$=VCC			1.0	mA
I_{CC7}	Operating Current (BE)	$\overline{S}$=VCC			1.0	mA
I_{CC8}	Operating Current (CE)	$\overline{S}$=VCC			1.2	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} =100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note:
1. Typical values given for T_A=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

AC CHARACTERISTICS

(T_A = -40°C ~ +85°C, VCC= 2.3V ~ 3.6V, C_L= 30pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency For: Dual I/O(BBH), on 2.7V-3.6V power supply			104	MHz
	Serial Clock Frequency For: Dual I/O(BBH), on 2.3V-2.7V power supply			85	MHz
f_{R1}	Serial Clock Frequency For: Read (03H)			33	MHz
t_{CLH}	Serial Clock High Time	4.5			ns
t_{CLL}	Serial Clock Low Time	4.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	$\overline{S}$ Active Setup Time	5			ns
t_{CHSH}	$\overline{S}$ Active Hold Time	5			ns
t_{SHCH}	$\overline{S}$ Not Active Setup Time	5			ns
t_{CHSL}	$\overline{S}$ Not Active Hold Time	5			ns
t_{SHSL}	$\overline{S}$ High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before $\overline{S}$ Low	20			ns
t_{SHWL}	Write Protect Hold Time After $\overline{S}$ High	100			ns
t_{DP}	$\overline{S}$ High To Deep Power-Down Mode			25	µs
t_{RES1}	$\overline{S}$ High To Standby Mode Without Electronic Signature Read			25	µs
t_{RES2}	$\overline{S}$ High To Standby Mode With Electronic Signature Read			25	µs
t_{SUS}	$\overline{S}$ High To Next Command After Suspend			20	µs
t_{RS}	Latency Between Resume And Next Suspend	100			µs
t_{RST}	$\overline{S}$ High To Next Command After Reset (Except From WRSR, Chip Erase)			30	µs
	$\overline{S}$ High To Next Command After Reset (From Chip Erase)			120	µs
	$\overline{S}$ High To Next Command After Reset (From WRSR)			4	ms
t_W	Write Status Register Cycle Time		3.5	4	ms
t_{BP1}	Byte Program Time (First Byte)		60	75	µs
t_{BP2}	Additional Byte Program Time (After First Byte)		10	15	µs
t_{PP}	Page Programming Time		1.5	2	ms
t_{SE}	Sector Erase Time (4K Bytes)		3.5	8	ms
t_{BE1}	Block Erase Time (32K Bytes)		3.5	8	ms
t_{BE2}	Block Erase Time (64K Bytes)		3.5	8	ms
t_{CE}	Chip Erase Time (A25L040B)		6	10	ms

Note:
1. Typical values given for T_A=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 35. Serial Input Timing

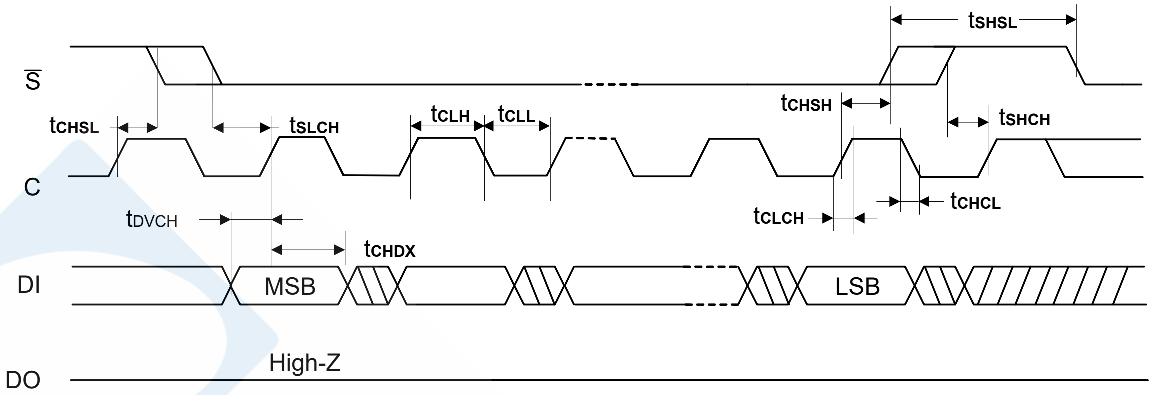


Figure 36. Output Timing

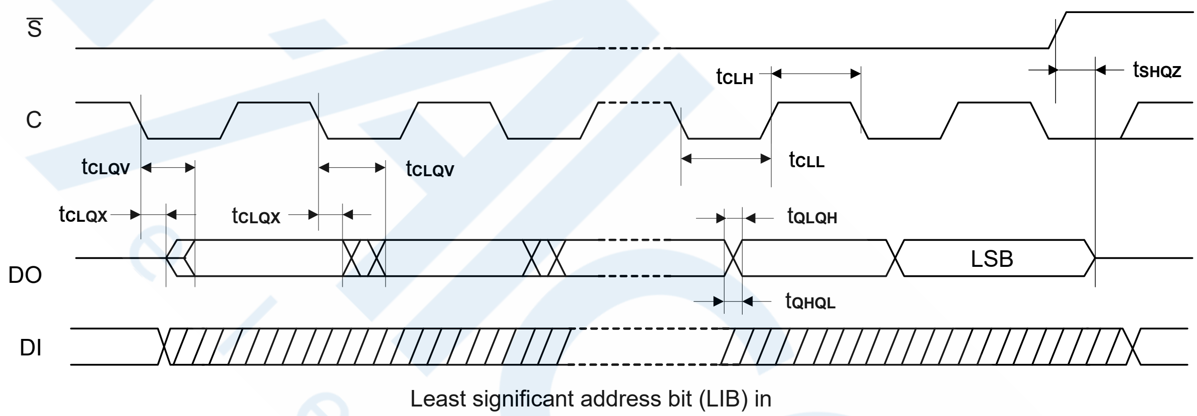


Figure 37. Resume to Suspend Timing Diagram

Part Numbering Scheme

A25 X XXX X X – X / X

Packing
- Blank: for DIP8
- G: for SOP8 In Tube
- Q: for Tape & Reel

Package Material
- Blank: normal
- F: PB free

Package Type
- Blank = 300 mil DIP8
- M = 209 mil SOP 8
- O = 150 mil SOP 8
- Q1 = USON 8 (2*3)
- Q4 = WSON 8 (6*5mm)

Device Version
- B = B Version

Device Density
- 040 = 4 Mbit (4KB uniform sectors)

Device Voltage
- L = 2.7-3.6V

Device Type
- A25 = AMIC Serial Flash

Ordering Information

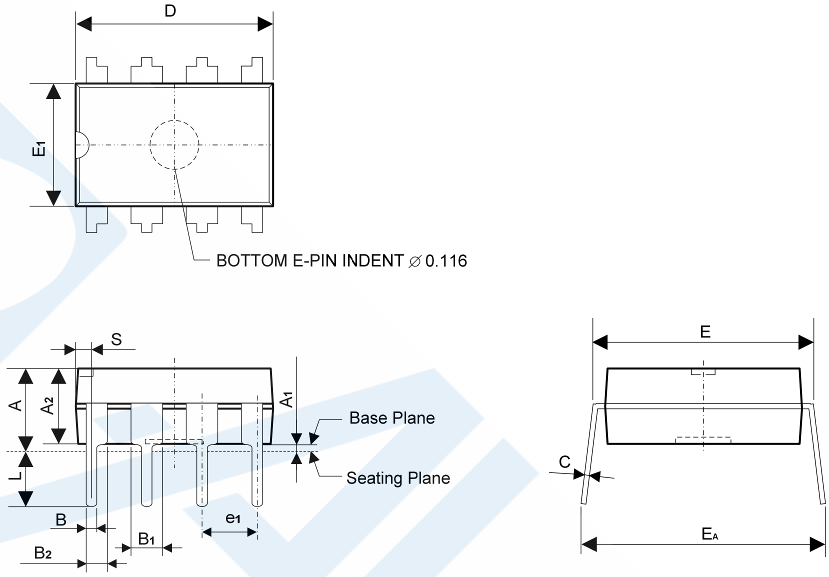
Part No.	Speed (MHz)	Active Read Current Max. (mA)	Program/Erase Current Max. (mA)	Standby Current Max. (μA)	Package
A25L040B-F	104	3.7	1.3	8	8 Pin Pb-Free DIP (300 mil)
A25L040BO-F					8 Pin Pb-Free SOP (150mil)
A25L040BM-F					8 Pin Pb-Free SOP (209mil)
A25L040BQ1-F					8 Pin Pb-Free USON (2*3mm)
A25L040BQ4-F					8 Pin Pb-Free WSON (6*5mm)

Operating temperature range: -40°C ~ +85°C.

Package Information

P-DIP 8L Outline Dimensions

unit: inches/mm

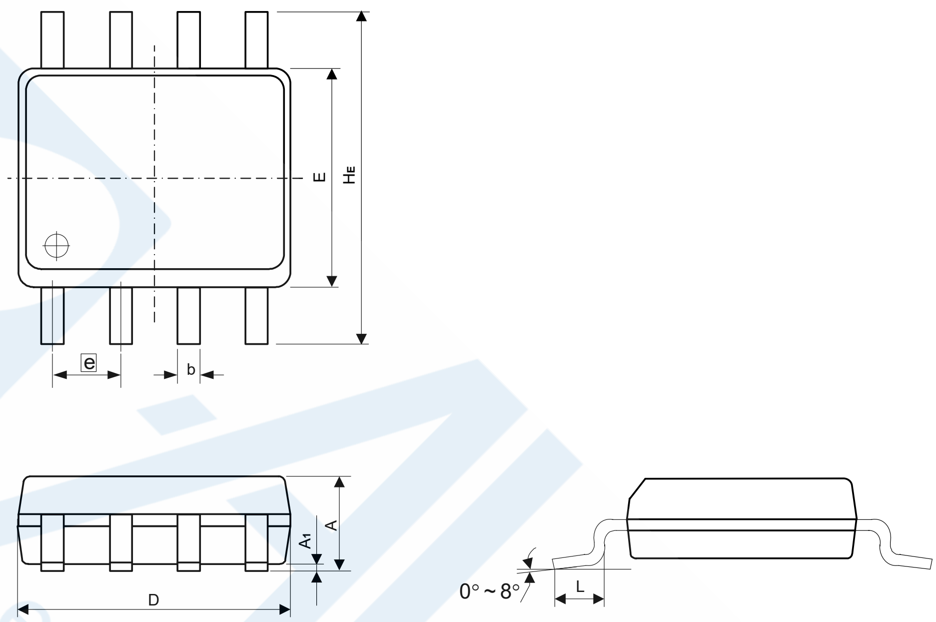


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.180	-	-	4.57
A_1	0.015	-	-	0.38	-	-
A_2	0.128	0.130	0.136	3.25	3.30	3.45
B	0.014	0.018	0.022	0.36	0.46	0.56
B_1	0.050	0.060	0.070	1.27	1.52	1.78
B_2	0.032	0.039	0.046	0.81	0.99	1.17
C	0.008	0.010	0.013	0.20	0.25	0.33
D	0.350	0.360	0.370	8.89	9.14	9.40
E	0.290	0.300	0.315	7.37	7.62	8.00
E_1	0.254	0.260	0.266	6.45	6.60	6.76
e_1	-	0.100	-	-	2.54	-
L	0.125	-	-	3.18	-	-
E_A	0.345	-	0.385	8.76	-	9.78
S	0.016	0.021	0.026	0.41	0.53	0.66

Notes:
1. Dimension D and E_1 do not include mold flash or protrusions.
2. Dimension B_1 does not include dambar protrusion.
3. Tolerance: ±0.010” (0.25mm) unless otherwise specified.

Package Information

SOP 8L (150mil) Outline Dimensions unit: mm



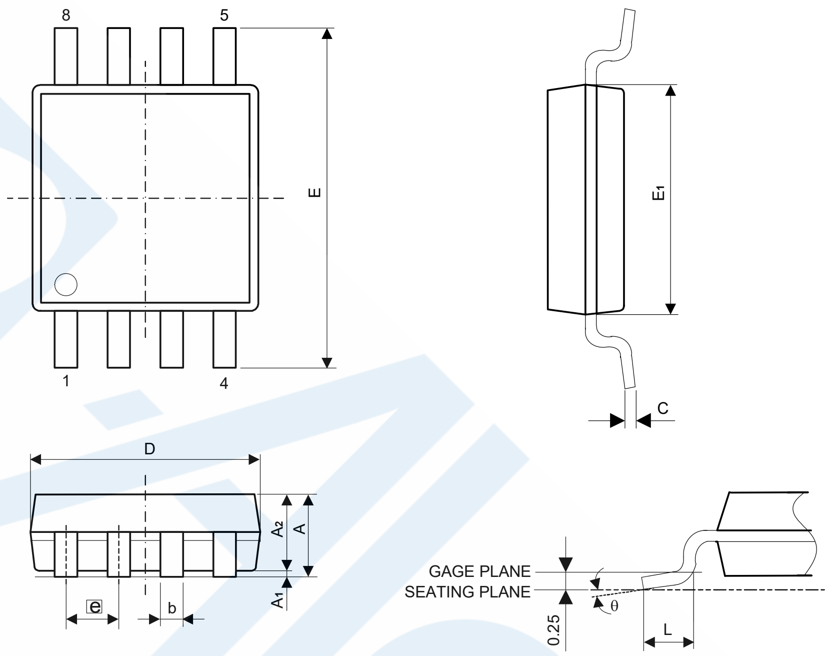
Symbol	Dimensions in mm
A	1.35~1.75
A1	0.10~0.25
b	0.33~0.51
D	4.7~5.0
E	3.80~4.00
e	1.27 BSC
HE	5.80~6.20
L	0.40~1.27

Notes:
1. Maximum allowable mold flash is 0.15mm.
2. Complies with JEDEC publication 95 MS –012 AA.
3. All linear dimensions are in millimeters (max/min).
4. Coplanarity: Max. 0.1mm

Package Information

SOP 8L (209mil) Outline Dimensions

unit: mm

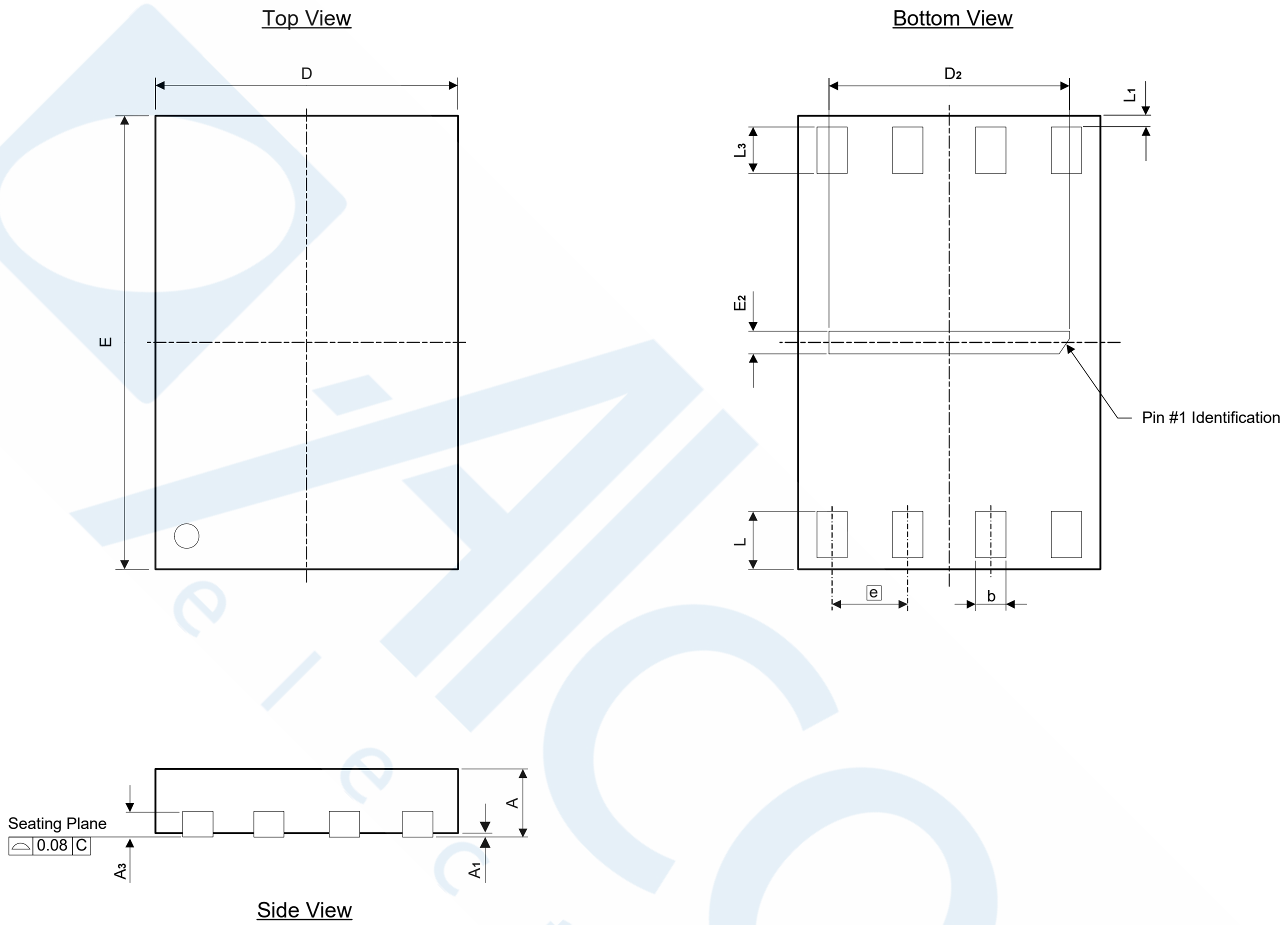


Symbol	Dimensions in mm		
	Min	Nom	Max
A	1.75	1.95	2.16
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.91
b	0.35	0.42	0.48
C	0.19	0.20	0.25
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.18	5.28	5.38
e	1.27 BSC		
L	0.50	0.65	0.80
θ	0°	-	8°

Notes:
Maximum allowable mold flash is 0.15mm at the package ends and 0.25mm between leads

Package Information

USON 8L (2 X 3 X 0.45mm) Outline Dimensions unit: mm

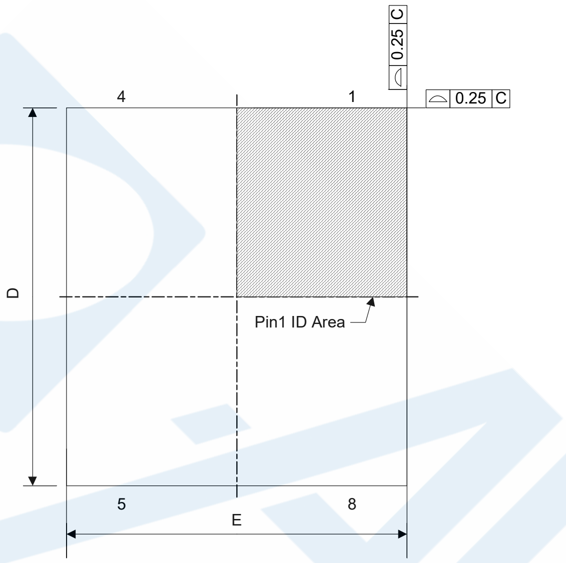


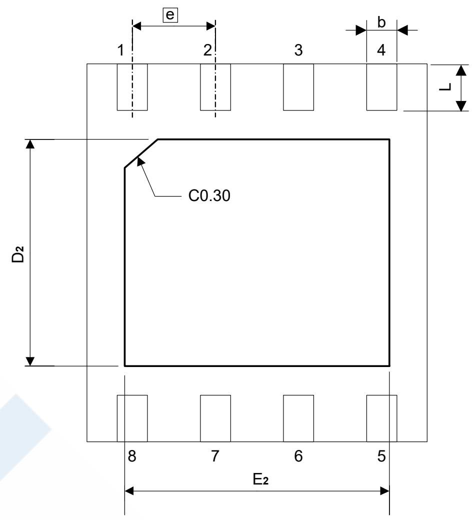
Symbol	Dimensions in mm		
	Min	Nom	Max
A	0.40	0.45	0.50
A_1	0	0.02	0.05
A_3	0.20 REF.		
D	1.90	2.00	2.10
D_2	1.45	1.55	1.65
E	2.90	3.00	3.10
E_2	0.10	0.20	0.30
e	0.50 BASIC		
b	0.20	0.25	0.30
L	0.40	0.45	0.50
L_1	0.10 REF.		
L_3	0.30	0.35	0.40

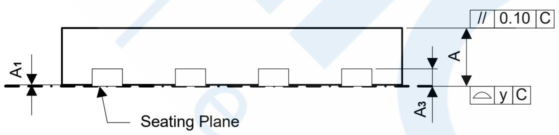
Package Information

WSON 8L (6 X 5 X 0.8mm) Outline Dimensions

unit: mm/mil







Symbol	Dimensions in mm			Dimensions in mil		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	27.6	29.5	31.5
A_1	0.000	0.020	0.050	0.0	0.8	2.0
A_3	0.203 REF			8.0 REF		
b	0.350	0.400	0.480	13.8	15.8	18.9
D	5.900	6.000	6.100	232.3	236.2	240.2
D_2	3.200	3.400	3.600	126.0	133.9	141.7
E	4.900	5.000	5.100	192.9	196.9	200.8
E_2	3.800	4.000	4.200	149.6	157.5	165.4
L	0.500	0.600	0.750	19.7	23.6	29.5
e	1.270 BSC			50.0 BSC		
y	0	-	0.080	0	-	3.2

Note:

1. Controlling dimension: millimeters
2. Leadframe thickness is 0.203mm (8mil)