CA-IS2092A Isolated RS-485 Transceivers with Integrated DC-DC Converter

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - Data rate is up to 0.5Mbps
  - 1/8 unit load enables up to 256 nodes on the bus
  - 3.0V to 5.5V DC-DC supply voltage range(VDDP)
  - 2.5V to 5.5V RS-485 supply input(VDDL)
- **Integrated DC-DC Converter for Cable-side Power**
  - 3.3V and 5V output options
  - High integration with internal transformer
  - Soft-start reduces input inrush current
  - Overload and short-circuit protection
  - Thermal shutdown
- **Robust Galvanic Isolation of Digital Signals**
  - 2.5kV$_{RMS}$ withstand isolation voltage for 60s (galvanic isolation)
  - ±150kV/μs typical CMTI
  - High lifetime: >40 years
- **Integrated Protection for Robust Communication**
  - ±8kV Human Body Model(HBM) ESD protection on bus I/O
  - True fail-safe guarantees known receiver output state
  - Driver current limit and thermal shutdown
- **Wide operating temperature range: –40°C to 125°C**
- **LGA16 Package**
- **Safety Regulatory Approvals(pending)**
  - 3535V$_{PK}$ V$_{IOTM}$ and 566V$_{PK}$ V$_{IORM}$ per DIN VDE V0884-11:2017-01
  - 2.5kV$_{RMS}$ isolation for 1 minute per UL 1577

2. Applications

- Industrial Automation Equipment
- Solar inverter
- Motor drivers
- Building automation

3. General Description

The CA-IS2092A family of devices is galvanically-isolated RS-485 transceivers with built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. The transceivers have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides up to 2.5kV$_{RMS}$ (60s) of galvanic isolation and ±150kV/μs typical CMTI Isolation improves data communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports. An integrated DC-DC converter generates the 3.3V or 5V operating voltage for the cable-side.

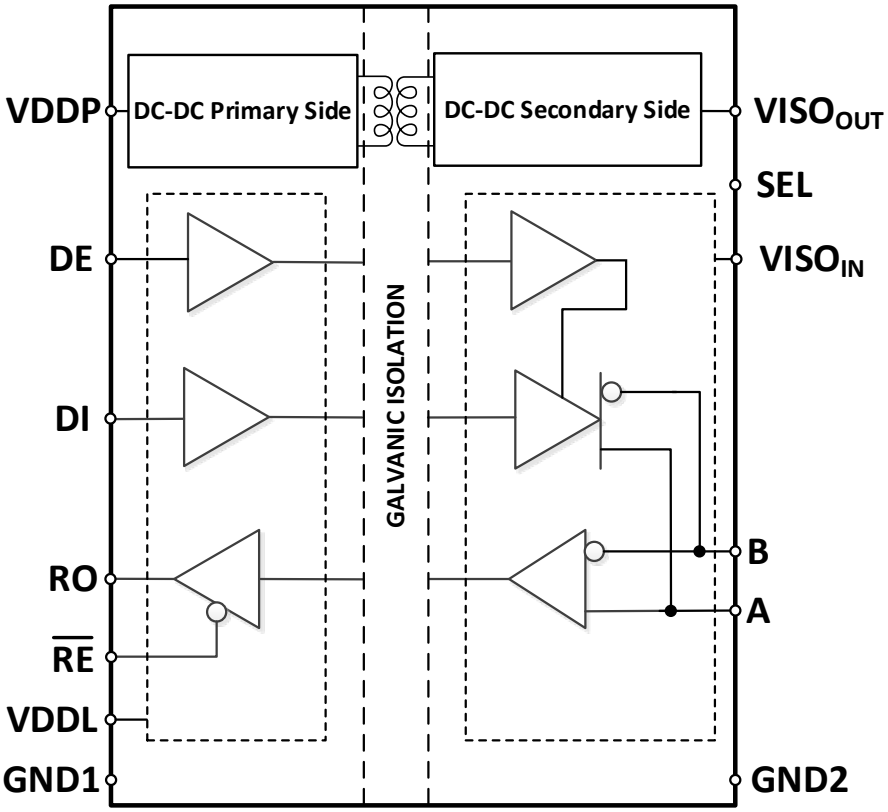
The CA-IS2092A is designed for multi-drop operation with high ESD protection of up to ±8kV Human Body Model (HBM) on the bus pins. The receiver is 1/8-standard-unit load, allowing up to 256 transceivers (loads) on a common bus. The CA-IS2092A provides half-duplex transceivers.This device provides slow slew rate to minimize EMI and reflections, allowing for error-free data transmission up to 0.5Mbps. The individual logic supply input allows fully compatible 2.5V to 5.5V logic on logic input lines.

The CA-IS2092A device is available in LGA16 package and operates over -40°C to +125°C temperature range.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS2092A	LGA16	5.2mm x4.65mm

CA-IS2092A Function Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Full/half duplex	Data Rate (Mbps)	$VISO_{out\_}$ (V)	Package
CA-IS2092A	Half-Duplex	0.5	3.3/5.0	LGA16

Contents

5. Revision History

Revision Number	Description	Page Changed
Version1.00	N/A	N/A

6. Pin Configuration and Description

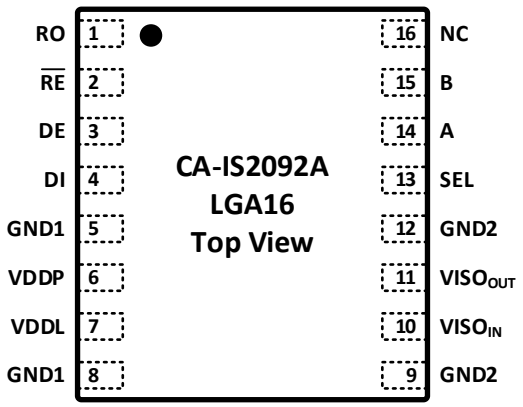


Figure 6-1. CA-IS2092A LGA16 Top View

Table 6-1. CA-IS2092A Pin Description and Functions

Name	Pin Number	Type	Description
RO	1	Digital I/O	Receiver data output.
$\overline{RE}$	2	Digital I/O	Receiver output enable. Drive $\overline{RE}$ low or connect to GND1 to enable receiver. Drive $\overline{RE}$ high to disable receiver. RO is high-impedance when $\overline{RE}$ is high.
DE	3	Digital I/O	Driver output enable. Drive DE high to enable bus driver outputs. Drive DE low or connect to GND1 to disable bus driver outputs. DE has an internal weak pull-down to GND1.
DI	4	Digital I/O	Driver input. With DE high, a logic low on DI forces the noninverting output (A) low and the inverting output (B) high; a logic high on DI forces the noninverting output high and the inverting output low.
GND1	5, 8	GND	Logic-side ground. GND1 is the ground reference for logic-side, pin 5 and pin 8 are connected together internally.
VDDP	6	Power Supply	DC-DC converter supply input.
VDDL	7	Power Supply	Logic-side power input.
GND2	9, 12	GND	Cable-side ground. This is the ground reference for the RS-485 bus signals and DC-DC converter on bus-side. Pin 9 and pin 12 are connected together internally.
$VISO_{IN}$	10	Power Supply	Cable side RS-485 input. Connect $VISO_{IN}$ and $VISO_{OUT}$ together on PCB.
$VISO_{OUT}$	11	Power Supply	Isolated DC-DC power supply output. Cable Side Power supply.
SEL	13	Digital I/O	Output voltage $VISO_{OUT}$,$VISO_{IN}$ select pin: $VISO_{OUT}$ = $VISO_{IN}$ =5.0 V when SEL is shorted to $VISO_{IN}$; $VISO_{OUT}$ = $VISO_{IN}$ =3.3 V when SEL is shorted to GND2 or floating; To improve the system's anti-interference ability, SEL pins do not recommend floating
A	14	Bus I/O	Non-inverting RS-485 receiver input and driver output.
B	15	Bus I/O	Inverting RS-485 receiver input and driver output.
NC	16	-	No internal connection.

7. Specifications

7.1. Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
VDDP, VDDL	Logic-side Supply Voltage[2]	-0.5	6.0	V
$VISO_{OUT}$, $VISO_{IN}$	Cable-side Supply Voltage[2]	-0.5	6.0	V
V_{IO1}	Logic Voltage (DI, DE, $\overline{RE}$, RO)	-0.5	VDDL + 0.5[3]	V
V_{IO2}	Cable-side logic voltage (SEL)	-0.5	$VISO_{IN}$ + 0.5[3]	V
V_{BUS}	Bus voltage A,B	-8	13	V
I_O	Output current on RO	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not be exceed 6V.

7.2. ESD Ratings

PARAMETER			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	Bus pins to GND2	±20	kV
		Other pins on cable-side	±5	
		All pins on logic-side	±6	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]		±2	

7.3. Recommended Operating Conditions

PARAMETER		Min	Typ.	Max	Unit
VDDP[1]	Supply voltage on logic side	3.0	3.3 or 5.0	5.5	V
VDDL	Logic supply voltage	2.5	3.3 or 5.0	5.5	V
V_{OC}	Common mode voltage at bus pins: A, B, Y and Z	-7		12	V
V_{ID}	Differential input voltage V_{AB}	-12		12	V
RL	Differential load resistance	54			Ω
V_{IH}	Input high voltage (DI, DE, $\overline{RE}$ to GND1)	0.7 × VDDL			V
V_{IL}	Input low voltage (DI, DE, $\overline{RE}$ to GND1)			0.3 x VDDL	V
V_{HYS}	Receiver input hysteresis		0.1 x VDDL		
DR	Data rate of the CA-IS2092A			0.5	Mbps
T_A	Ambient Temperature	-40		125	°C

Note:

1. $VISO_{OUT} \leq V_{DDP}$, this means if VDDP = 3.3V, SEL pin must be floating or connected to GND2 and set the $VISO_{out}$ output to 3.3V; if VDDP = 5.0V, there is no connection limit for SEL pin.

7.4. Thermal Information

THERMAL METRIC		CA-IS2092A	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W

7.5. Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			A	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	3.45	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	3.45	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	18	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	3535	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	5000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~3	pF
R_{IO}	Isolation resistance , input to output[5]	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	2500	V_{RMS}

Notes:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6. Safety-Related Certifications (pending)

VDE	UL	TUV
Certified according to DIN V VDE V 0884-11:2017-01 Basic insulation: Maximum transient isolation voltage: 3535V_{pk} Maximum repetitive peak isolation voltage: 566V_{pk} Maximum surge isolation voltage: 5000V_{pk}	Certified according to UL 1577 Component Recognition Program	Basic insulation 2500 V_{RMS} for LGA16 package
Certificate number: pending	Certificate number: pending	Certificate number: CN23RC4J 001

7.7. Electrical Characteristics

7.7.1. Driver

All typical specs are at, VDDL = VDDP, $VISO_{IN}$ = $VISO_{OUT}$, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter		Test Condition	Min	Typ	Max	Unit
$\|V_{OD1}\|$	Driver differential output voltage	I_O = 0mA, unloaded bus. SEL = LOW or float	3	3.3		V
		I_O = 0mA, unloaded bus. SEL = HIGH	4.5	5		
$\|V_{OD2}\|$	Driver differential output voltage	R_L=54Ω, see Figure 8-1, SEL = LOW or float	1.5	2.3		V
		R_L=54Ω,see Figure 8-1, SEL = HIGH	2.1	3.6		
$\|V_{OD3}\|$	Driver differential output voltage with bus load	V_{test} = -7V to 12V, see Figure 8-1	1.5			V
$\Delta\|V_{OD}\|$	Change in differential output voltage between two states	R_L=54Ω, or R_L=100Ω, see Figure 8-1	–0.2		0.2	V
V_{OC}	Common-mode output voltage	R_L=54Ω, or R_L=100Ω, see Figure 8-1	1	$VISO_{IN}$/2	3	V
ΔV_{OC}	Change in steady-state common-mode output voltage between two states	R_L=54Ω, or R_L=100Ω, see Figure 8-1	–0.2		0.2	V
I_{IH}	Hi-Z output leakage current	DI, DE = VDDL	-20		20	μA
I_{IL}	Input leakage current	DI, DE = 0V	-20		20	μA
I_{os}	Short-circuit output current	DE = VDDL, DI = 0V or VDDL, V_A or V_B = –7V	-150		150	mA
		DE = VDDL, DI = 0V or VDDL, V_A or V_B = 12V				
CMTI	Common mode transient immunity	V_{CM} = 1.5kV; See Figure 8-6.	100	150		kV/μs

7.7.2. Receiver

All typical specs are at, VDDL = VDDP, $VISO_{IN}$ = $VISO_{OUT}$, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

	Parameter	Test Condition	Min	Typ.	Max	Unit
V_{OH}	Output logic high voltage	V_{DDL}=5V, I_{OH}=4mA	V_{DDL}-0.4	4.8		V
		V_{DDL}=3.3V, I_{OH}=-4mA	V_{DDL}-0.4	3.1		
V_{OL}	Output logic low voltage	V_{DDL}=5V, I_{OL}=4mA		0.2	0.4	V
		V_{DDL}=3.3V, I_{OL}=4mA		0.2	0.4	
I_{IH}	Input current on $\overline{RE}$ pin	V_{IH} = VDDL	-20		20	μA
I_{IL}	Input current on $\overline{RE}$ pin	V_{IL} = 0V	-20		20	μA
$V_{IT+(IN)}$	Positive-going input threshold voltage			–110	–50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		–200	–140		mV
$V_{I(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B =12V, other inputs = 0 V		75	125	μA
		V_A or V_B =12V, V_{DDL} = 0 V, other inputs = 0 V		80	125	
		V_A or V_B = –7 V, other inputs = 0 V	–100	–40		
		V_A or V_B = –7 V, V_{DDL} = 0 V, other inputs = 0 V	–100	–40		
R_{ID}	Differential input resistance	A, B, -7V < V_{CM} < 12V	96			KΩ
C_D	Differential input capacitance	Sine-wave input, f = 1 MHz, V_I = 0.4×sin(2πft). Measure C_D at A and B pins.		12		pF
C_I	Input capacitance (input to GND1)	VI = 0.4 × sin (2πft), f = 1MHz		18		pF

7.8. Supply Current

All typical specs are at, VDDL = VDDP, $VISO_{IN}$ = $VISO_{OUT}$, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameter	Test Condition		Min	Typ	Max	Unit
V_{ISO} Isolated supply output	I_{ISO} = 0 to 80mA, V_{DDP} = 5V, SEL = $VISO_{IN}$		4.5	5	5.5	V
	I_{ISO} = 0 to 100mA, V_{DDP} = 5V, SEL = GND2		3	3.3	3.6	
	I_{ISO} = 0 to 50mA, V_{DDP} = 3.3V, SEL = GND2		3	3.3	3.6	
$VDDP_{UVLO+}$	VDDP rising		2.5	2.7	2.9	V
$VDDP_{UVLO-}$	VDDP falling		2.1	2.3	2.5	
$VDDP_{UVLO\_HYS}$	VDDP threshold			0.4		
$VDDL_{UVLO+}$	VDDL rising		2.05	2.25	2.45	
$VDDL_{UVLO-}$	VDDL falling		1.9	2.1	2.3	
$VDDL_{UVLO\_HYS}$	VDDL threshold			0.15		
Quiescent current, both driver and receiver enabled ($\overline{RE}$=0V , DE= VDDL , DI= 0V)						
I_{DDP} Supply current on logic side	R_L = NC	VDDP = 3.3V, SEL = GND2		15	20	mA
		VDDP = 5.0V, SEL = GND2		10	15	
		VDDP = 5.0V, SEL = $VISO_{IN}$		15	20	
	R_L = 54Ω	VDDP = 3.3V, SEL = GND2		100	135	
		VDDP = 5.0V, SEL = GND2		80	110	
		VDDP = 5.0V, SEL = $VISO_{IN}$		145	195	
	R_L = 100Ω	VDDP = 3.3V, SEL = GND2		75	90	
		VDDP = 5.0V, SEL = GND2		55	75	
		VDDP = 5.0V, SEL = $VISO_{IN}$		100	130	
	R_L = 120Ω	VDDP = 3.3V, SEL = GND2		60	80	
		VDDP = 5.0V, SEL = GND2		50	65	
		VDDP = 5.0V, SEL = $VISO_{IN}$		85	115	
Average current, both driver and receiver enabled (DE = VDDL, $\overline{RE}$ = 0V), DI input 250kHz square-wave, 50% duty cycle						
I_{DDP} Supply current on logic side	R_L = NC	VDDP = 3.3V, SEL = GND2		20	30	mA
		VDDP = 5.0V, SEL = GND2		20	65	
		VDDP = 5.0V, SEL = $VISO_{IN}$		30	45	
	R_L = 54Ω	VDDP = 3.3V, SEL = GND2		100	135	
		VDDP = 5.0V, SEL = GND2		80	110	
		VDDP = 5.0V, SEL = $VISO_{IN}$		145	200	
	R_L = 100Ω	VDDP = 3.3V, SEL = GND2		75	95	
		VDDP = 5.0V, SEL = GND2		55	80	
		VDDP = 5.0V, SEL = $VISO_{IN}$		110	140	
	R_L = 120Ω	VDDP = 3.3V, SEL = GND2		70	90	
		VDDP = 5.0V, SEL = GND2		50	75	
		VDDP = 5.0V, SEL = $VISO_{IN}$		95	130	

7.9. Switching Characteristics

7.9.1. Driver

All typical specs are at, VDDL = VDDP, $VISO_{IN}$ = $VISO_{OUT}$, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Min	Typ	Max	Unit
t_{PLH},t_{PHL}	Driver Propagation Delay	See Figure 8-2		100	250	ns
t_{PWD}	Driver output skew $\|t_{PLH} - t_{PHL}\|$				20	ns
t_r , t_f	Differential output rise/full time			150	500	ns
t_{PZH},t_{PZL}	Driver enable time	See Figure 8-3		30	100	ns
t_{PHZ},t_{PLZ}	Driver disable time			30	100	ns

7.9.2. Receiver

All typical specs are at, VDDL = VDDP, $VISO_{IN}$ = $VISO_{OUT}$, T_A = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test conditions	Min	Typ	Max	Unit
t_{PLH},t_{PHL}	Receiver propagation delay	See Figure 8-4.		80	150	ns
t_{PWD}	Receiver output skew $\|t_{PLH} - t_{PHL}\|$				8	ns
t_r , t_f	Receiver output rise/full time			2.5	4	ns
t_{PHZ},t_{PLZ}	Receiver disable time	See Figure 8-5.		5	20	ns
t_{PZH},t_{PZL}	Receiver enable time, DE = 0V			5	20	ns

7.10. Typical Operating Characteristics

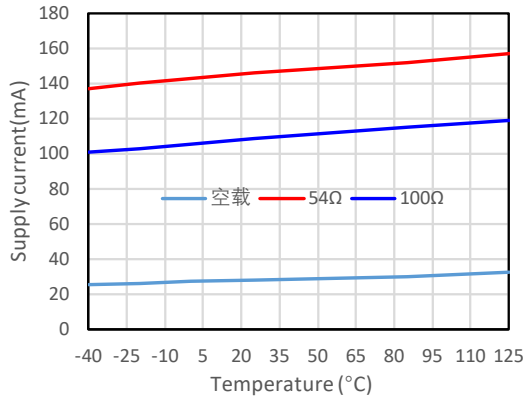


图 7.10-1
Logic-side supply current (I_{CC}) at different bus load
CA-IS2092A，VDDP = 5V，$VISO_{OUT}$ = 5V，DR = 500kbps

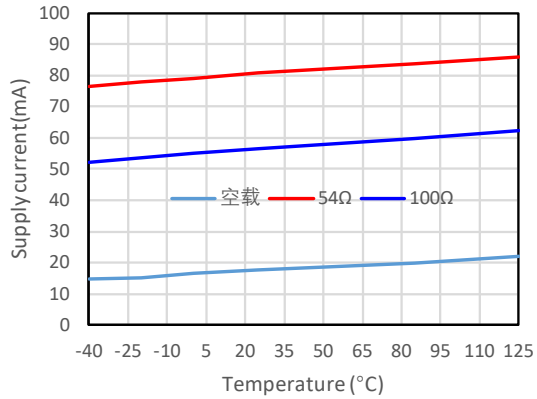


图 7.10-2
Logic-side supply current (I_{CC}) at different bus load
CA-IS2092A，VDDP = 5V，$VISO_{OUT}$ = 3.3V，DR = 500kbps

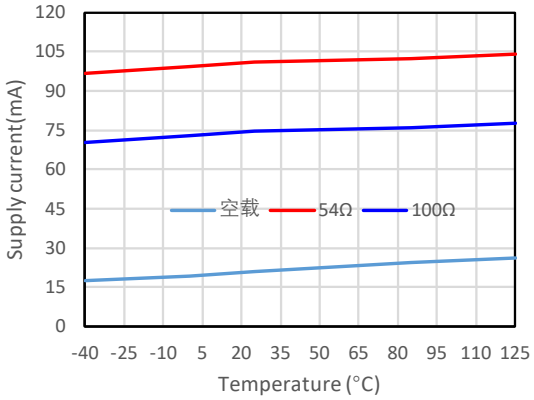


图 7.10-3
Logic-side supply current (I_{CC}) at different bus load
CA-IS2092A，VDDP = 3.3V，$VISO_{OUT}$ = 3.3V，DR = 500kbps

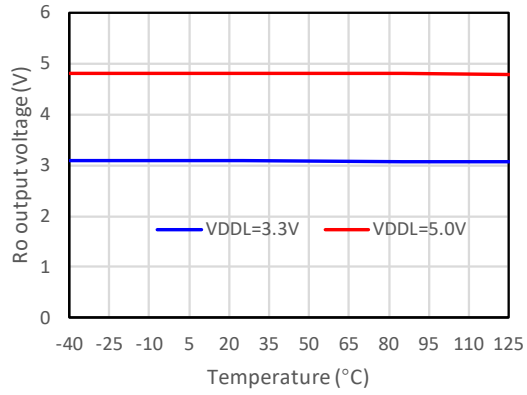


图 7.10-4
R_O = High, R_O pull-down current = 4mA

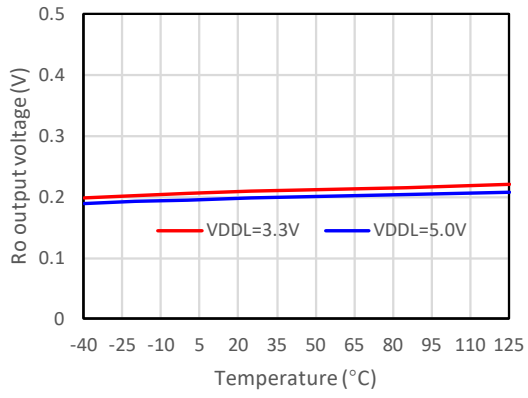


图 7.10-5
R_O = Low, R_O pull-up current = 4mA

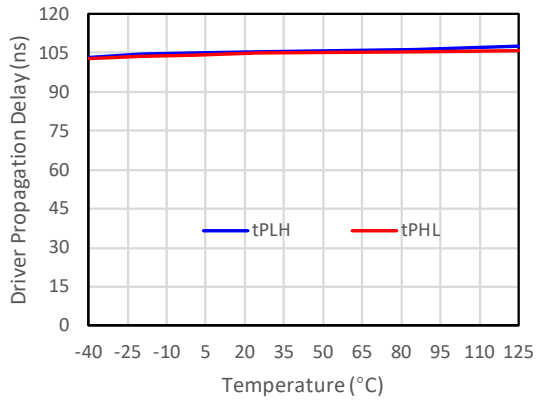


图 7.10-6
driver propagation delay，VDDP = 3.3V，$VISO_{OUT}$ = 3.3V，R_L = 54Ω

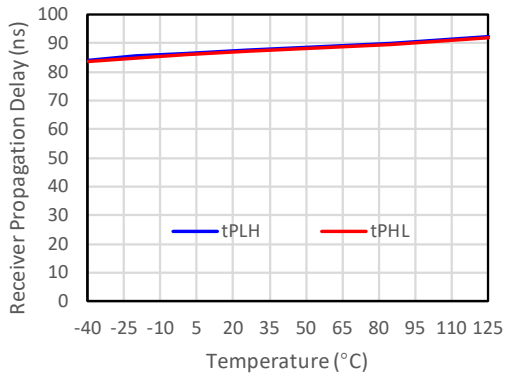


图 7.10-7
receiver propagation delay， VDDP = 3.3V， $VISO_{OUT}$ = 3.3V， R_L = 54Ω

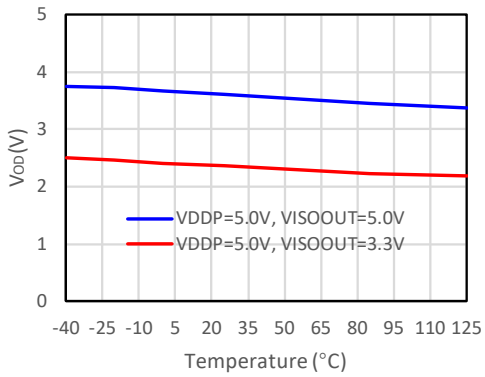


图 7.10-8
Differential output voltage V_{OD}， R_L = 54Ω， VDDP = 5V

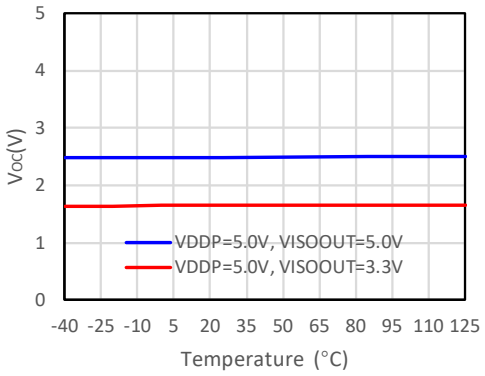


图 7.10-9
Common-mode output voltage V_{OC}， R_L = 54Ω， VDDP = 5V

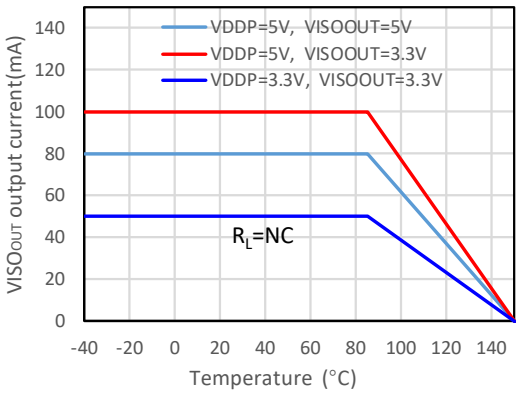
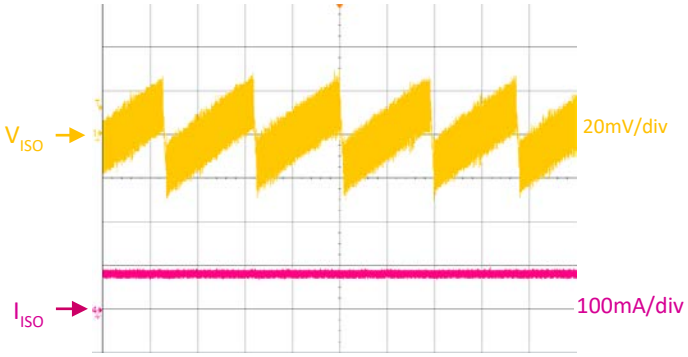
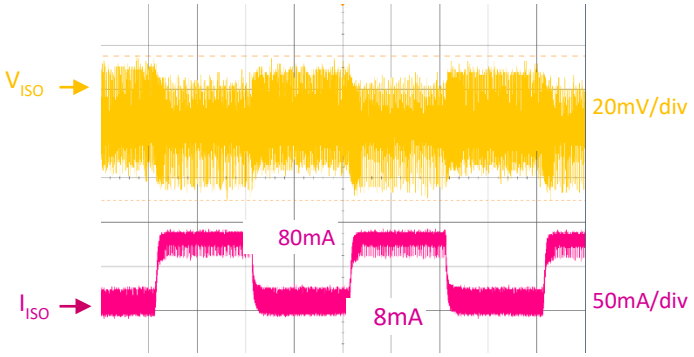


图 7.10-10
Maximum output current from V_{ISO} vs. temperature with R_L = NC
Without data transmission



20µs/div

图 7.10-11
VDDP = 5V， $VISO_{OUT}$ = 5V， R_L = NC
I_{ISO} = 80mA
V_{ISO} Ripple Voltage: 60mV_{P-P}



2ms/div

图 7.10-12
VDDP = 5V， $VISO_{OUT}$ = 5V， R_L = NC
8mA to 80mA I_{ISO} load transient，
V_{ISO} Ripple Voltage: 66mV_{P-P}

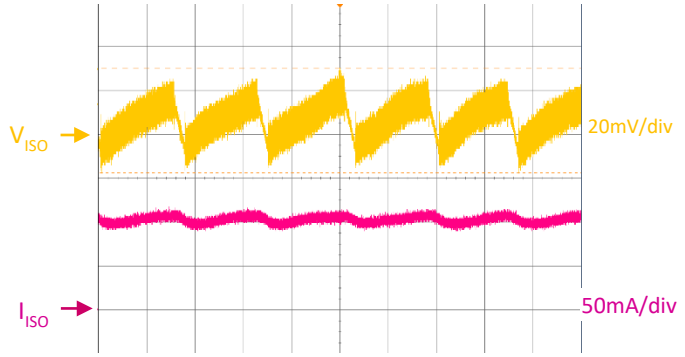


图 7.10-13
VDDP = 5V， $VISO_{OUT}$ = 3.3V， R_L = NC
I_{ISO} = 80mA
V_{ISO} Ripple Voltage: 60mV_{P-P}

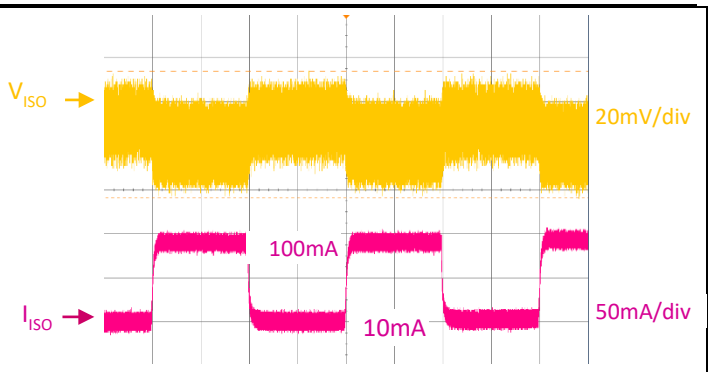


图 7.10-14
VDDP = 5V， $VISO_{OUT}$ = 3.3V， R_L = NC
8mA to 80mA I_{ISO} load transient，
V_{ISO} Ripple Voltage: 66mV_{P-P}

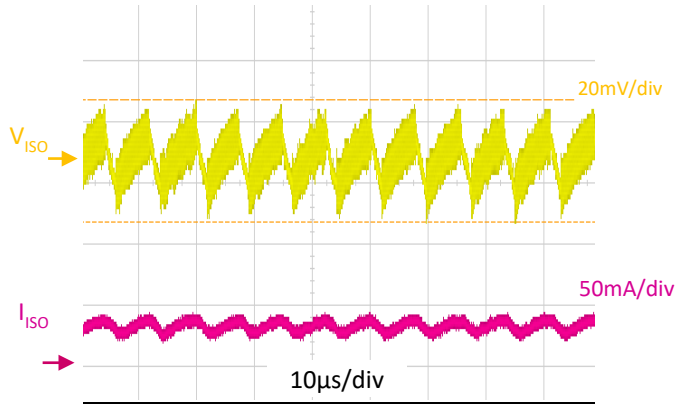


图 7.10-15
VDDP = 3.3V， $VISO_{OUT}$ = 3.3V， R_L = NC
I_{ISO} = 40mA
V_{ISO} Ripple Voltage: 40mV_{P-P}

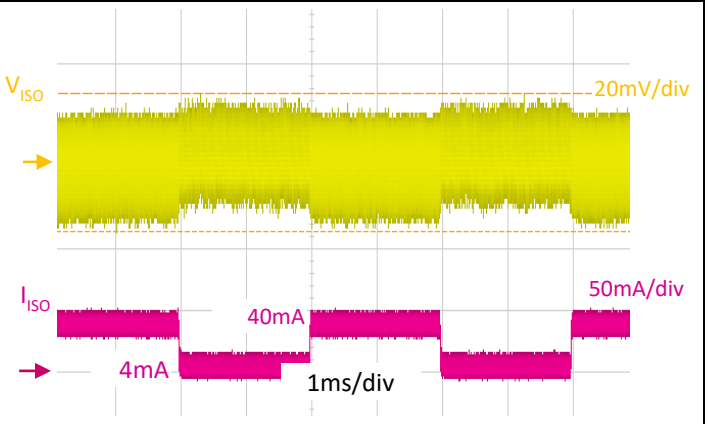


图 7.10-16
VDDP = 3.3V， $VISO_{OUT}$ = 3.3V， R_L = NC
4mA to 40mA I_{ISO} load transient，
V_{ISO} Ripple Voltage: 45mV_{P-P}

8. Parameter Measurement Information

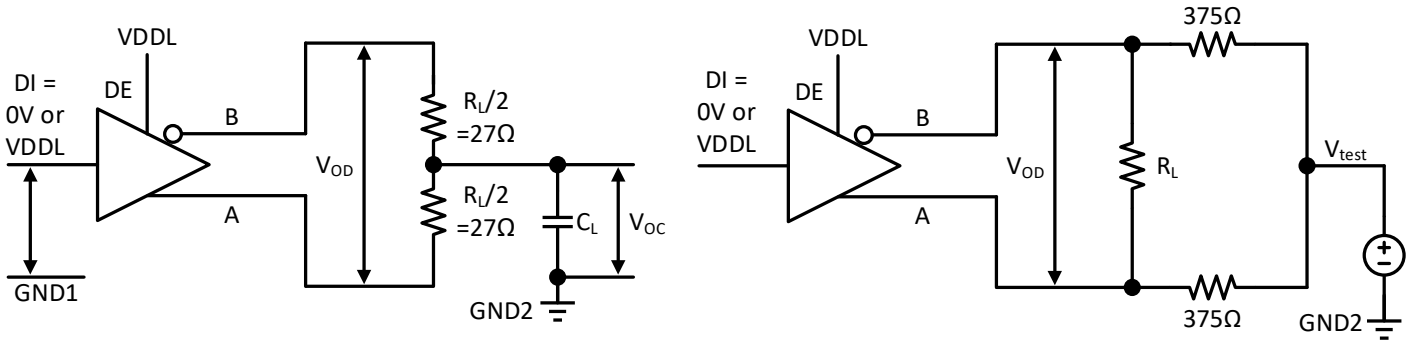


Figure 8-1. Driver DC Test Circuit

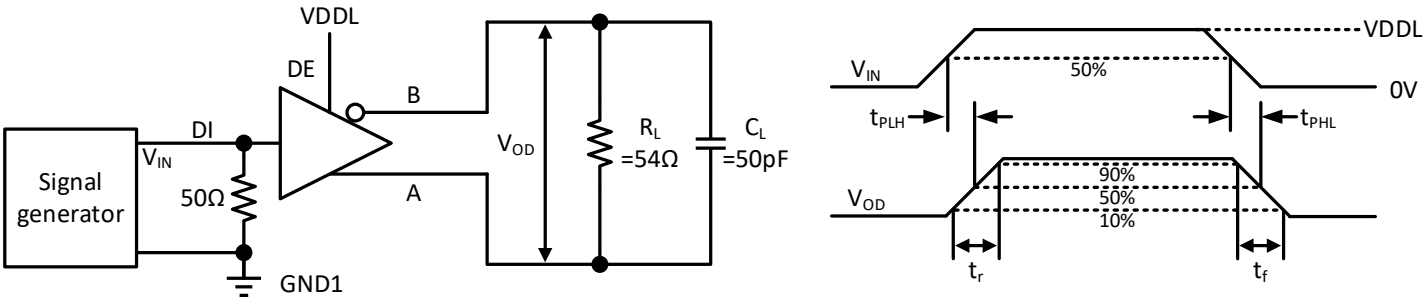


Figure 8-2. Driver Propagation Delays

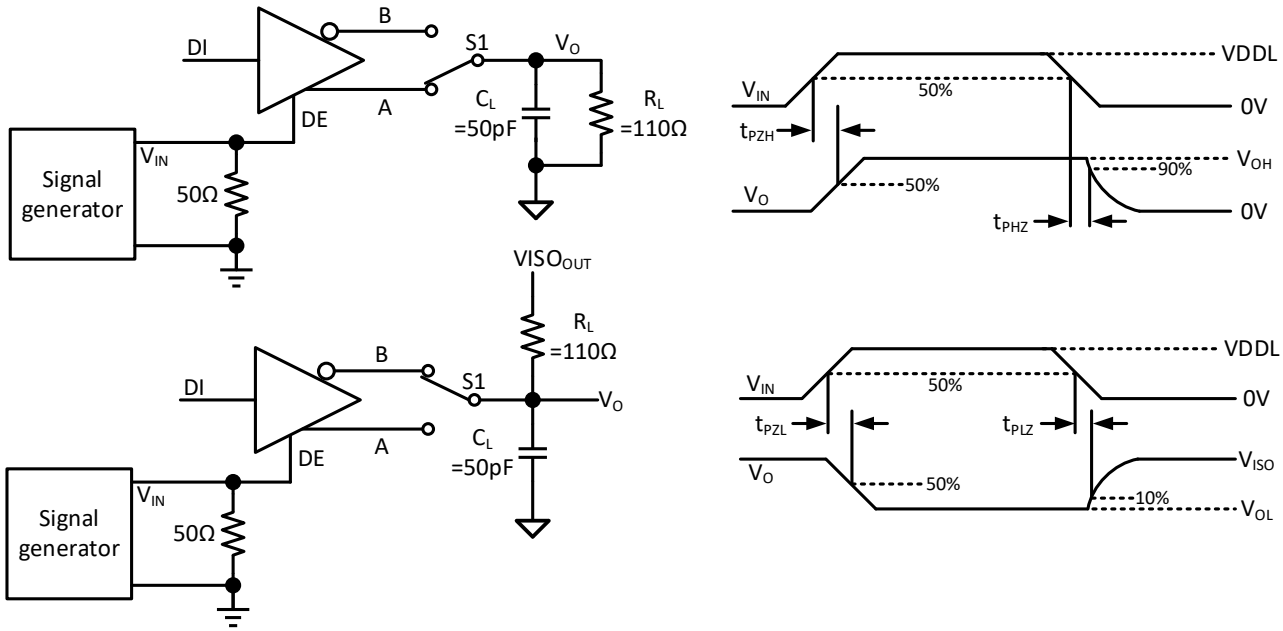


Figure 8-3. Driver Enable and Disable Times

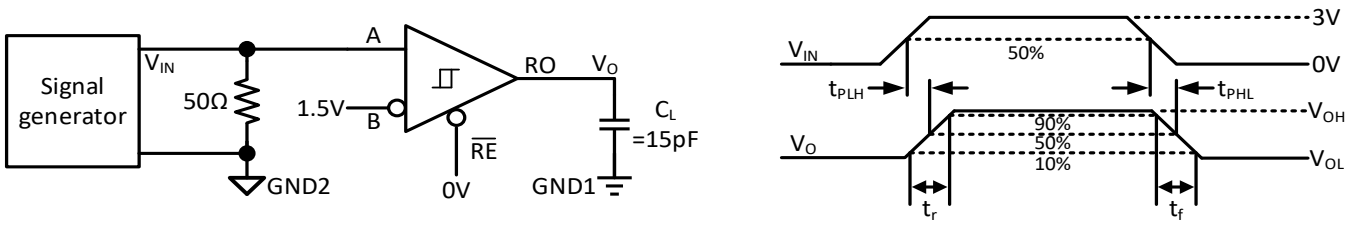


Figure 8-4. Receiver Propagation Delays

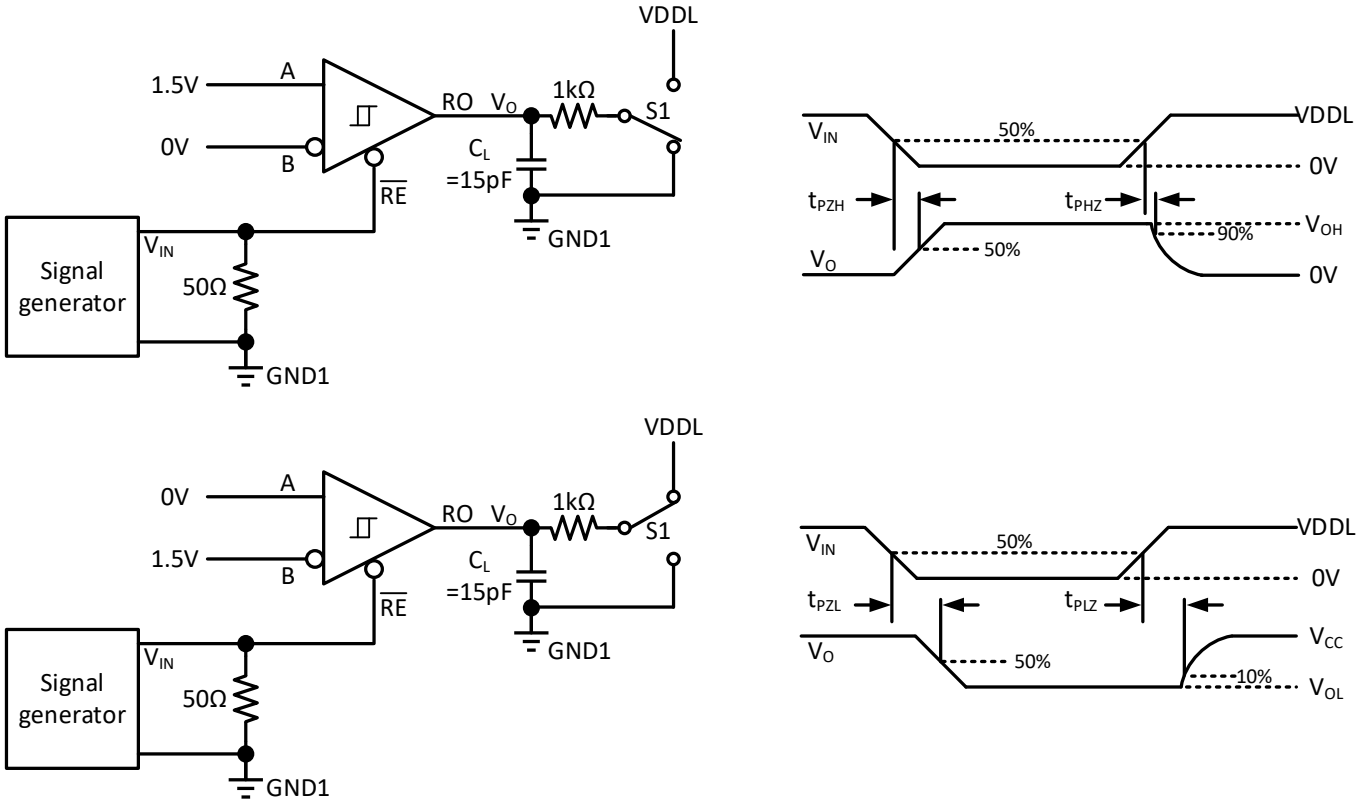


Figure 8-5. Receiver Enable and Disable Times

Notes:

1. R_L = 54 Ω for RS-485
2. C_L includes external circuit (fixture and instrumentation etc.) capacitance.

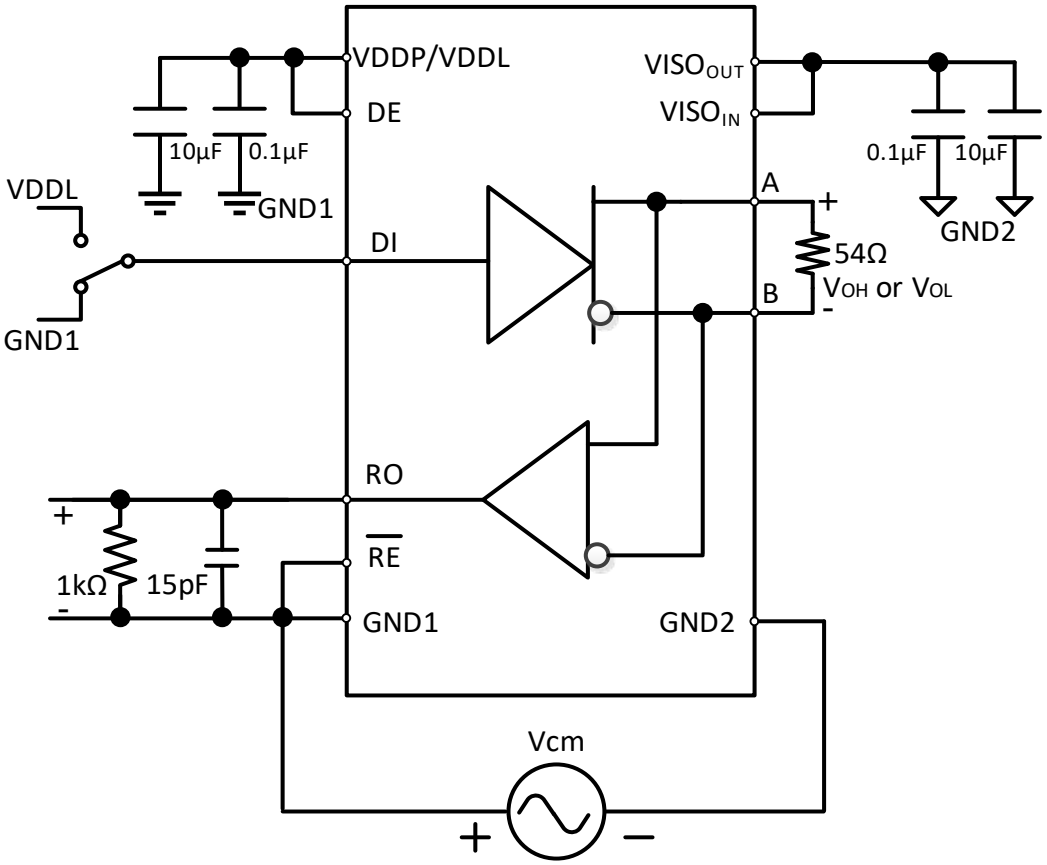


Figure 8-6. Common Mode Transient Immunity (CMTI) Test for the Half-duplex

9. Detailed Description

The CA-IS2092A isolated half-duplex RS-485 transceiver provides up to 2.5kV$_{RMS}$ of galvanic isolation between the cable side (bus-side) and the controller side (logic-side) of the transceiver. This device features up to 150kV/μs common mode transient immunity, allows up to 0.5Mbps communication across an isolation barrier. Power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side circuit. The CA-IS2092A does not require any external components other than bypass capacitors and bus termination resistors to realize an isolated RS-485 port. Robust isolation coupled with extended ESD protection enables efficient communication in noisy environments, making them ideal for long distance transmission and multi-drop communication in a wide range of applications such as motor drives, PLC communication modules, PV Inverter etc.Two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state.

9.1. Logic Input

The CA-IS2092A device includes three logic inputs on the logic side: receiver enable, driver enable and driver digital input. The driver enable control DE pin has an internal weak pull-down to GND1, while the digital input DI and receiver enable pins have an internal pull-up to VDDL, see Figure 9-1 the input equivalent circuit.

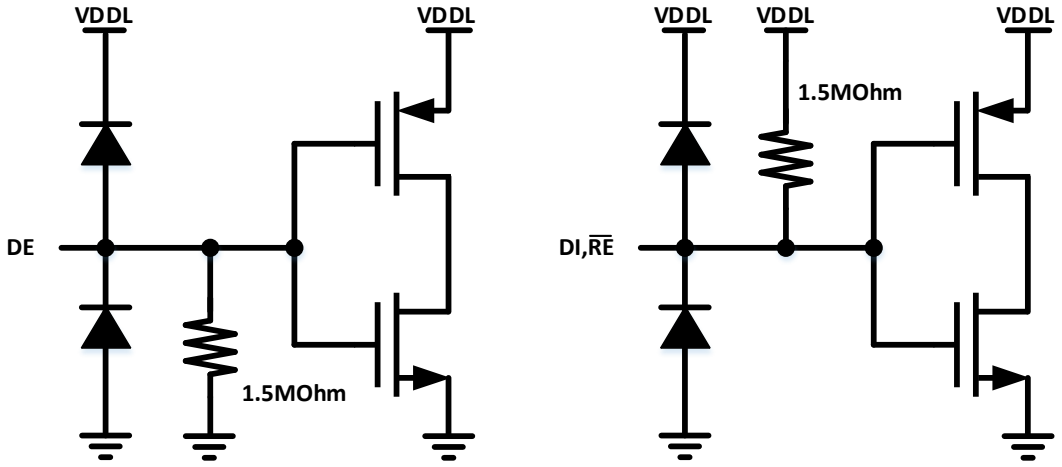


Figure 9-1. Input equivalent circuit

9.2. Fail-Safe Receiver

The receiver reads the differential input from the bus line (A and B) and transfers this data as a single-ended, logic-level output RO to the controller. Driving the enable input $\overline{RE}$ low to enable the receiver; Driving $\overline{RE}$ logic high to disable the receiver. RO is high impedance when $\overline{RE}$ is logic high. The $\overline{RE}$ pin has an internal pull-up resistor to VDDL.

The CA-IS2092A RS-485 transceiver does not require external fail-safe bias resistors because a true fail-safe feature is integrated into the device. In true fail-safe, the receiver's positive-going input threshold is $V_{IT+(IN)}$ (-50mV, max.), if the differential receiver input voltage of V_A-V_B is greater than or equal to $V_{IT+(IN)}$, RO is logic high when $\overline{RE}$ is low; RO is logic low when V_A-V_B is less than or equal to $V_{IT-(IN)}$ (-200mV, min.) in case the receiver is enabled; thereby eliminating the need for fail-safe bias resistors while complying fully with the RS-485 standard, see Table 9-1 the receiver truth table. Fail-safe feature is used to keep the receiver's output in a defined state when the receiver is not connected to the cable, the cable has an open or the cable has a short.

Table 9-1. Receiver Truth Table

Differential Input: $V_{ID} = (V_A - V_B)$	Enable ($\overline{RE}$)	Receiver Output (RO)
$V_{IT+(IN)} \le V_{ID}$	L	H
$V_{IT-(IN)} < V_{ID} < V_{IT+(IN)}$	L	Indeterminate
$V_{ID} \le V_{IT-(IN)}$	L	L
X	H	Hi-Z
Open/Short/Idle	L	H
X	Open	Hi-Z

Notes:
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. $\overline{RE}$ has an internal weak pull-up to V_{DDL}.

9.3. Driver

The transmitter converts a single-ended input signal (DI) from the local controller to differential outputs on the bus lines A and B. The truth table for the transmitter is provided in Table 9-2, the driver enable control DE pin has an internal weak pull-down to GND1, see Figure 9-1 the input equivalent circuit; while the digital input DI pin has an internal pull-up to V_{DDL}. The driver outputs and receiver inputs on the bus side are protected from ±8kV electrostatic discharge (ESD) to GND2, as specified by the Human Body Model (HBM). The driver outputs also feature short-circuit protection and thermal shutdown.

Table 9-2. Transmitter Truth Table

Driver Input	Enable Input	Driver Output	
(DI)	(DE)	A	B
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z
X	OPEN	Hi-Z	Hi-Z
OPEN	H	H	L

Notes:
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. DE pin has an internal weak pull-down to GND1, and DI pin has an internal pull-up to V_{DDL}.

9.4. Protection Functions

9.4.1. Signal Isolation and Power Isolation

The CA-IS2092A device integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. Also, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 3.3V or 5V supply for the cable-side.

9.4.2. Thermal Shutdown

If the junction temperature of the CA-IS2092A device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (180°C, typ.),output Voltage $VISO_{OUT}$ shutdown the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range (< 160°C, typ.) of the device.

9.4.3. Current-Limit

The CA-IS2092A protects the transmitter output stage against a short-circuit to a positive or negative voltage over the common mode voltage range of -7V to 12V by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit fault. The transmitter returns to normal operation once the short-fault is removed.

10. Applications Information

10.1. Overview

The CA-IS2092A half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Because of high peak currents flowing through V_{DDP} and $V_{ISO\_}$ supplies, bulk capacitance of typical 10μF (or at least 4.7μF) is recommended on both pins. Higher values of bulk capacitors are helpful to reduce noise and ripple further and enhance performance, see Figure 10-1 the typical application circuit. Make sure there is no data transmission during the CA-IS2092A power up.

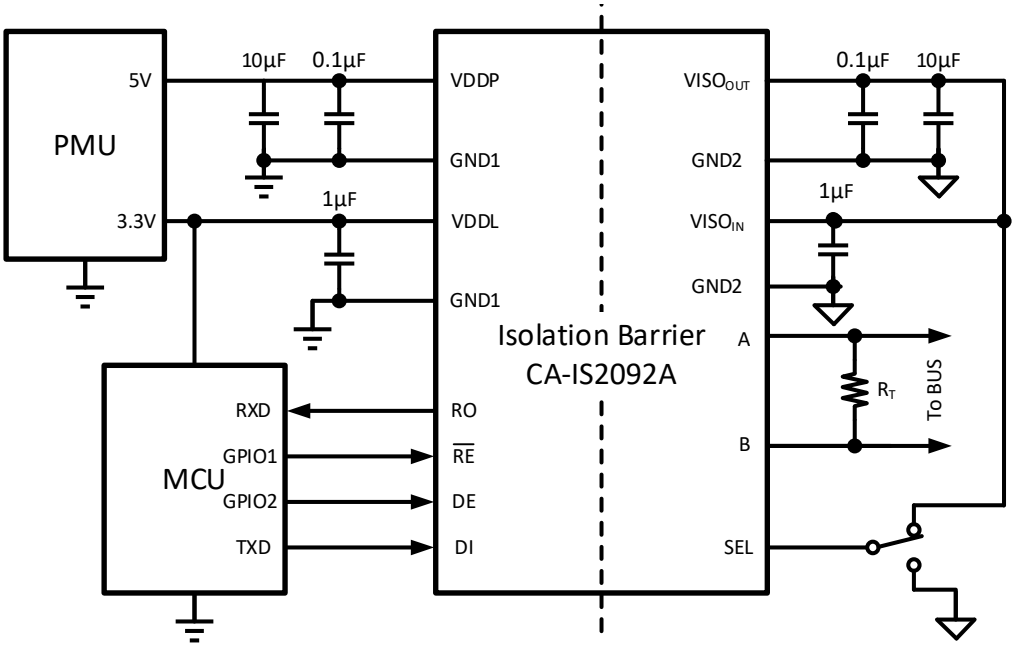


Figure 10-1. Typical application circuit

10.2. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, Figure 10-2.In application, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors. For RS-485 network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. To minimize reflections, terminate the line at both ends with a termination resistor (120Ω in the typical application circuits), whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. As a general rule moreover, termination resistors should be placed at both far ends of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

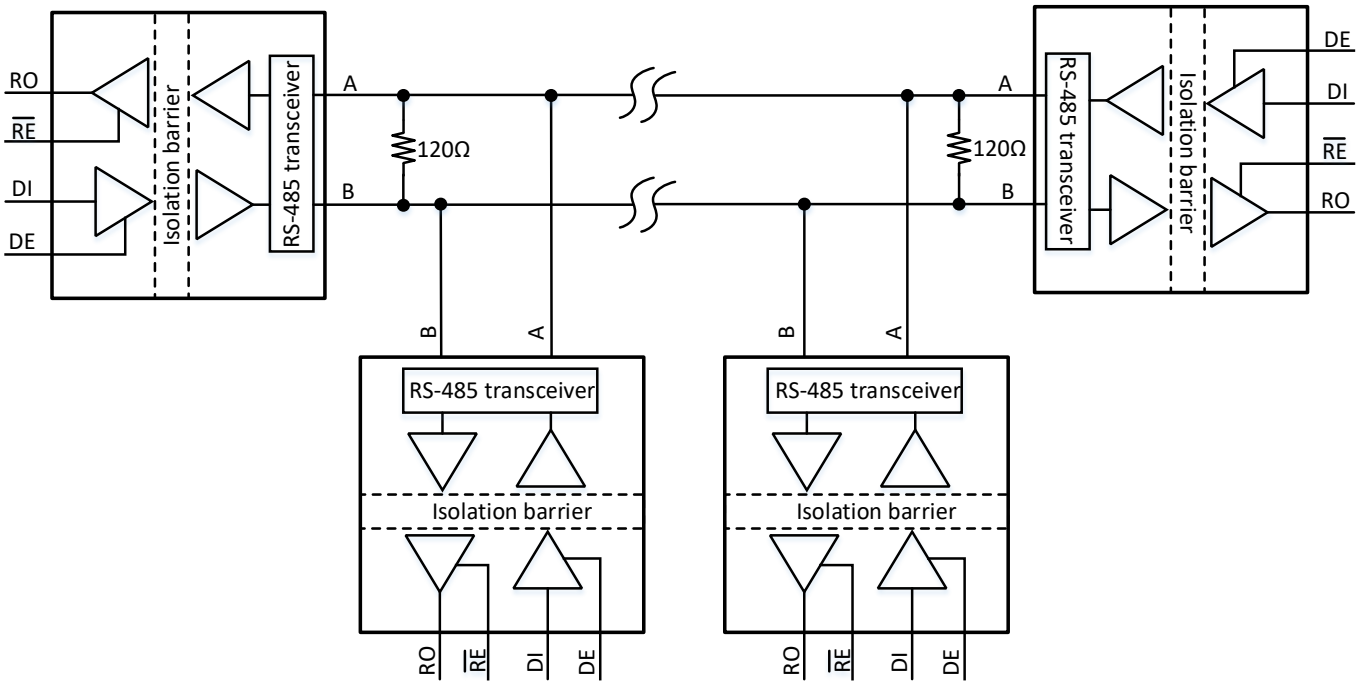


Figure 10-2. Typical isolated half-duple RS-485 application circuit

10.3. 256 transceivers on the bus

The maximum number of transceivers and receivers allowed depends on how much each device loads down the system. All devices connected to an RS-485 network should be characterized in regard to multiples or fractions of unit loads. According to RS-485 standard, the maximum number of unit loads allowed one twisted pair, assuming a properly terminated cable with a characteristic impedance of 120Ω or more, is 32. The CA-IS2092A transceivers have a 1/8-standrad-unit load (96kΩ) receiver, which allows up to 256 transceivers connected in parallel on one communication line.

10.4. PCB Layout

Careful PCB layout is critical to achieve clean and stable communication operation. It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and logic side will defeat the isolation. To make sure device operation is reliable at all data rates and supply voltages, the minimum 0.1μF//10μF decoupling capacitors between VDDP and GND1, between $VISO_{OUT}$ and GND2 are recommended. For the individual logic supply input VDDL and $VISO_{IN}$, we recommend to use a 1μF ceramic capacitors between VDDL pin and GND1,$VISO_{IN}$ pin and GND2.Place the bypass capacitors, and the CA-IS2092A IC on the same PCB layer. Place

decoupling capacitors as close as possible to the CA-IS2092A device pins, see Figure 10-3 recommended components placement for the PCB layout. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths.

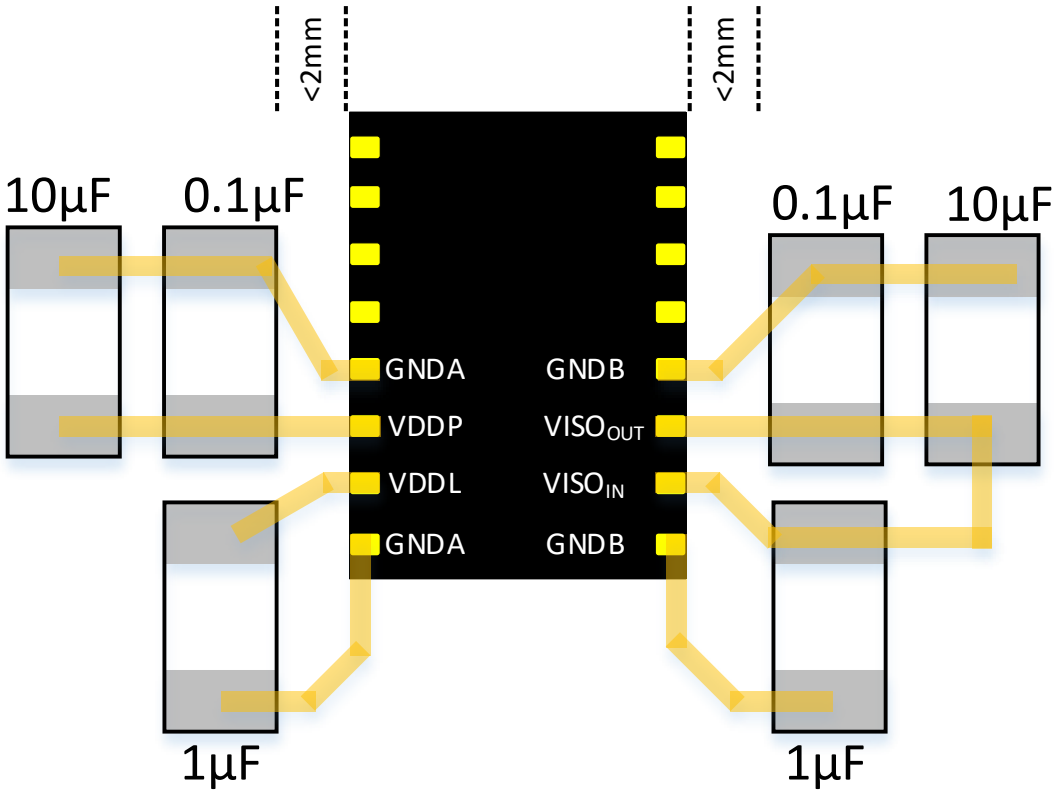
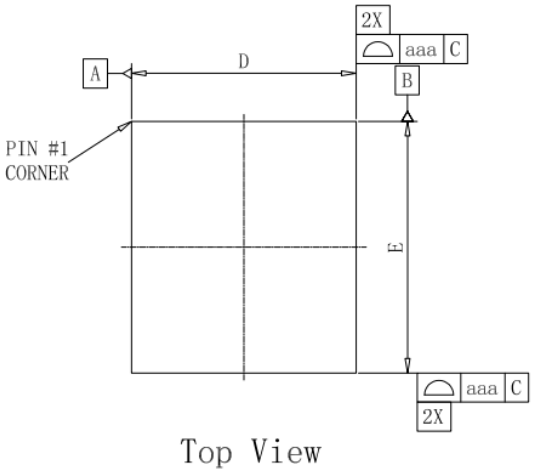


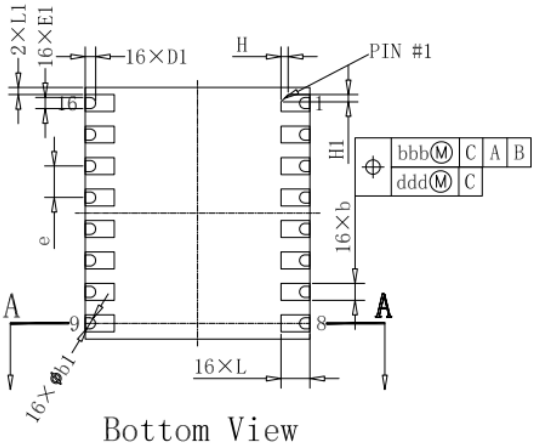
Figure 10-3. Recommended PCB Layout

11. Package Information

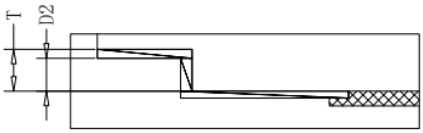
LGA16 Package Outline



Top View

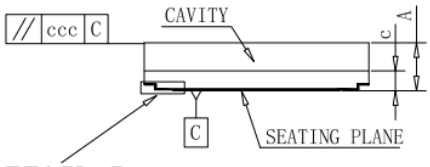


Bottom View



DETAIL B

80:1



DETAIL B

SECTION A-A

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.890	0.990	1.090	0.035	0.039	0.043
c	0.370	0.410	0.450	0.015	0.016	0.018
D	4.550	4.650	4.750	0.179	0.183	0.187
E	5.100	5.200	5.300	0.201	0.205	0.209
D1	0.185	0.215	0.245	0.007	0.008	0.010
E1	0.200	0.230	0.260	0.008	0.009	0.010
D2	0.060	0.085	0.110	0.002	0.003	0.004
H	---	0.150	---	---	0.006	---
H1	---	0.150	---	---	0.006	---
L	0.500	0.600	0.700	0.020	0.024	0.028
L1	0.075	0.150	0.225	0.003	0.006	0.009
e	---	0.650	---	---	0.026	---
b	0.300	0.350	0.400	0.012	0.014	0.016
b1	0.200	0.230	0.260	0.008	0.009	0.010
T	0.083	---	---	0.003	---	---
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

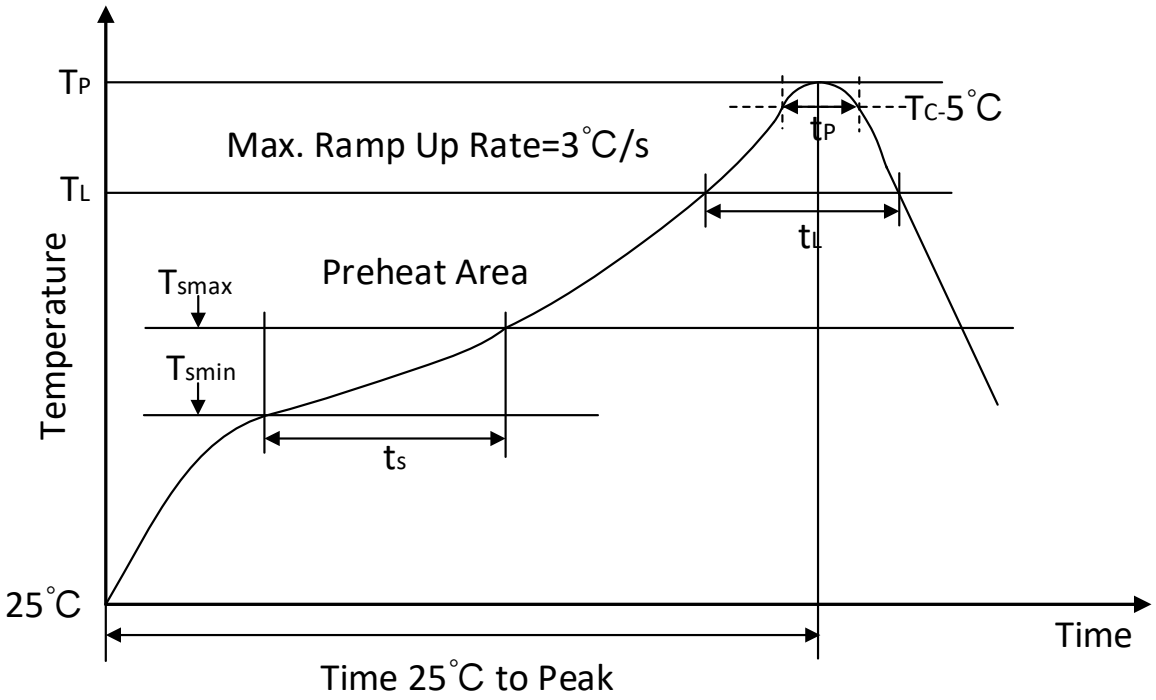


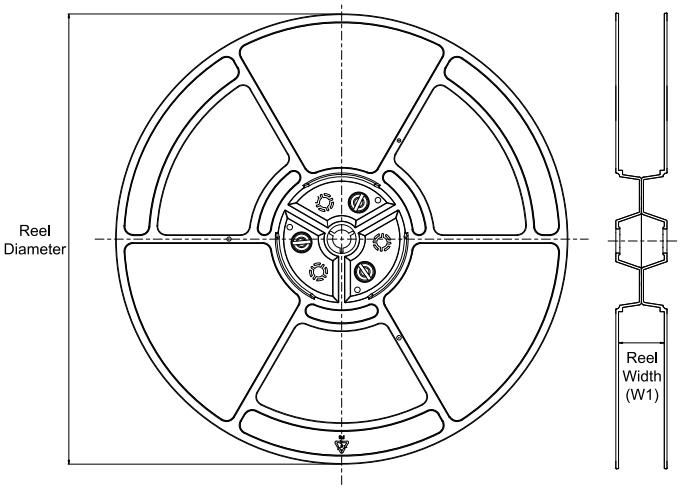
Figure. 12-1 Soldering Temperature (reflow) Profile

Table. 12-1 Soldering Temperature Parameter

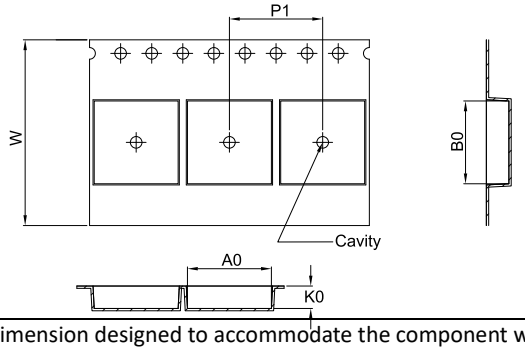
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃ /second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5℃ of actual peak temp	30 second
Ramp-down rate	6 ℃ /second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape And Reel Information

REEL DIMENSIONS

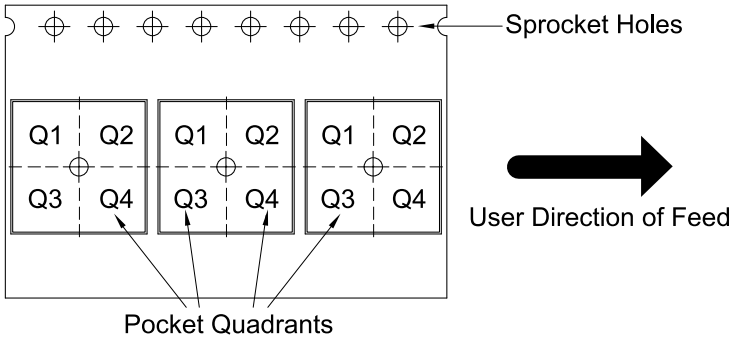


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2092A	LGA16 4.65x5.2	A	16	3000	330	12.4	4.95	5.50	1.29	8.0	12.0	Q1

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