PoE PD Solution with PSR or SSR Active Clamp Flyback Converter

Features

- Compatible with 802.3af Specifications
- 100-V 0.56-Ω PD Input MOSFET
- Active Clamp Primary-Side Regulated (PSR) Flyback without Aux-winding
- Active Clamp Secondary-Side Regulated (SSR) Flyback through Opto-coupler
- 0.36-Ω and 0.78-Ω Integral Flyback MOSFETs
- Programmable up to 650-kHz Frequency
- 1.5-A Switching Current Limit
- Output Diode Compensation in PSR Mode
- Programmable Soft-Start Time
- Frequency Foldback during Startup and Protection
- Automatic Light Load Power Maintain Signature
- EMI Reduction with Frequency Dithering
- Hiccup OLP, OVP, and OTP Protection
- Operating T_J Temperature Range from −40°C ~ +125°C
- Available in 3×4 19-pin QFN Package

Applications

- IEEE 802.3af-Compliant Devices
- Security Camera
- VoIP Phones
- WLAN Access Points
- IoT Devices

Description

The TPE15017 is a monolithic power over ethernet (PoE) powered device (PD) with integrated PD interface and fly-back power converter. The device supports IEEE 802.3af standard interface and targets for small-size 13-W isolated PoE applications.

The PD interface has all the functions of IEEE 802.3af, including detection, classification, inrush current, operation current limit, and 100-V hot-swap MOSFET.

To achieve small size and high-switching frequency, the TPE15017 fly-back converter is specifically designed with active clamp primary-side regulation (PSR) fly-back topology. TPE15017 can also be set in secondary-side regulation (SSR) active clamped fly-back topology, which can get best regulation through opto-coupler from secondary side.

The TPE15017 automatically sinks 15-mA pulse current as the maintain power signature in light load condition to maintain the connection with the PSE equipment and turns off the MPS current when the load current is above the MPS threshold.

The TPE15017 is available in 3mm x 4mm QFN-19 package.

Typical Application Circuit

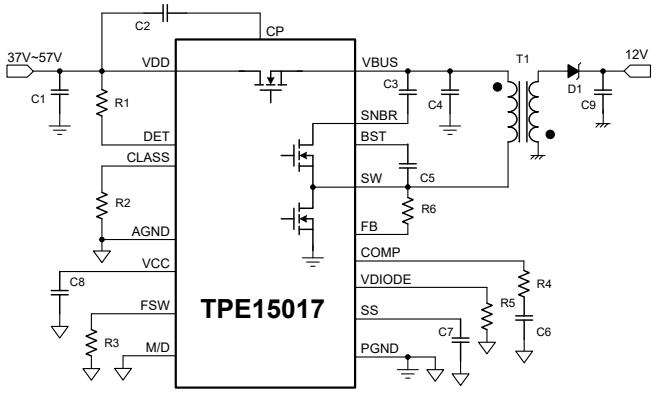


Table of Contents

Revision History

Date	Revision	Notes
2024-5-13	Rev.A.0	Initial Release

Pin Configuration and Functions

TPE15017
QFN3X4-19
Top View

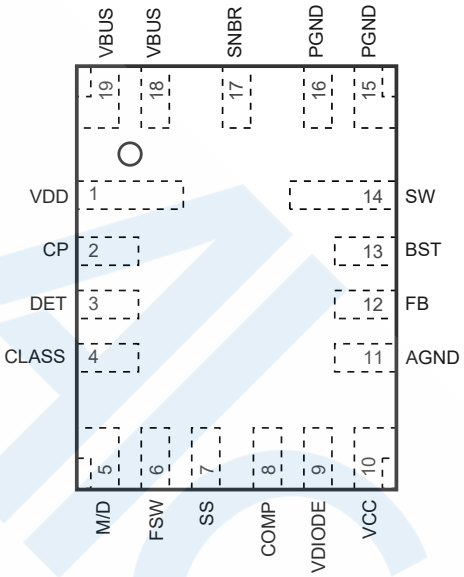


Table 1. Pin Functions: TPE15017

Pin		I/O/P	Description
No.	Name		
1	VDD	P	Positive power supply from PoE input power rail.
2	CP	O	Charge-pump output for hot-swap MOSFET driver power supply.
3	DET	O	PD detection and power enable pin. Connect a 24.9kΩ resistor between VDD and DET for PoE detection. Pulling DET to ground can disable class function, hot-swap MOSFET and fly-back converter.
4	CLASS	O	Classification pin. Connect a resistor from CLASS to AGND to program the classification current.
5	M/D	O	Feedback MODE and dither function select pin. Refer to “Table 2” for the detail function setting.
6	FSW	O	Switching Frequency Set Pin. An external resistor from this pin to AGND sets the switching frequency.
7	SS	O	Soft-start and hiccup period control pin. Connect one capacitor between the SS pin and AGND. The SS pin controls the FB ramp slew-rate in PSR mode and controls the COMP ramp slew rate in SSR mode. The SS pin also controls the hiccup protection period.

Pin		I/O/P	Description
No.	Name		
8	COMP	I/O	Feedback loop control pin. The COMP pin is the output of the feedback error amplifier for PSR mode and the feedback input pin for SSR mode.
9	VDIODE	O	Compensation pin for the output rectifier diode voltage drop. A resistor between the VDIODE pin and AGND compensates the output voltage for different switching current.
10	VCC	P	DCDC converter internal circuit power supply pin. The VCC pin is the output of an internal LDO powered from VDD input. Connect more than 2.2μF capacitor between the VCC pin and AGND for the internal LDO. VCC also can be powered from an external power supply of lower than 6.5 V to eliminate the power loss of the internal LDO.
11	AGND	GND	Analog signal power ground.
12	FB	I	Output voltage feedback in PSR mode, and PSR/SSR OVP pin. In PSR mode, connect one resistor from SW pin to FB pin to regulate the output voltage. In SSR mode, the internal EA is disabled, and output voltage signal is feedback from the COMP pin, connect one resister FB to SW can set the OVP threshold, or float FB pin if OVP function isn`t required.
13	BST	I	Bootstrap power supply for the high-side MOSFET driver. Connect one 0.1μF capacitor between the BST pin and the SW pin.
14	SW	I	Drain of the main MOSFET switch and source of the synchronous active clamp MOSFET switch.
15, 16	PGND	GND	Power ground of the flyback converter.
17	SNRB	O	Active clamp snubber capacitor connection pin. It is connected to the drain of internal synchronous MOSFET switch.
18, 19	VBUS	P	Source of the PD hot-swap MOSFET. It supplies power for fly-back converter.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage range at terminals	VDD, VBUS, DET, SW, SNBR	−0.3	105	V
	FB	VBUS − 0.3	VBUS+0.2	V
	CP	VDD − 0.3	VDD+7	V
	BST	SW − 0.3	SW+7	V
	All Other Pins	−0.3	7	V
T_J	Maximum Junction Temperature	−40	125	°C
T_A	Operating Temperature Range	−40	85	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{DD}	Power Supply	37		57	V
V_{SW}	Voltage at the Switching Node			95	V
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN3X4-19L	56.5	13.4	25.5	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 48 V, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C. R_{DET} = 24.9 kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Detection						
V_{DET_ON}	Detection On	V_{DD} rising		0.9	1.3	V
V_{DET_OFF}	Detection Off	V_{DD} falling	10.1	10.7		V
V_{DET_LKG}	DET Leakage Current	V_{DET} = V_{DD} = 57 V		0.1	5	μA
I_{SUPPLY}	Supply Current	V_{DD} = 10.1V, float DET pin, not in Mark event			12	μA
I_{DET}	Detection Current	V_{DD} = 2 V	78	81	84	μA
		V_{DD} = 10.1 V	400	410	420	μA
V_{DET_TH}	DET Disable Threshold	Disable functions except detection. Falling edge	2.4	2.9	3.4	V
V_{DET_HYS}	DET Disable Threshold Hysteresis			0.5		V
Classification						
T_{CLASS}	Classification Stability Time			250		μs
V_{CLASS}	Class Output Voltage	13 V < V_{DD} < 21 V, 1 mA < I_{CLASS} < 44 mA	1.11	1.16	1.21	V
I_{CLASS}	Classification Current	R_{CLASS}= 578 Ω, 13V ≤ V_{DD} ≤ 21 V	1.8	2	2.4	mA
		R_{CLASS}= 110 Ω, 13 V ≤V_{DD} ≤ 21 V	9.9	10.55	11.3	mA
		R_{CLASS}= 62 Ω, 13 V ≤ V_{DD} ≤ 21 V	17.7	18.7	19.8	mA
		R_{CLASS}= 41.2 Ω, 13 V ≤ V_{DD} ≤ 21 V	26.6	28.15	29.7	mA
		R_{CLASS}= 28.7 Ω, 13 V ≤ V_{DD} ≤ 21 V	38.2	40.4	42.6	mA
V_{CLON}	Classification Low Threshold	Regulator turns on, V_{DD} Rising	11.8	12.4	13.0	V
V_{CLON_HYS}	Classification Low Threshold Hysteresis	Low threshold hysteresis		1.0		V
V_{CLOFF}	Classification High Threshold	Regulator turns off, V_{DD} Rising	21.2	22	22.7	V
V_{CLOFF_HYS}	Classification High Threshold Hysteresis	High threshold hysteresis		0.5		V
V_{MARK_L}	Mark Event Reset Threshold		4.5	5.0	5.5	V
V_{MARK_H}	Max Mark Event Voltage		10.8	11.4	12.0	V
I_{MARK}	Mark Event Current		1.0	1.5	2	mA
R_{MARK}	Mark Event Resistance	2-point measure at 5.5 V and 10.1 V, R=ΔV / ΔI	45			kΩ
I_{IN_CLS}	IC Supply Current During Classification	V_{DD}= 17.5 V, CLASS floating		90	150	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CLS_LKG}	CLASS Leakage Current	V_{CLASS}= 0 V, V_{DD} = 57 V			1	μA
PD UVLO						
V_{DD_R}	VDD Turn-on Threshold	V_{DD} Rising	36	37.9	40	V
V_{DD_F}	VDD Turn-off Threshold	V_{DD} Falling	30	31	32.5	V
V_{DD_HYS}	VDD UVLO Hysteresis		5	6.9		V
I_{DD_LKG}	Input Leakage Current	V_{DD}= 29.5 V			200	μA
I_Q	IC Supply Current during Operation	No load, no switching		1.5	1.8	mA
Pass Device and Current Limit						
R_{ON_PD}	PD MOSFET On Resistance	360-mA load on VBUS		0.56		Ω
I_{PD_LKG}	Leakage Current of PD MOSFET	V_{DD} = 57 V, V_{BUS} = 0 V, DET = low		1		μA
V_{CP}	CP Regulation Voltage			5		V
I_{PD_LIMIT}	PD Current Limit	V_{BUS} drop from V_{DD}, V_{DD} -V_{BUS} = 1 V	350	460		mA
I_{INRUSH}	Inrush Current Limit	V_{BUS} ramps up from low to high, V_{DD} - V_{BUS} = 1 V		115		mA
I_{TERM}	Inrush Current Termination	V_{BUS} Rising		98		mA
t_{DELAY}	Inrush to Operation Mode Delay		80	110		ms
V_{FDBK}	Current Fold-Back Threshold	V_{BUS} falling, V_{DD}- V_{BUS}		10		V
t_{FDBK}	Fold-back Deglitch Time	V_{BUS} falling to inrush current		1		ms
VBUS OVP Protection						
V_{CLAMP}	VBUS Maximum Regulated Voltage	V_{CC} = 5 V	57	63	69.5	V
Converter Power Supply						
V_{BUS_R}	Converter VBUS UVLO Rising Threshold	V_{BUS} starts charging V_{CC}		10		V
V_{BUS_F}	Converter VBUS UVLO Falling Threshold	V_{BUS} stops charging V_{CC}		8		V
V_{CC}	VCC Regulation Voltage	0 mA to 10 mA load current	4.7	5	5.3	V
V_{CC_R}	VCC UVLO Rising Threshold	V_{DD} is higher than UVLO threshold, V_{CC} rising		4.5		V
$V_{CC\text{-}F}$	VCC UVLO Falling Threshold	V_{DD} is higher than UVLO threshold, V_{CC} falling		4.3		V
V_{SNBR_DIS}	SNBR Discharge Threshold Before Switching	V_{SNBR} - V_{BUS}		1.5		V
I_{SNBR_DIS}	SNBR Discharge Current	Discharge to V_{BUS}		3		mA
Voltage Feedback						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{FB_REG}	FB Regulation Current	V_{BUS} = 37 V - 57 V, T_J= 25°C	99	100	101	μA
		V_{BUS} = 37 V - 57 V, T_J= −40°C to +125°C	98	100	102	μA
V_{FB_OS}	FB to VBUS Offset Voltage	V_{FB}- V_{BUS}, 100-μA current into the FB pin.	-50	0	50	mV
I_{FB_OVP}	FB Feedback OVP Threshold		115	127	139	μA
Error Amplifier						
G_{EA}	Error Amplifier Gain	PSR mode, I_{FB} = I_{FB_REG}± 5 μA, V_{COMP}= 1.5 V		14		μA/μA
I_{SOURCE}	Amplifier Maximum Source Current	PSR mode, V_{COMP}= 1.5 V, I_{FB} = 90 μA		-110		μA
I_{SINK}	Amplifier Maximum Sink Current	PSR mode, V_{COMP}= 1.5 V, I_{FB}= 110 μA		110		μA
V_{CLMP_H}	COMP High Voltage	PSR mode, I_{FB}= 90 μA		3.5		V
		SSR mode, float COMP		3.5		V
R_{PULLUP}	COMP Pull-up Resistor	SSR mode	8	10.3	13	kΩ
I_{PULLUP}	COMP Pull-up Bias Current	SSR mode	80	96	115	μA
PSR Mode Regulation Compensation						
G_{D_COMP}	VDIODE Compensation Gain	LS-FET current to VDIODE voltage gain		0.8		V/A
Switching MOSFET						
R_{ON_LS}	Low-side Switching MOSFET			0.36		Ω
R_{ON_HS}	High-side Switching MOSFET			0.78		Ω
I_{LS_LKG}	Low-side FET Leakage Current	V_{SW} = 100 V		0.1	10	μA
I_{HS_LKG}	High-side FET Leakage Current	V_{BUS} – V_{SW} = 100 V		0.1	10	μA
M/D Pin Setting						
I_{MD_DET}	MODE/Dither Pin Detection Current		85	100	115	μA
t_{MD_DET}	MODE/Dither Detection Period			160		μs
V_{MD_DET}	MODE/Dither Pin Detection Threshold Voltage	Voltage level 1 range			0.1	V
		Voltage level 2 range	0.5		0.95	V
		Voltage level 3 range	1.15		1.95	V
		Voltage level 4 range	2.15			V
Frequency Dither						
f_{DITH}(1)	Dither Frequency Range			±7%		f_{SW}
f_{MOD}(1)	Dither Modulation Frequency			12.5		kHz
OLP, SCP, OVP Protection						
I_{LS_LIMIT}	LS FET Switching Current Limit		1.35	1.5	1.65	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SCP}	SCP Limit			2.1		A
I_{HS_LIMIT}	HS FET Negative Current Limit	SNBR to SW	-1.0	-0.8	-0.6	A
I_{SS}	SS Charge Current			50		μA
I_{SS_OVLD}	SS Discharge Current during Overload			20		μA
I_{SS_PRO}	SS Discharge Current during Protection			2		μA
V_{SS}	SS Charged Threshold Voltage			3.5		V
V_{SHDN}	Overload Shutdown Threshold Voltage			3		V
V_{RST}	Protection Reset Threshold Voltage			0.2		V
V_{SNBR_OV}	SNBR Pin Over-Voltage Threshold			105		V
Switching Frequency						
f_{SW}	Switching Frequency	R_{SW} =9.31 kΩ	450	500	550	kHz
		R_{SW} = 18.7 kΩ	215	250	285	kHz
f_{SW_FDBK}	Fold-back Frequency	V_{SS} = 0 V or V_{FB} = 0 V.		76		kHz
t_{MIN_ON}	Minimum On Time			200		ns
t_{MIN_OFF}	Minimum Off Time		350	475	560	ns
D_{MAX}	Maximum Duty Cycle	f_{SW} = 500 kHz		74		%
Thermal Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		150		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		20		ºC

(1) Guaranteed by design and sample characterization. Not tested in production.

Typical Performance Characteristics

All test conditions: V_{DD} = 48V, V_{OUT} = 12V, TJ = 25℃, unless otherwise noted.

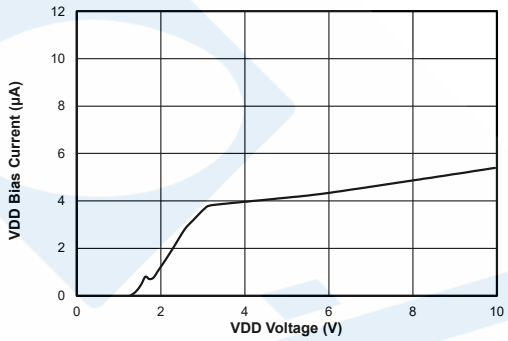
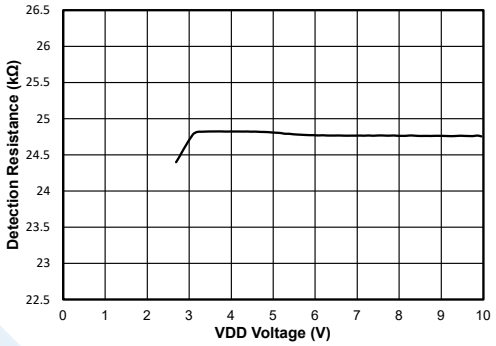


Figure 1. VDD Bias Current During Detection vs. VDD Voltage



R_{DET} = 24.9 kΩ

Figure 2. Detection Resistance vs. VDD Voltage

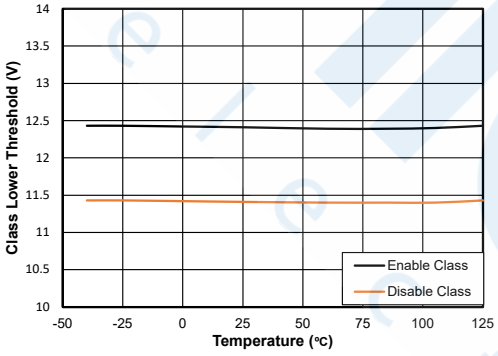


Figure 3. Class Lower Threshold Voltage vs. Temperature

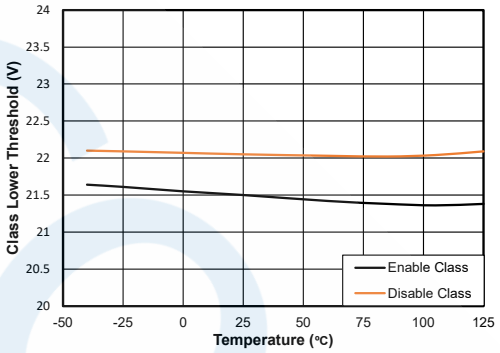


Figure 4. Class Upper Threshold Voltage vs. Temperature

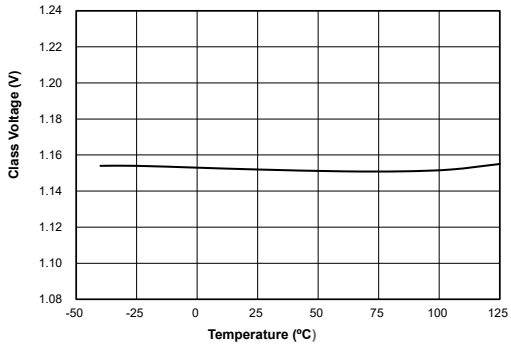


Figure 5. Class Voltage vs. Temperature

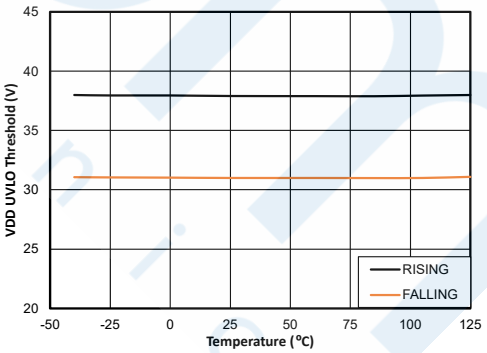
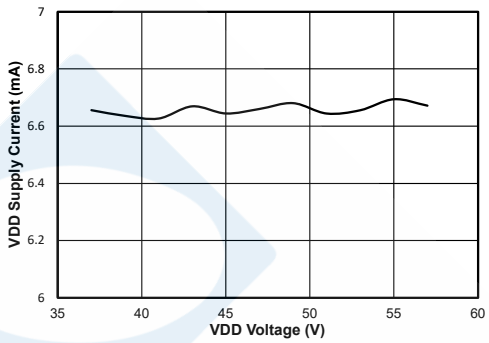


Figure 6. VDD UVLO Threshold vs. Temperature



f_{sw} = 500 kHz

Figure 7. VDD Supply Current vs. VDD Voltage

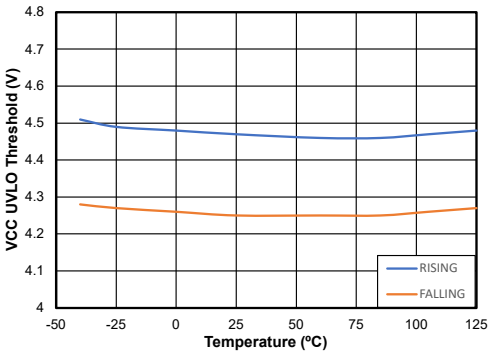


Figure 8. VCC UVLO Threshold Voltage vs. Temperature

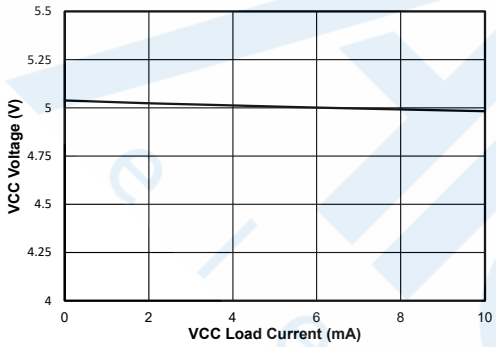
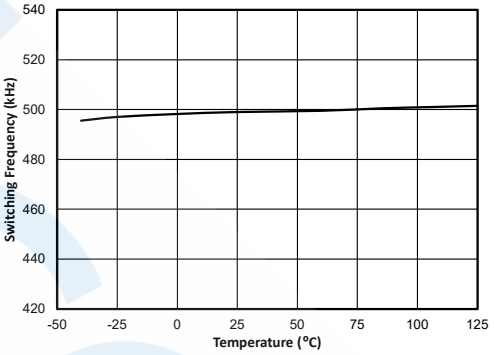


Figure 9. VCC Voltage vs. External VCC Load



f_{sw} = 500 kHz

Figure 10. Frequency Vs. Temperature

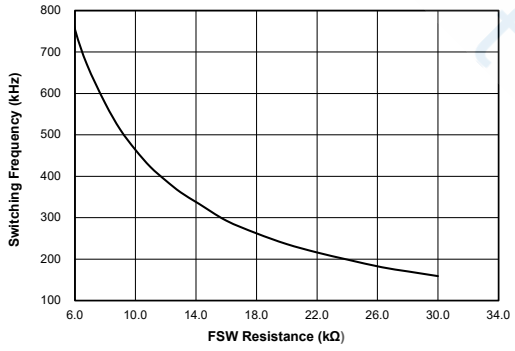


Figure 11. Switching Frequency vs. FSW Resistance

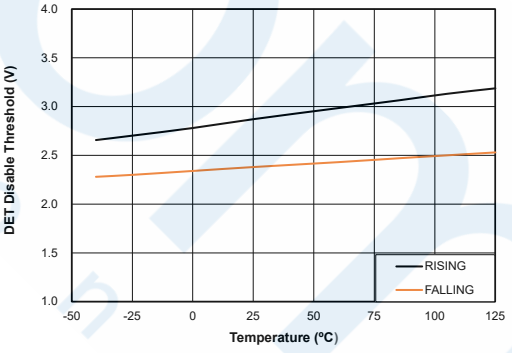


Figure 12. DET Disable Threshold vs. Temperature

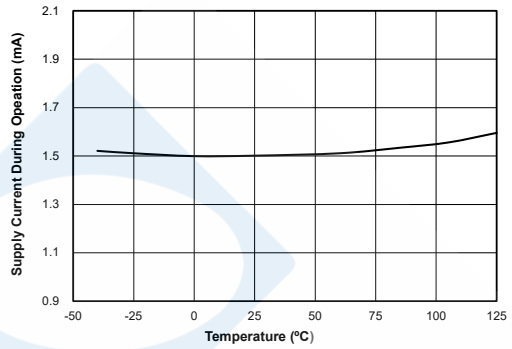


Figure 13. IC Supply Current during Operation vs. Temperature

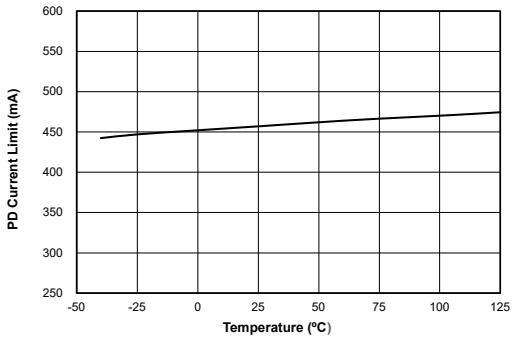


Figure 14. PD current Limit vs. Temperature

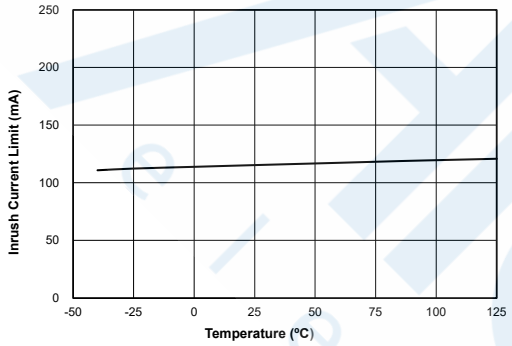


Figure 15. Inrush Current Limit vs. Temperature

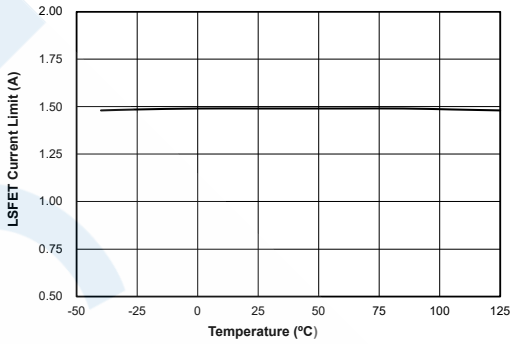


Figure 16. LSFET Switching Current Limit vs. Temperature

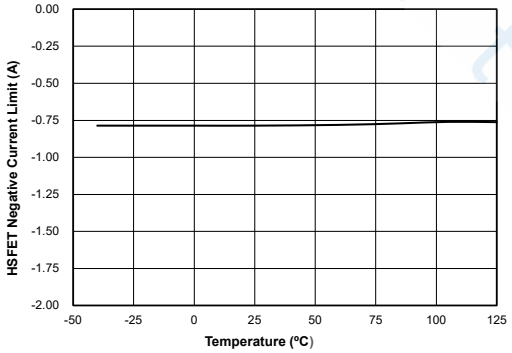
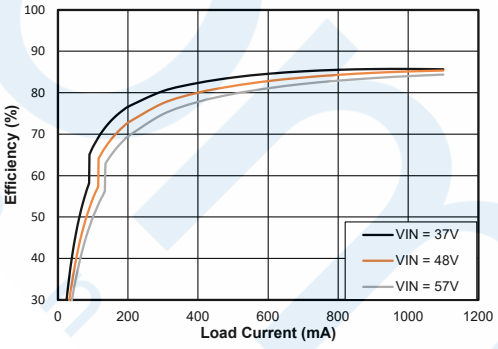
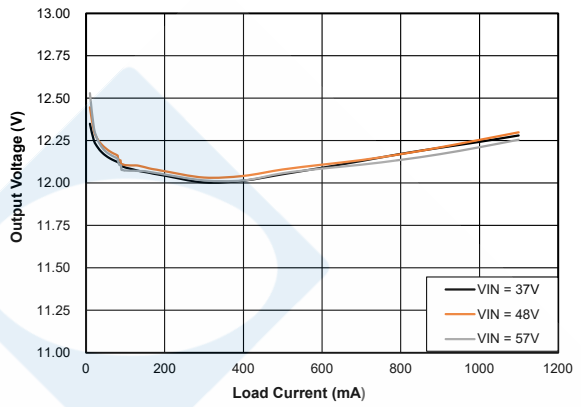


Figure 17. HSFET Negative Current Limit vs. Temperature



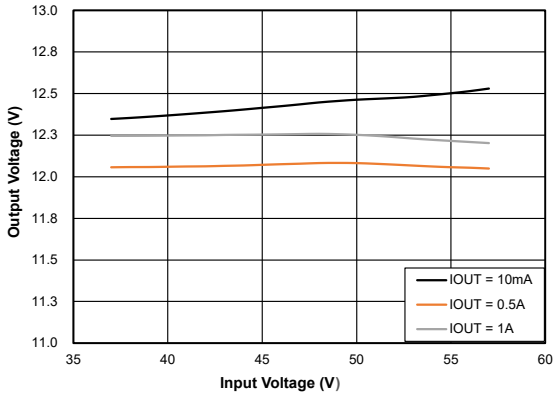
V_{DD} = 37 V, 48 V, 57 V, f_{SW} = 500 kHz, V_{OUT} = 12 V

Figure 18. Efficiency vs. Load Current



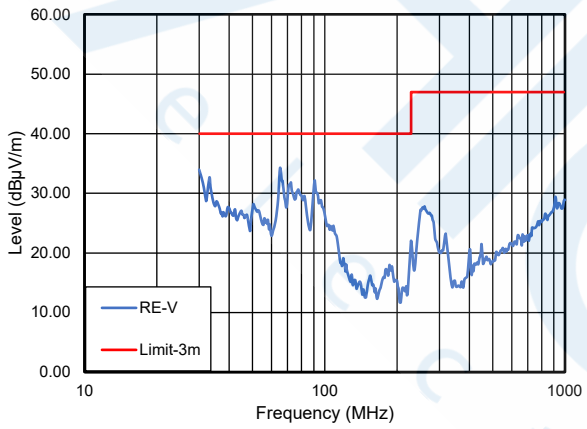
V_{DD} = 37 V, 48 V, 57 V, f_{SW} = 500 kHz, V_{OUT} = 12 V

Figure 19. Output Voltage vs. Load Current



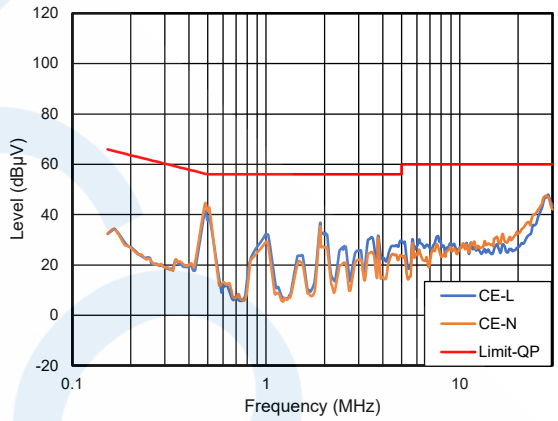
f_{SW} = 500 kHz, V_{OUT} = 12 V, I_{OUT} = 10 mA, 0.5 A, 1 A

Figure 20. Output Voltage vs. Input Voltage



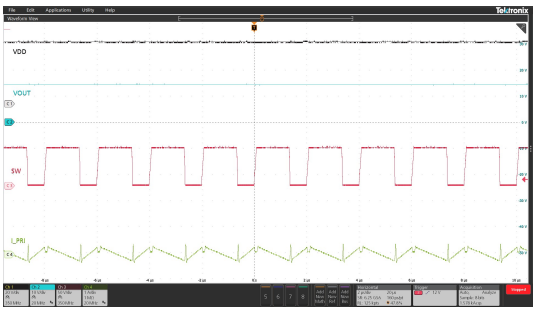
V_{DD} = 48 V, f_{sw} = 500 kHz, V_{OUT} = 12 V

Figure 21. Radiated Emissions Results



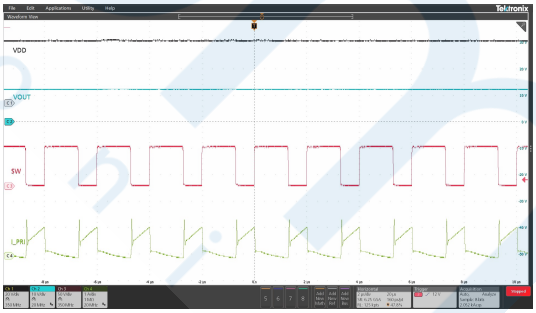
V_{DD} = 48 V, f_{sw} = 500 kHz, V_{OUT} = 12 V

Figure 22. Conducted Emissions Results



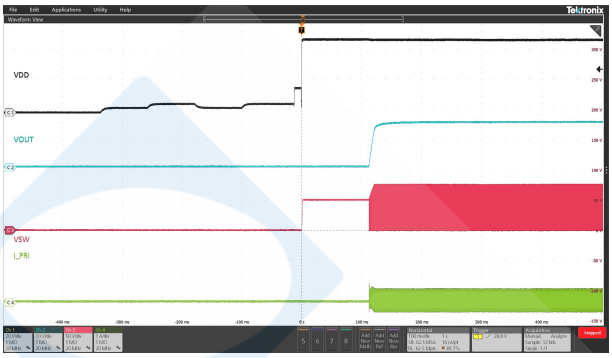
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0 A

Figure 23. Steady Switching Waveforms at Light Load



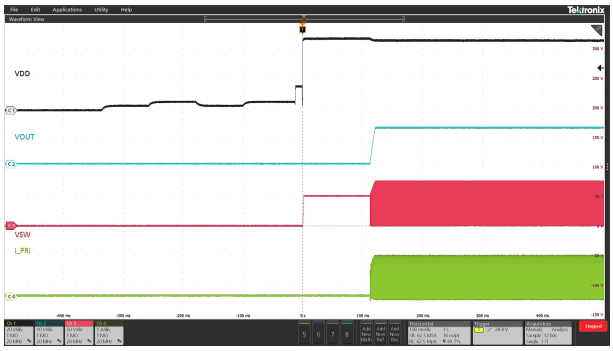
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A

Figure 24. Steady Switching Waveforms at Heavy Load



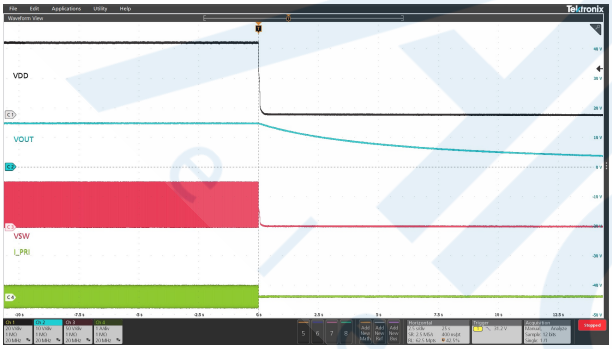
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0 A

Figure 25. Start-up Waveforms through PSE at Light Load



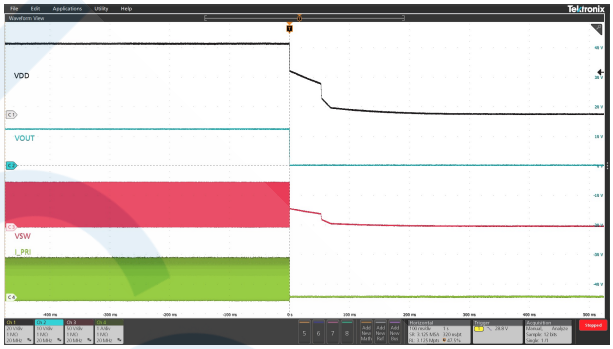
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A

Figure 26. Start-up Waveforms through PSE at Heavy Load



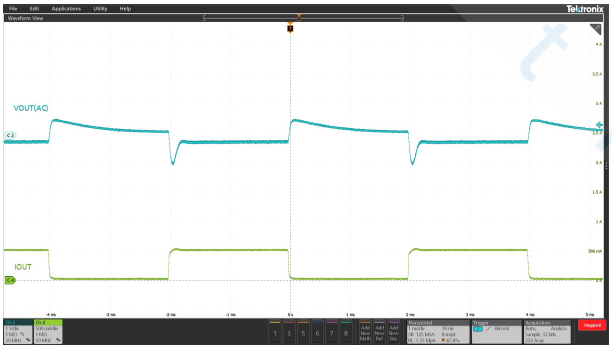
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0 A

Figure 27. Shutdown Waveforms at Light Load



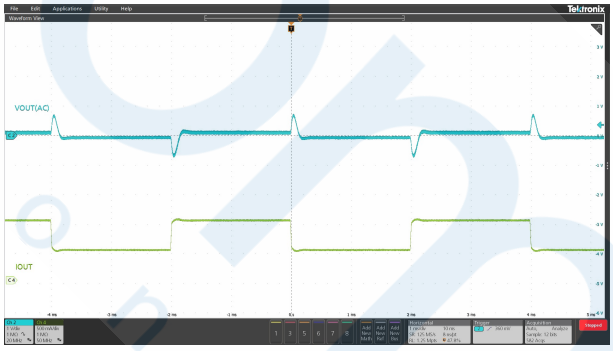
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A

Figure 28. Shutdown Waveforms at Heavy Load



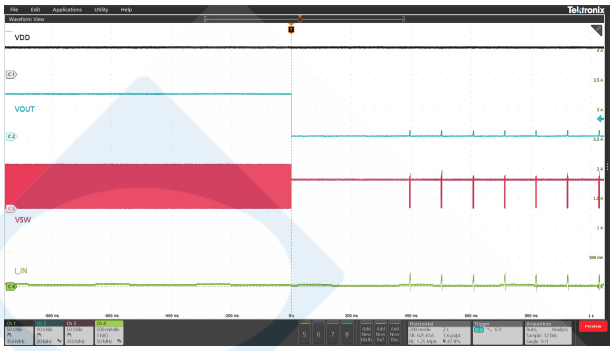
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 10 mA to 0.5 A, 25 mA/µs

Figure 29. Load Transient



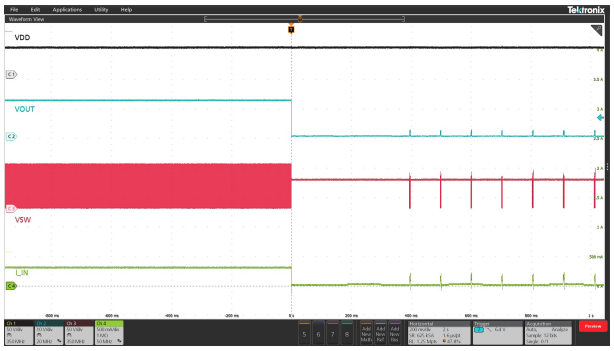
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0.5 A to 1 A, 25 mA/µs

Figure 30. Load Transient



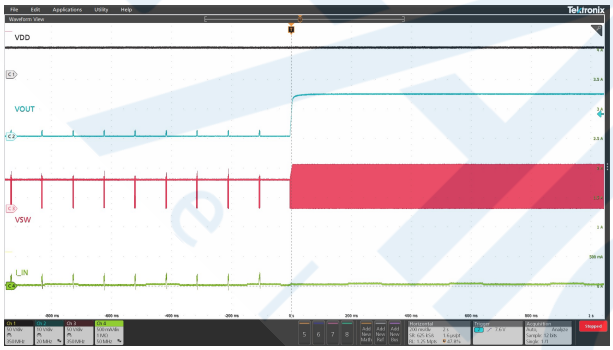
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0 A to short

Figure 31. SCP Entry at Light Load



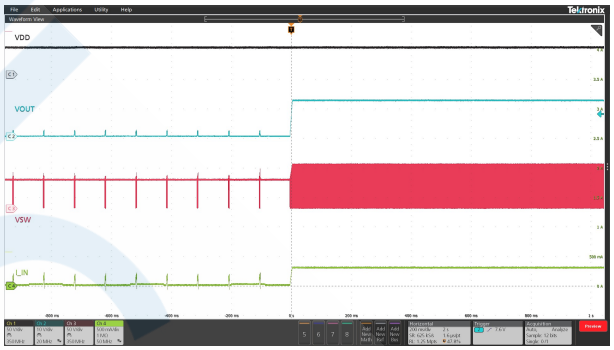
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A to short

Figure 32. SCP Entry at Heavy Load



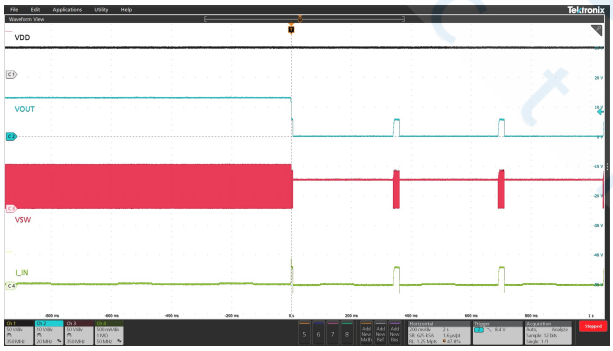
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = short to 0 A

Figure 33. SCP Recovery at Light Load



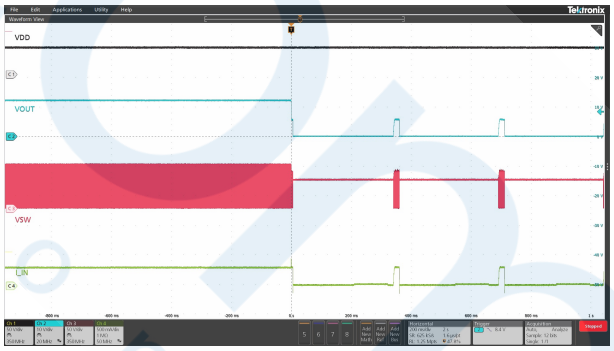
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = short to 1 A

Figure 34. SCP Recovery at Heavy Load



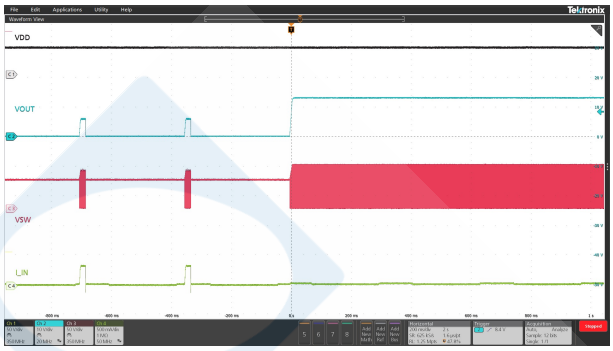
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0 A to overload

Figure 35. OCP Entry at Light Load



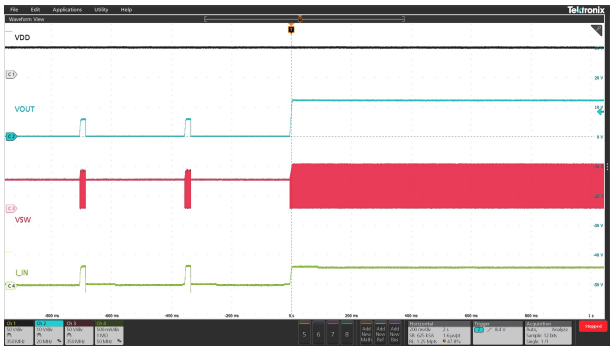
V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = 1 A to overload

Figure 36. OCP Entry at Light Load



V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = overload to 0A

Figure 37. OCP Recovery at Light Load



V_{DD} = 48 V, V_{OUT} = 12 V, I_{OUT} = overload to 1 A

Figure 38. OCP Recovery at Heavy Load

Detailed Description

Overview

The TPE15017 is a monolithic power over ethernet (PoE) powered device (PD) with integrated PD interface and fly-back power converter. The power converter can be set in active clamp PSR flyback mode and active clamp SSR flyback mode. The TPE15017 supports IEEE 802.3af standard interface and targets for small size 13-W isolated PoE applications. The TPE15017 can also support IEEE 802.3at PSE at class 4 level for those applications requiring high peak power above 13 W within short time.

Figure 39 shows the internal block diagram of the TPE15017 and below sections describe the detail functions.

Functional Block Diagram

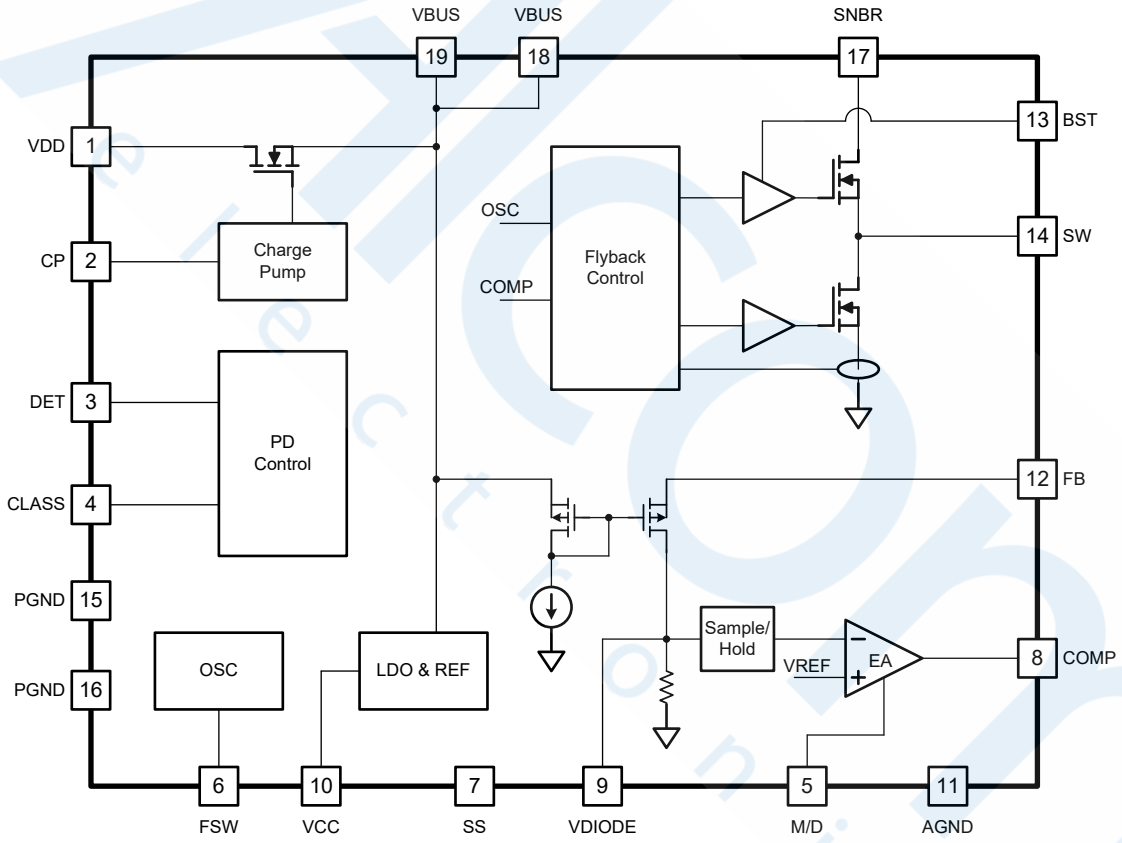


Figure 39. Functional Block Diagram

Feature Description

Detection

In order to identify a device as a valid PD, the Power Sourcing Equipment (PSE) senses the Ethernet connection by applying two voltages in a range of 2.7 V to 10.1 V on the Ethernet cable and measuring the corresponding currents. An equivalent

resistance is calculated using the ΔV/ΔI. During the detection phase, a valid signature resistance between 23.7 kΩ and 26.1 kΩ must be seen from the power interface (PI). Thus, a 24.9-kΩ resistor is recommended between the VDD pin and DET pin to respond the PSE detection.

The DET pin also controls the enable function of the TPE15017 except detection. By pulling the DET pin low, the TPE15017 disables classification, hot-swap MOSFET, power maintain signature and flyback switching. This function can be used to disable flyback converter when an auxiliary adaptor power supply is available on the output of the flyback converter.

Classification

In the classification mode, the PSE will classify the PD for one of five power levels or classes. This allows the PSE to efficiently manage power distribution so that the PSE can support as many loads as it can within its maximum current capability. IEEE802.3af classification mode is active when the PSE presents a fixed voltage between 14.5V and 20.5V to the PD. Then the TPE15017 presents a load current in classification mode as showing in Table 2. The current is measured by the PSE to determine which of the five available classes is advertised.

Table 2. CLASS Resistor Selection

Class	Max. Power to PD (W)	Classification Current (mA)	R_{CLASS} (Ω)
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

PD UVLO and Current Limit

Once the classification is successfully completed, the PSE will rise its output voltage. When VDD voltage is higher than the turn-on threshold, the hot-swap MOSFET switch will start pass a limited current I_{INRUSH} to charge the bulk capacitor at the VBUS pin until the voltage across the hot-swap switch is sufficiently low and the charge current drops to lower than 80% of the inrush current limit. Then the current limit changes to normal operation current limit threshold.

After the 100-ms delay time (T_{DELAY}) from the UVLO starting, the TPE15017 will assert one internal enable signal and go from the startup mode to the running mode after the inrush period elapses, the internal enable signal can enable flyback converter internally.

If the VDD voltage drops below the falling UVLO threshold, the input MOSFET and the DCDC flyback converter both are disabled.

If the output current overloads on the input hot-swap MOSFET, the current limit works and the VBUS voltage drops. When the voltage drop across the VDD pin and the VBUS pin is more than 10V for longer than 1 ms, or the VBUS voltage drops to 15V, the current limit reverts to the inrush limit, and the internal enable signal is pulled down to disable DCDC switching at the same time. Then The TPE15017 works in a new inrush current limit cycle. In this condition, internal enable signal doesn`t have 100ms delay time (T_{DELAY}).

The following figure shows the current limit and internal EN signal work sequence during startup from PSE power supply.

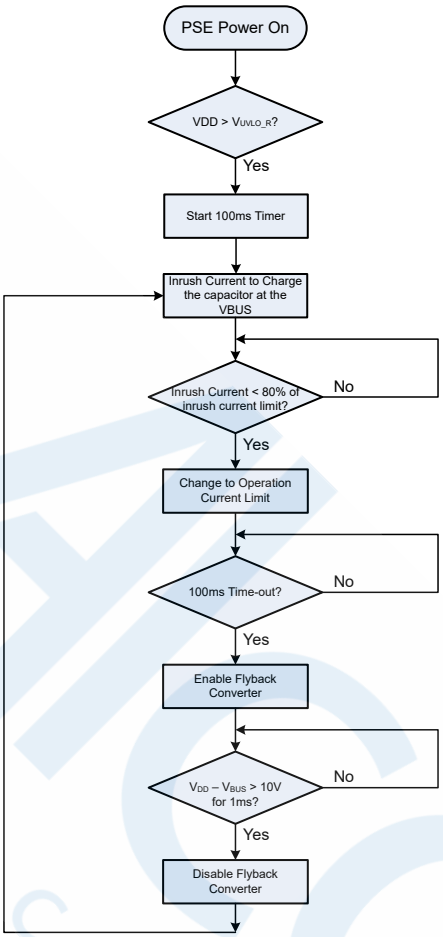


Figure 40. Startup Sequence

VBUS over Voltage Clamp

Except the current limit function, the PD input hot-swap MOSFET can also protect the V_{BUS} from surge voltage from V_{DD}. If the V_{BUS} voltage is charged higher than 63 V, the input MOSFET will be regulated to keep the V_{BUS} voltage at 63 V.

DCDC Converter Startup and Power Supply

The TPE15017 DCDC converter has an internal startup circuit. When the VBUS voltage is higher than the VBUS UVLO rising threshold, the capacitor at the VCC pin is charged through an internal LDO. The V_{CC} voltage is regulated at 5.0V. The internal reference circuit is enabled once the V_{CC} voltage is above its UVLO rising threshold.

When both V_{BUS} and V_{CC} are at high level, and the SNBR voltage is closed to the VBUS voltage, the internal enable signal from the PD controller will enable the DCDC converter. The DCDC converter starts switching and regulates the isolated output.

Flyback Work Mode Detection

The TPE15017 supports active clamp flyback control in both primary-side regulate mode (PSR) and secondary-side regulate mode (SSR). After startup, The TPE15017 detects the M/D pin voltage and latches the work mode. After work mode detection, The TPE15017 can`t change the work mode any more unless the flyback converter is disabled due to the VCC toggling.

In PSR mode, the V_{OUT} feedback signal is detected from the SW voltage through the FB pin without opto-coupler or aux-winding. In SSR mode, the V_{OUT} feedback signal is detected through the COMP pin directly by an external TL431 and an opto-coupler. In both modes, the frequency keeps constant and won't run into sleep mode in light load condition. Which can avoid any audible noise issues from transformer.

PWM Operation

The TPE15017 integrates two MOSFET switches for active clamp flyback design. In each cycle, the low-side MOSFET turns on at the beginning, forcing the current in the transformer to increase, the current through the low side MOSFET is internally sensed. When the sum of sensed current signal and slope compensation signal touches the voltage set by the COMP pin, the low side MOSFET turns off. The transformer current then transmits energy from primary-side winding to secondary-side winding, and charges output capacitor through the schottky diode. At the same time, the high-side MOSFET turns on once the low side MOSFET turns off, providing a clamp loop for the energy in transformer leakage inductance. During the high side MOSFET on period, the energy in transformer leakage inductance can be absorbed by the clamp cap at the SNBR pin, and then the capacitor energy can be discharged back to the output through transformer at the same cycle, finally keep the clamp capacitor voltage in balance in each cycle.

The current of the transformer's primary-side winding is controlled by the COMP voltage. In PSR mode, the COMP voltage is controlled by the output feedback voltage at the FB pin. In SSR mode, the COMP voltage is controlled by the output feedback voltage through an opto-coupler and TL431. Thus the output voltage controls the transformer current to meet the load demand.

One 4.7-μF capacitor is recommended on the SNBR pin to clamp the transformer leakage inductance energy, or else the SW and SNBR pins' voltage may run to high voltage. In case the TPE15017 stops switching due to the UVLO or other protections, both the high side MOSFET and the low side MOSFET keep off.

Voltage Control
PSR MODE

Unlike the traditional flyback with opto-isolator feedback, the TPE15017 can detect the transformer primary winding voltage (V_{SW}-V_{BUS}) from the FB pin during the secondary-side output diode conduction period.

Assume the secondary winding is the master, and the primary winding is the slave. When the secondary-side diode conducts, primary winding voltage is:

$$V_{PRI} = \frac{N_P \times (V_{OUT} + V_D)}{N_S} \quad (1)$$

The TPE15017 senses the primary side winding voltage through the FB pin, which generates one feedback current I_{FB} through the resistor:

$$I_{FB} = \frac{V_{PRI}}{R_{FB}} \quad (2)$$

Where:

I_{FB} is the feedback current, it is 100uA

V_D is the output diode forward-drop voltage

V_{OUT} is the output voltage

V_{PRI} is transformer primary winding voltage

N_P and N_S are the turns of the primary winding and output winding, respectively

R_{FB} is the resistor from the SW pin to the FB pin.

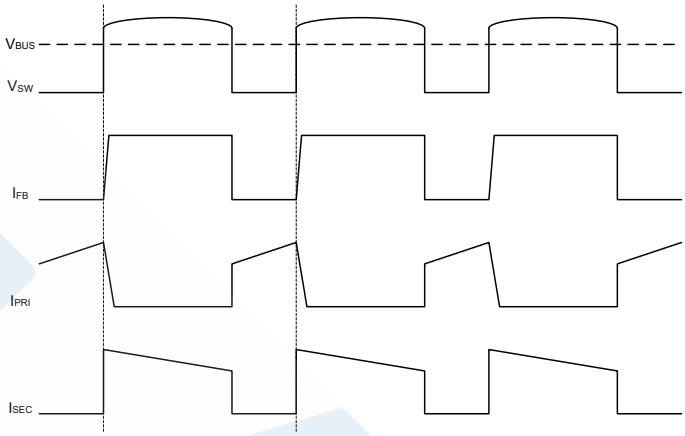


Figure 41. FB Feedback Control

The TPE15017 samples the primary side winding voltage after the low side MOSFET turns off. Blanking time is added to avoid SW rising edge affection. To guarantee long enough FB sensing period, the TPE15017 has a minimum low side MOSFET off time, which also limits the maximum duty cycle when the switching frequency is high.

During FB sensing period, the FB signal is sent into the negative input of the error amplifier and held after the sense window is close.

SSR MODE

The TPE15017 can also be set as SSR flyback mode. In SSR mode, the V_{OUT} voltage signal feedback to COMP pin through one opto-coupler and TL431. The internal error amplifier is disable. The FB pin is only used for OVP protection.

Output Voltage Compensation

In PSR mode, the primary-side winding voltage reflects the secondary-side winding voltage with transformer turns ratio. However, the output voltage differs from the output winding voltage due to the output rectifier diode voltage drop and the power winding resistance. The dropout voltage varies when the conducted current changes. The TPE15017 has a VDIODE pin which can be used to compensate the dropout voltage when current varies.

The TPE15017 senses the low side MOSFET current when it is on, and then hold the current signal when the low side MOSFET is off. By filtering the current signal, the TPE15017 controls a current sinking from the FB pin based on the sensed low side MOSFET current in each cycle. Different resistor on the VDIODE pin sets the different sinking current from the FB pin, which is determined by Equation 3.

$$I_{FB\_COMP} = \frac{I_{IN} \times G_{D\_COMP}}{D \times R_{VDIODE}} \quad (3)$$

Where:

I_{FB_COMP} is the expected compensation current into the FB pin

I_{IN} is the average input current

G_{D_COMP} is the VDIODE compensation gain

D is the duty cycle

R_{VDIODE} is the resistance between the VDIODE pin and ground

The FB sinking current leads to voltage drop on feedback resistor between the SW and the FB pin so that it compensates the V_{OUT} voltage when load varies.

In SSR flyback mode, this voltage compensation function is disabled.

Dual Triangle Frequency Dithering Function

The TPE15017 supports frequency dithering function by different M/D pin settings. During startup, the TPE15017 outputs 100μA current to M/D pin to detect the resistor setting after the VCC voltage is ready. Refer to Table 3 for detail.

The M/D pin detection current lasts about 200 μs. Normally one resistance from the M/D pin to AGND is good enough. In noise environment, it may need a capacitor from the M/D pin to AGND to provide filtering. The capacitor should be less than 100 pF so that the M/D pin voltage can rise to steady state before the TPE15017 detects it.

Table 3. M/D Function Setting

Pin to GND Resistance (kΩ)			MODE	Dither Function
MIN	TYP. (1%)	MAX		
0	0	0.82	PSR	Yes
6.2	6.8	7.68	PSR	No
13.7	15	16.2	SSR	No
24.9	Float	Float	SSR	Yes

Dual Triangle spread spectrum combines a low frequency triangular modulation profile with a high frequency triangular modulation profile. The modulation frequency of the low frequency triangular modulation is about 12.5 kHz. The modulation frequency of the high frequency triangular modulation is about 100 kHz. Figure 42 shows the frequency dithering range.

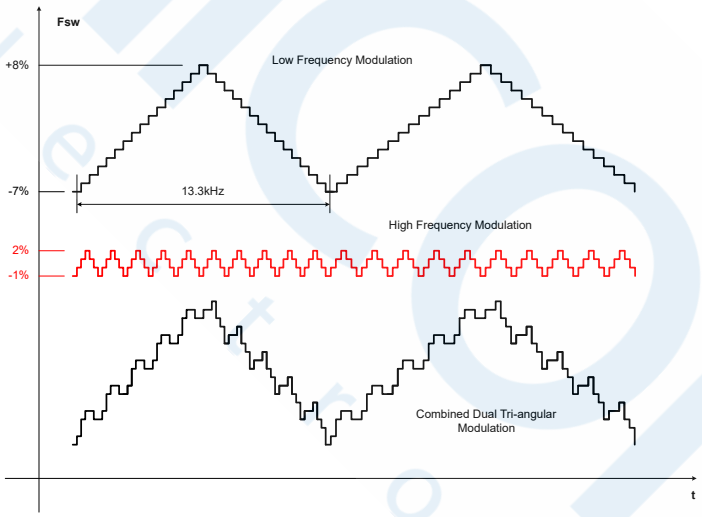


Figure 42. Dual Tri-angular Switching Frequency Dithering

Overload Protection

The TPE15017 senses the low side MOSFET current in each switching cycle. When the low side MOSFET current trips the current-limit threshold, the TPE15017 turns off the low side MOSFET for this switching cycle until the internal oscillator starts the next cycle. The TPE15017 has cycle-by-cycle over current protection (OCP).

If the load current continues increasing after triggering OCP, the output voltage will decrease, and the peak current will trigger switching limit every cycle. The TPE15017 sets overload protection (OLP) by continuously monitoring the low side MOSFET current.

Once the SS voltage is charged to 3.5 V after start-up (soft start complete), the OLP protection is enabled. If an OCP signal is detected, the soft start charging current is disabled and one over current discharge source is enabled, the SS voltage drops with the rate of 20-μA current. At the same time, a 50-μs one-shot timer is activated and it remains active for 50 μs after

the OCP condition stops. The 20-μA discharge source current cannot be turn off until the one-shot timer becomes inactive. When the OCP disappears before at least 50 μs prior than the SS capacitor discharging to 3 V, the TPE15017 will run back to normal work condition and the SS capacitor will be re-charged to 3.5 V with 50-μA current. When the SS capacitor is discharged to 3 V, the TPE15017 will register it as overload condition and turn off the switching MOSFETs until next re-start cycle. At the same time, the 20-μA discharge current changes to 2-μA. After the SS voltage is discharged to 0.2 V, the TPE15017 will re-start up with new soft-start cycle. This is hiccup mode protection.

The OLP detection function is disabled after the SS voltage is discharged to be lower than 3V and it will be re-enabled after SS voltage is recharged to 3.5 V. So the OLP only occurs after the soft-start is completed.

Short Circuit Protection (SCP)

When the output is shorted to the ground, the TPE15017 works in OCP mode and current is limited cycle-by-cycle. The device may run into OLP protection. However, when the peak current cannot be limited by cycle-by-cycle limit due to minimum on time, the current may run out of control and the transformer may run into saturation. If the monitored low side MOSFET current reaches SCP threshold, the part will turn off switching MOSFETs and run into hiccup protection immediately by discharging the SS capacitor with 2-μA current. The device will also restart up when the SS voltage is discharged to 0.2V.

During the SCP condition, when the low side MOSFET current does not reach the SCP threshold, but the high side MOSFET negative current is higher than the high side MOSFET negative current limit, the TPE15017 also runs into hiccup mode and discharge the SS capacitor with 2-μA current until 0.2 V.

Over-voltage Protection (OVP)

The TPE15017 has output over-voltage protection (OVP) in both PSR and SSR mode by sensing the current into the FB pin. When the feedback current into the FB pin exceeds 125 percent of I_{REF}, the TPE15017 shuts off the switching, and enters hiccup mode immediately by discharging the SS capacitor with 2-μA current. The device will also restart up after the SS voltage is discharged to 0.2 V.

To avoid the mis-trigger due to the oscillation of the leakage inductance and the parasitic capacitance, the OVP sampling has a T_{OVPS} blanking time.

The TPE15017 also monitors the SNBR pin for maximum over voltage protection. Once the SNBR pin voltage exceeds 105V, TPE15017 turns off all switching, and then discharges the SS to 0.2 V and discharge the SNBR voltage to the VBUS voltage before re-start again.

Soft Start

The TPE15017 provides soft start by charging an SS pin capacitor with a current source. During soft-start period, the SS voltage ramps up slowly. The soft-start capacitor is discharged completely in normal shutdown, thermal protection or other protection conditions.

In PSR mode, the SS signal clamps the feedback voltage until meeting reference voltage. In SSR mode, the SS signal clamps the COMP voltage until the level meeting the switching current. Then SS signal ramps up with the same rate reaching to 3.5 V. The SS time is controlled by the capacitor on the SS pin.

During soft start period, the switching frequency is fold-back when SS is low, refer to the Switching Frequency section for more detail.

Switching Frequency

The switching frequency of the TPE15017 is set by an external resistor between the FSW pin and AGND. The resistor value can be calculated by Equation 4.

$$R_{SW} = \frac{4650}{f_{SW}} \quad (4)$$

Where：

R_{SW} is the frequency setting resistor in kΩ.

f_{SW} is the expected frequency in kHz.

The TPE15017 works with this switching frequency in full load range. The device doesn't decrease frequency in no load condition. Generally, the switching frequency is set between 80 kHz to 650 kHz per application demand.

The TPE15017 has frequency fold-back function during soft-start, which prevents transformer saturation when the low side MOSFET reaches minimum on time condition. The fold-back frequency is 80k when the SS voltage is below 0.2 V. The switching frequency increases slowly to normal frequency with the SS voltage rising. After soft start completes, the frequency fold-back function is disabled.

BST Power Supply

The TPE15017 integrates both low side MOSFET and high side MOSFET for active clamp topology. The high side MOSFET driver is supplied by the BST pin. During startup, the BST pin is charged up by an internal charge-pump from CP pin. During stead state switching mode, the BST capacitor can be charged up by VCC when the low side MOSFET turns on.

Minimum On Time and Minimum Off Time

The transformer's parasitic capacitance induces a current spike on low-side power MOSFET when it turns on. The TPE15017 includes a leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled and the switching power MOSFET can not switch off.

The TPE15017 also limits the minimum off time to ensure the primary side feedback loop can work well. Refer to the Voltage Control section for detail.

Thermal Protection (OTP)

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature is higher than its upper threshold, the TPE15017 shuts down the whole chip including the PD controller and the DCDC converter.

When the temperature is lower than its lower threshold, the OTP cool down timer counts out and the SNBR voltage is discharged to close to VBUS, the chip is enabled again with a new start-cycle.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPE15017 is designed for PoE PD applications with 48-V input voltage. It integrates all PD detection, classification functions and flyback converter.

Typical Application

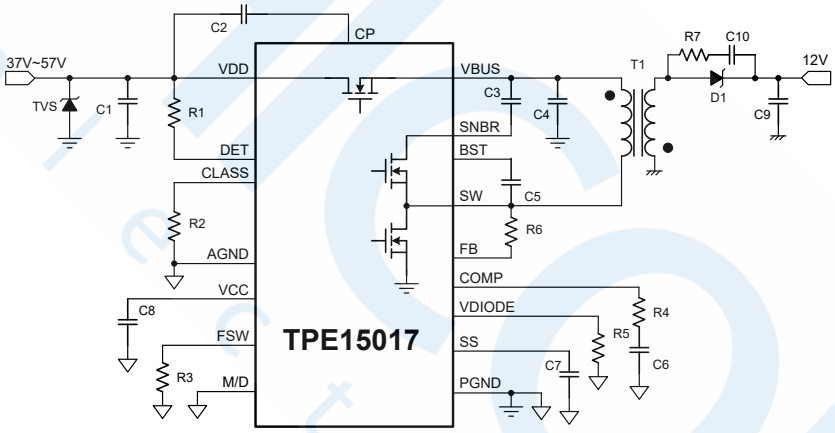


Figure 43. TPE15017 48 V to 12 V Flyback Application Circuit

Detection Resistor

In the Detection Mode, a resistor connected between the DET pin and the VDD pin is needed as a load to the PSE. The resistance is calculated as a $\Delta V/\Delta I$, with an acceptable range of 23.7 kΩ to 26.1 kΩ. Use a typical value of 24.9kΩ as detection resistor.

Classification Resistor

In order to distribute power to as many loads as possible from PSE, a resistor between the CLASS and AGND pins is used to classify the PD power level. The TPE15017 draws a fixed current set by classification resistor. The supplied power to PD set by classification resistor is shown in Table 2. Typical voltage on the CLASS pin is low, so it only produces a little power loss on class resistor even in the class 4 range.

Protection TVS

To limit input transient voltage within the absolute maximum ratings, a TVS across the rectified voltage (V_{DD}-V_{SS}) must be used. A SMAJ58A, or equivalent, is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

PD Input Capacitor

An input bypass capacitor (from VDD to VSS) of 0.05μF to 0.12μF is needed for IEEE 802.3af standard specification. Typically a 0.1-μF, 100-V ceramic capacitor is used.

Output Voltage Setting

The TPE15017 has two feed-back Mode, PSR and SSR.

In PSR mode, TPE15017 senses the primary side winding voltage through the FB pin, the output voltage can be calculated as blew:

$$V_{OUT} = \frac{I_{FB} \times R_{FB}}{N_P} \times N_S - V_D \quad (5)$$

Where

V_{OUT} is the output voltage.

R_{FB} is the SW to FB resistance.

I_{FB} is the feedback current, it is 100 μA.

V_D is the output diode forward-drop voltage.

N_P and N_S are the turns of the primary winding and output winding, respectively.

In SSR Mode, the output voltage is set by an external TL431, suppose the TL431's reference voltage is 2.5 V, and expected output voltage is 12 V, the upper and lower divider resister ratio is 3.8. Then the TL431 generates an amplified signal and controls the COMP pin of the TPE15017 through an opto-coupler, such as PC357. COMP controls the current, and then the output voltage is regulated based on the feedback signal.

Work Mode/Frequency Dithering Setting

After enabled, the TPE15017 outputs a current to the M/D pin to detect the M/D resistance. Table 3 shows the programming options.

Selecting Transformer

A transformer is important in a fly-back converter since it determines the duty cycle, peak current, efficiency, MOSFET, output diode rating, and so on.

The transformer winding ratio determines the duty cycle. Calculate the duty with Equation 6.

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (6)$$

Where:

D is the duty cycle.

N is the transformer primary winding to output winding ratio. For this typical application, 2:1 winding ratio for 12-V output matches the SW voltage rating.

The primary-side inductance affects the input current ripple ratio factor. A high inductance results in a large transformer size and high cost. A low inductance results in high switching peak current and RMS current, which causes a decrease

in efficiency. Choose a primary-side inductance to make the current ripple ratio factor around 30% ~ 50%. Estimate the primary-side inductance with Equation 7.

$$L_P = \frac{V_{IN} \times D^2}{2 \times K_P \times I_{IN} \times f_{SW}} \quad (7)$$

Where:

K_P is the current ripple ratio.

I_{IN} is the input current.

L_P is the primary inductance.

Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current. Otherwise, the transformer inductance decreases sharply.

The current rating counts the max RMS current, which allows flow through each winding. The current density should be controlled. Otherwise, it can cause a high resistive power loss.

VOUT Compensation Setting

The TPE15017 senses the low side MOSFET current when it is on, and controls a current sinking into the FB pin based on the sensed low side MOSFET current in each cycle. Different resistor on the VDIODE pin sets the different sinking current, which is determined by Equation 3.

Selecting Output Diode

The flyback output rectifier diode supplies current to the output capacitor when the primary side MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than the value calculated from Equation 8.

$$V_{DR} = \frac{V_{IN}}{N} + V_{OUT} \quad (8)$$

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current.

An R-C snubber circuit for output diode is recommended for better EMI performance.

Input Capacitor Selecting

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, and tantalum or low-ESR electrolytic capacitors may also suffice. For ceramic capacitors, the capacitance dominates the input ripple at the switching frequency.

The input ripple can be estimated with Equation 9.

$$\Delta V_{IN} = \frac{V_{IN}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{IN}}{C_{IN}} \quad (9)$$

Where

ΔV_{IN} is the input voltage ripple

I_{IN} is the input current

C_{IN} is the input capacitor.

Output Capacitor Selecting

The output capacitor maintains the DC output voltage. For best results, use ceramic capacitors or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the output ripple at the switching frequency.

The output ripple can be estimated with:

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (10)$$

Application Examples

Non-Isolated PoE PD

The TPE15017 also can be configured as a non-isolated DCDC converter using an inductor. The following figure shows the typical application schematic of -48 V to 12 V converter.

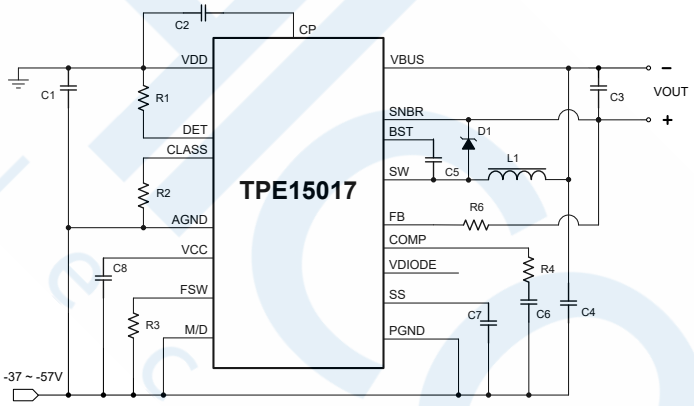


Figure 44. TPE15017 Non-Isolated Application Circuit

Layout

Layout Guideline

Efficient layout of the PoE front-end and high frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, follow the guidelines below.

- Keep the input-switching loop between the flyback input capacitor, the transformer, the SW pin and PGND as short as possible.
- Keep the output loop between the rectifier diode, the output capacitor and the transformer as short as possible.
- Keep the active clamp loop between the active clamp capacitor, the transformer, the SW pin and the SNBR pin as short as possible.
- Keep the input hot-swap loop between the PD input capacitor, the VDD pin, the VBUS pin and the VBUS capacitor as short as possible.
- The VCC capacitor must be placed close to the VCC pin for best decoupling.
- The feedback trace should be short and far away from noise source such as switching node.
- Other signal leads should be as short as possible, such as the DET, CLASS, COMP, VDIODE, SS, and FSW pins.
- CP loop and BST loop should be short for good hot-swap and HS-FET driver.
- Use single point connection between the power ground and the signal ground.
- Use copper and vias under the TPE15017 package for good thermal performance.

Refer to below figure for recommended layout, which is referenced to Figure 43. For more detail information, refer to the offiial evaluation board.

Layout Example

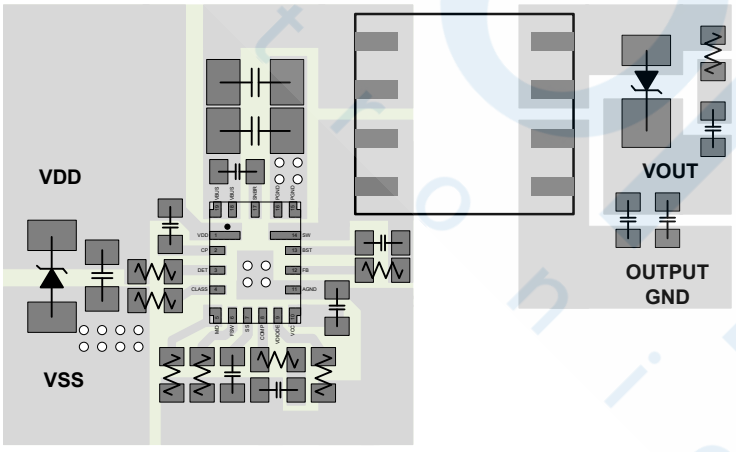
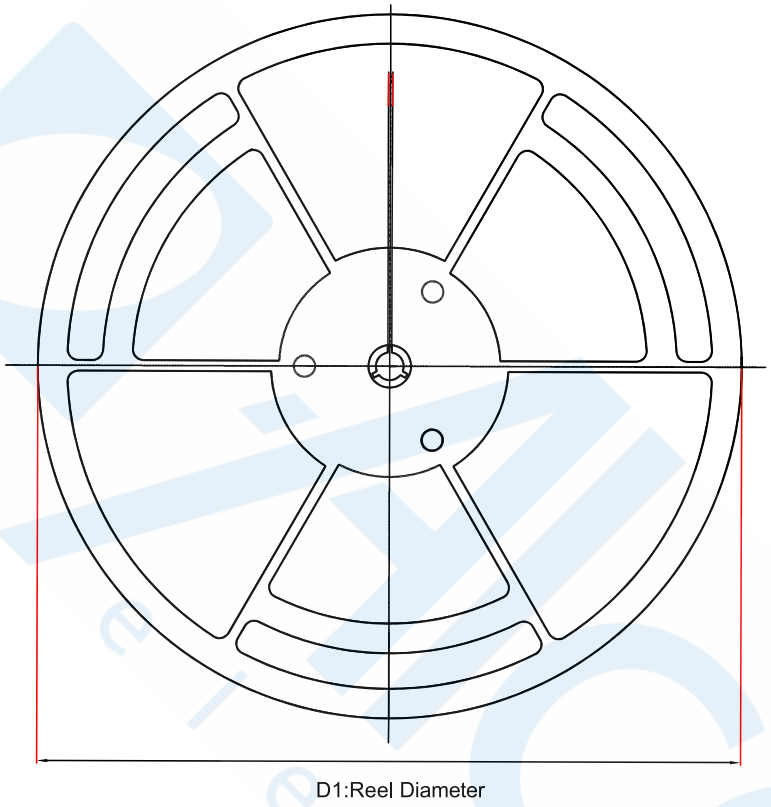
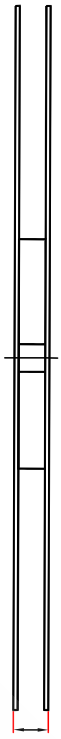
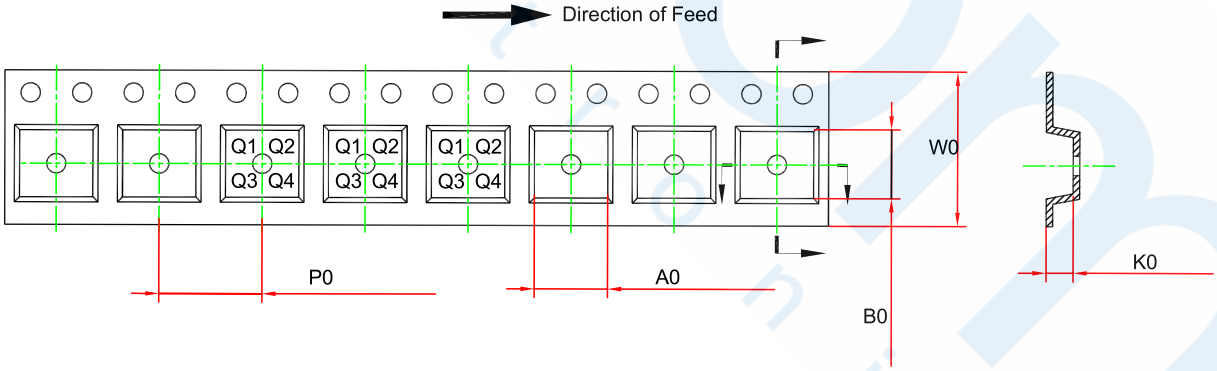


Figure 45. PCB Layout Example

Tape and Reel Information





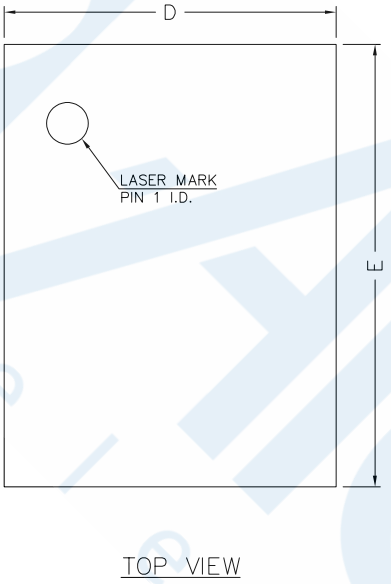


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPE15017-QF5R	QFN3X4-19	330	17.6	3.3	4.3	1	8	12	Q1

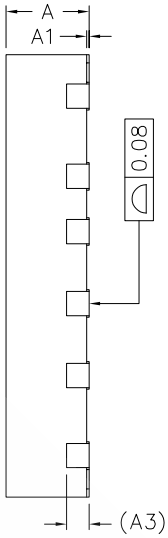
Package Outline Dimensions

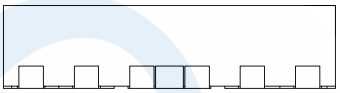
QFN3X4-19

Package Outline Dimensions QF5(QFN3X4-19-A)

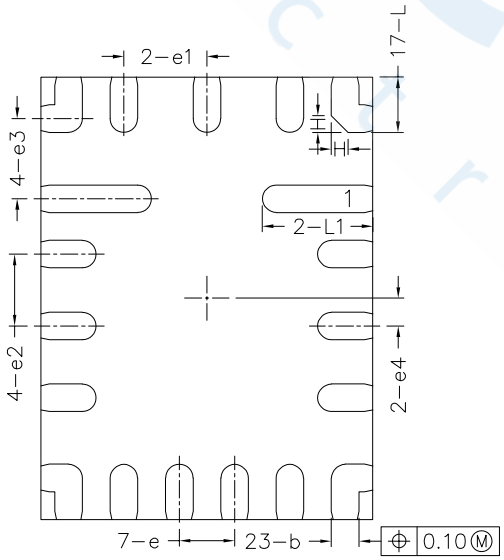


TOP VIEW





SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
E	3.900	4.100	0.154	0.161
e	0.450	0.550	0.018	0.022
e1	0.700	0.800	0.028	0.031
e2	0.600	0.700	0.024	0.028
e3	0.675	0.775	0.027	0.031
e4	0.200	0.300	0.008	0.012
L	0.450	0.550	0.019	0.022
L1	0.950	1.050	0.037	0.041

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPE15017-QF5R	−40 to 125°C	QFN3X4-19	15017	MSL1	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.